Low *k* Dielectrics:

# Integration of Plasma Deposited Fluorocarbon Polymer Low *k* Material in a Copper / Low *k* Damascene Architecture

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**Introduction**

Nowadays the implementation of copper and low *k* material into IC fabrication is a serious issue for IC manufacturers. The application of these films is combined with the damascene technology. At present, numerous low *k* materials were investigated with respect to their low *k* characteristics. In general, organic materials were described to be very soft, thermally unstable [1] and should have poor thermal conductivity. PTFE-like materials consisting of carbon and fluorine have, due to their low values of the dielectric constant, the potential to be used as IMD [2]. Unfortunately, this material group normally shows very bad adhesion with respect to other technology relevant film materials like $SiO_2$, SiN and barriers [3]. The way to overcome this limitation was already presented [4]. The integration of PECVD deposited CF based low *k* material in a single damascene architecture will be demonstrated and the compatibility of low *k* materials with existing technological processes was evaluated.

**Experiment**

***Low k stack patterning***

Furthermore for technology integration within a copper / low *k* damascene architecture, the polymer films have to be patterned and should be able to withstand CMP processes. Because usually organic materials cannot be patterned directly by a photosensitive organic resist, a well adhering hardmask (e.g. $SiO_2$) has to be used on top of the CF low *k* film stack. The hardmask was patterned after lithography (wafer stepper or electron beam exposure) by reactive ion etching (RIE). Stepper lithography required a partial hardmask RIE, followed by resist stripping and final hardmask etch (RIE). For e-beam lithography, the resist was stripped in situ during low *k* stack RIE. Low *k* stack etch was stopped on a Si-N film. An oxygen based RIE process is used for low *k* etch with etch rates of up to 500 nm/min. As shown in figure 1a and 1b the patterning of the dielectric stack could be demonstrated on a single damascene film stack (1 µm $SiO_2$, 50 nm PECVD SiN on Si).

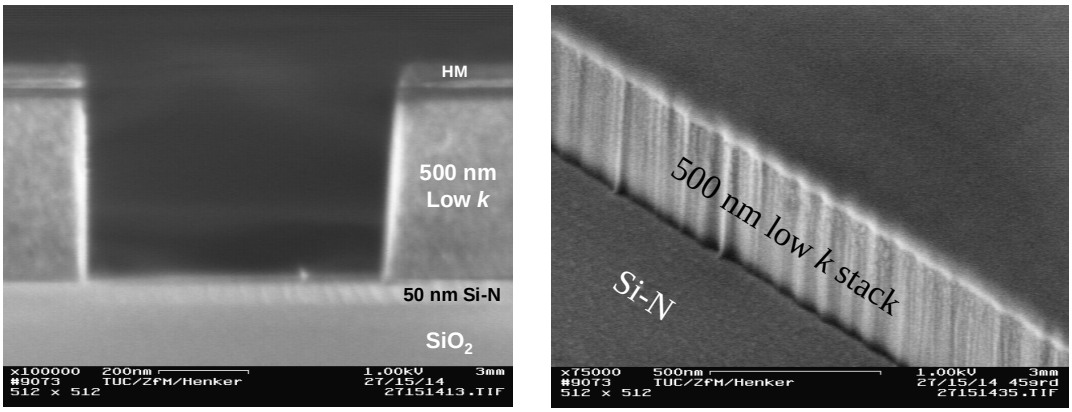


Figure 1a and 1b: HR-SEM of RIE patterned low *k* stack

***Barrier and copper deposition***

Barrier deposition was tested with TiN CVD barriers and Ta / TaN PVD barriers. Both materials were applied. The electro-chemical deposition (ECD) of copper requires the previous deposition of a copper seed layer (sputtering) and a wet chemical conditioning to achieve good adhesion and gap fill. Conventional electrolyte was used for copper ECD.

***CMP processing***

The basis for a successful CMP processing is a minimum mechanical stability of the low *k* material and excellent adhesion to each other of all films in the damascene stack. According to Lin et al. [5] materials with high Young´s modulus (E > 3.5 GPa) and high hardness (H > 0.3 GPa) are able to withstand CMP.
In Table 1 the requirements for low *k* materials to withstand CMP processing are summarized.

| Hardness [GPa] | Young`s Modulus [GPa] | CMP ability |
|---|---|---|
| > 0.5 | > 4 | Blanket CMP: OK<br>Integration CMP: OK |
| 0.4 ... 0.5 | 3 ... 4 | Integration CMP: OK |
| 0.2 ... 0.4 | 1.6 ... 3 | Integration CMP: Struggling |
| < 0.2 | < 1.5 | Integration CMP: Bad |

Table 1: CMP processing - mechanical requirements for low *k* materials [5]

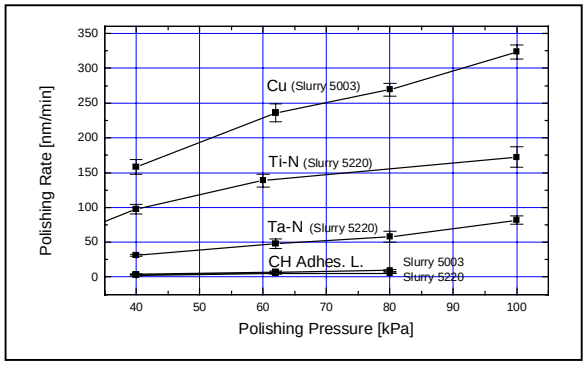


Figure 2: Polishing rates for Cu, barrier and CH adhesion layers using commercially available slurries

The plasma deposited CF film stack described here, offers E > 5.5 GPa (results from LSAW - Laser induced Surface Acoustic Wave analysis) and H > 0.5 GPa (nanoindentation) [6]. Moreover, as demonstrated by the polishing rates using commercially available slurries (Fig. 2) the upper adhesion layer of the CF polymer stack acts as CMP stop layer. Compared to Cu and various barrier layers the CH polishing rate ($R_{pol}$) is much smaller. Figure 3a and 3b show Cu / CF polymer single damascene architectures after CMP processing.

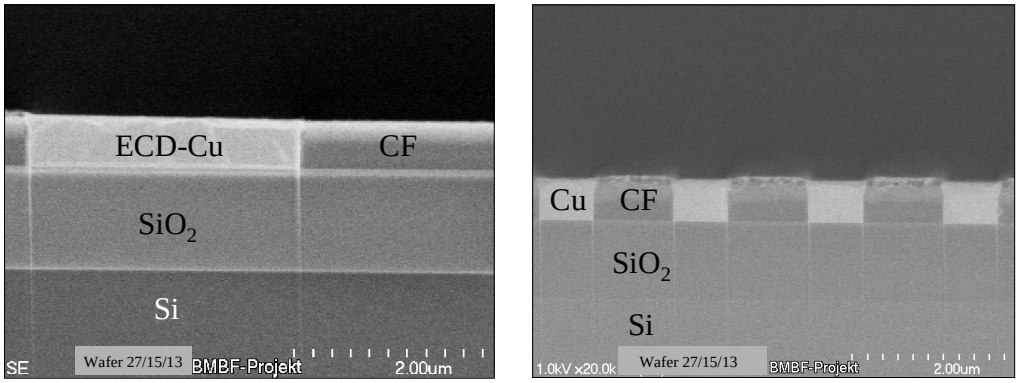


Figure 3: Cross section (FIB preparation) of a CF polymer low *k* / Cu single damascene stack after CMP

**Summary**

CF polymers with ultra low dielectric constant ($k < 2.2$) were deposited successfully by plasma enhanced chemical vapor deposition. Adhesion of the CF polymer with respect to the etch stop as well as the hardmask films can be increased easily by in situ deposition of a very thin (5 ... 10 nm) lower and upper adhesion layer. Fortunately, this adhesion promoting material can be considered as low *k* dielectric material, too ($k = 2.7$). Thus the adhesion layers have only slight influence on the dielectric stack characteristics. Moreover, the upper CH adhesion layer can be applied as CMP stop layer due to the low polishing rate. As a whole, deposition processes, patterning and CMP of a Cu / CF low *k* single damascene architecture is been demonstrated successfully using IC fabrication compatible chemicals and tools.

**References**

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