Tunable Fabry-Perot-Interferometer for 3 - 4.5 µm Wavelength with Bulk Micromachined Reflector Carrier

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Much effort has been involved in developing micromachined optical filters on base of Fabry-Perot interferometers (FPI) in recent years. Most of them is dedicated to wavelength division multiplexing for optical communication or for gas analysis in near infrared, e.g. 1.5 µm wavelength, applying self-supporting InP-air based Bragg mirrors [1,2]. An FPI applying single layer silver mirrors evaporated on Si_3N_4 membranes as carrier supported by a solid thick Si rim is used for the visible spectral range resulting in high reflectivity over a wide wavelength range and in narrow bandwidth [3]. However, the transmittance is limited to about 20% because of absorption in Ag layers [4]. Dielectric mirror based FPIs for infrared radiation suitable for e.g. the chemical analysis by spectroscopy are presented in Refs. [5, 6].

The approach discussed here is based on bulk micromechanics. The device (Fig. 1) consists of a carrier for the fixed mirror and electrodes (layer 1), the movable mirror carrier and suspension (layer 2 and layer 3) and the upper electrode (layer 1). Mirrors of dielectric layer stacks enclose the cavity in first order configuration. The cavity size is electrostically tuned and capacitively detected by a closed loop control. The optical active area with 2.2 x 2.2 mm² is placed in the middle of the driving and detection electrodes, the suspension with diagonal bending beams and the rim.

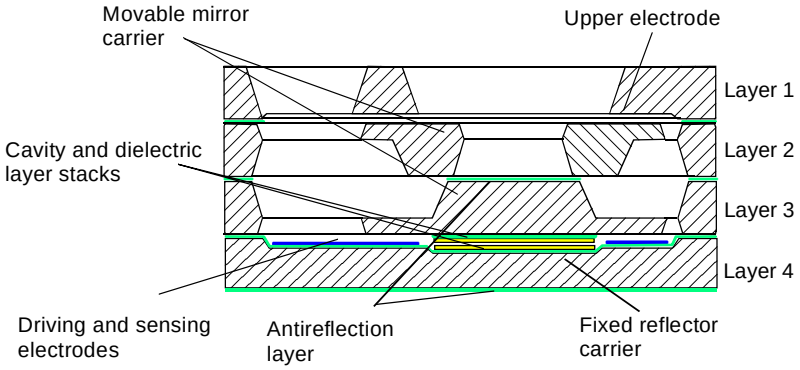

Fig. 1. Cross sectional drawing of the FPI

Relatively thick (300 µm Si) mirror carriers are used for both, the fixed and the movable mirror. It results in very low mirror curvature what is beside of good parallelism a necessity for a uniform cavity size over the optical active area. The loss due to the thick substrate has been minimized by choosing lowly doped silicon with high specific resistance (e.g. 4 ... 10 Ω cm).

The mirrors of the FPI consist of two or three quarter wavelength stacks each (two versions). Polysilicon is used for high refractive material and SiO_2 for low refractive material. The first low refractive layer is a thermally grown λ/4 thick SiO_2 layer on top side of the layer 4 and bottom side of layer 3 in the optical active area. It is followed by a polysilicon high refractive layer. A second and a third quarter wavelength stack (in case of version 2) of PECVD-SiO_2 and polycrystalline silicon complete the mirrors. We use a λ/4 thick SiO_2 layer with a conformal lateral shape as stress compensation and as an antireflection layer on each other side of this 3rd and 4th layer. Results of reflectivity measurements are depicted within Fig. 2. Three quarter wavelength stacks have a reflectivity of more than 95% in the wavelength range of 3 ... 5 µm compared to a gold surface.

The movable mirror carrier consists of layer 2 and layer 3. Each layer is elastically suspended by four diagonal bending beams located in the corners (Fig. 3a). This arrangement in combination with a parallel spring suspension (Fig. 3b) resulting in eight diagonal bending beams provides a vertical movement and a higher stiffness regarding a tilting of the movable mirror carrier. The center of gravity has been placed in the middle plane between layer 2 and layer 3 in order to prevent tilting by gravity force. Four fixed electrodes at the top side of layer 4 surrounding the mirror are used for electrostatic driving and capacitive detection of the cavity size (Fig. 3c). The electrodes are separately wired to the electronics to have the opportunity to detect and compensate the tilt of the movable mirror. The outer movable part of layer 3 and layer 2 is used as movable electrodes. Applying a negative bias voltage to the fixed electrodes of layer 4 and a positive bias voltage to the layer 1 the movable mirror can be actuated by a applying a voltage in the range between the bias voltages to it.

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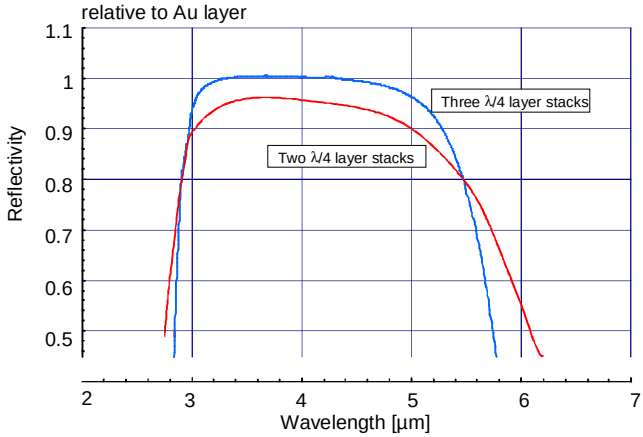
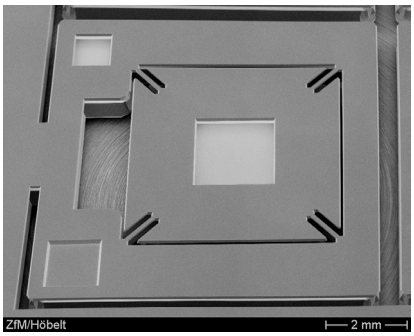
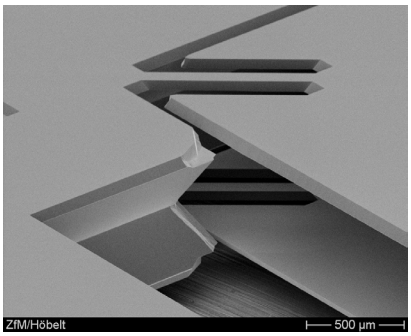


Fig. 2. Measurement result of the reflectivity of the layer stack relative to a gold layer

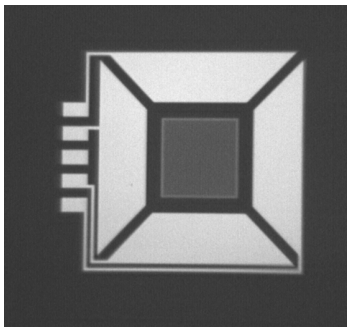
Four 300 µm thick, double side polished 4“ Si wafers are processed to form the layers 1 ... 4. For a high transmission in IR, layers 3 and 4 should have a high resistivity (low doping). Wafers with 10 ... 40 Ωcm are available with a very good quality and low thickness tolerance (TTV < 1 µm). Layers 1 and 2 do not have an optical function and should provide a good conductivity, therefore a resistivity of 0.01 ... 0.05 Ωcm is used.



a) SEM picture of layers 2 and 3



b) parallel spring suspension



c) layout of the fixed electrodes

Fig. 3 Design of movable mirror carrier and fixed mirror carrier with electrodes

Well established Silicon bulk technology in combination with direct wafer bonding is used to pattern the layers and to fuse them together. Direct bonding can be applied with or without thermal oxide layers, as high or low temperature process [7]. No other intermediate layers are necessary. This allows the small gaps to be adjusted with a very good accuracy. The technology of layers 3 and 4 must integrate both mechanical patterning (plates, springs, gaps) and the dielectric layer system. Layer 3 starts with creating the bottom λ/4-layer. It would be possible at first to create the optical layer system, but this multi layer system with a nitride mask on top was found to be not stable during the relatively long (240 µm) Si wet etch process (using KOH solution with 30% KOH concentration at 80°C). Therefore, the concept has been changed to realize the deep etching before creating the optical stack. This process creates a 60 µm thick membrane with no limitations for lithography on this side. Now the optical layer stack is patterned. Finally, the springs are etched using a low stress PECVD nitride mask layer. The four springs have a 45° orientation with respect to wafer flat and are defined by <100> planes, which have equal etch rates in vertical and lateral directions. After perforation of the wafers, the etching is continued until a spring width of 100 µm is reached. A very well defined geometry of the springs with nearly perpendicular and flat side walls is reached by this process. The springs in layer 2 are fabricated with an equal technology. After bonding of layers 2 and 3, the springs form a parallel spring suspension (see Fig. 3).
Within layer 4, the electrostatic and optical gaps are defined at first. Then the mask layer is removed and thermal oxide is grown for the bottom λ/4-layer. This layer also provides the bond surface and is therefore protected with a nitride layer. Next step is the optical stack patterning similar to layer 4. Finally, metallic electrodes and contacts are formed.
The mounting process starts with bonding of the layers 2 and 3. RCA cleaning is used for surface activation. An optical mark system allows the alignment of the wafers with about 5 µm accuracy. Pre-bonding is carried out at room temperature with a slight mechanical pressure. The result can be checked by infrared transmission light. A special wafer design with suspension of the chips only at one side in the wafer frame contributes to a high bond yield. Afterwards, an annealing process at 900°C is applied to strengthen the bond. The second bond process is realized with simultaneously bonding of layers 1 and 4 to the compound. A special pre-treatment and low

temperature annealing must be applied because of the Al structures on layer 4. Oxygen plasma activation or rinsing in concentrated nitric acid can be used as well. The alignment for the pre-bonding can be done using an optical mark system (two-step-alignment) or, most easily, using mechanical alignment pins. After pressing the wafers into contact with a small force and annealing at 400°C for several hours, a bond strength of about 50% of high temperature strength is reached [8]. After bonding, a selective sputter process using a hard mask is applied to create the wire bond pads on layers 1, 2 and 3. Finally, the compound is diced into chips.
The FPI has been tested regarding electrical, mechanical and optical properties. A driving voltage has been applied to the fixed electrodes in order to deflect the movable mirror towards the fixed one during this measurement. The curves depicted within Fig. 4 (left) show a capacitance change between 2.91 pF ... 3.03 pF depending on the electrode location. The deflection (measured curve within Fig. 4 right) shows the corresponding displacement of the movable mirror towards layer 4.

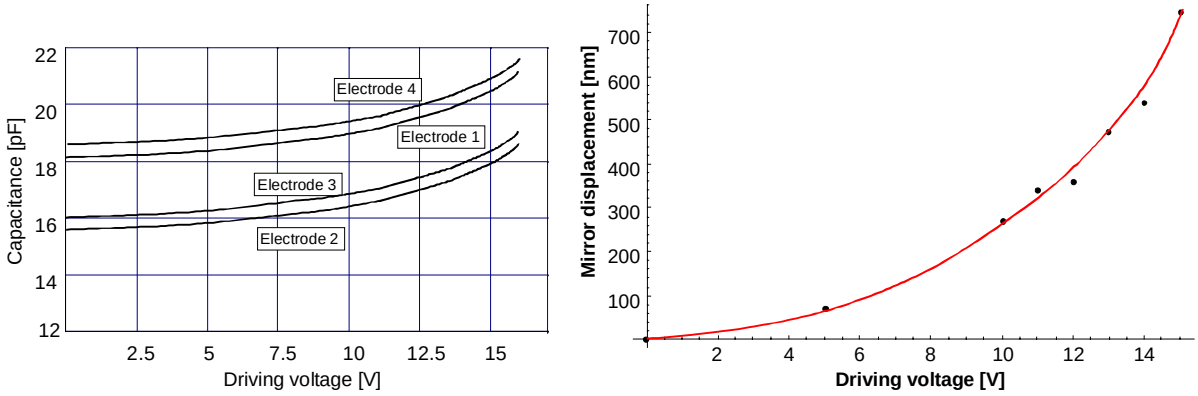


Fig. 4. Result of capacitance measurement of the four separate fixed electrodes and deflection applying voltage to the driving electrodes

Flatness measurements have been done by a customized phase shift interferometer. The flatness of the mirrors within the optically active area (2200 µm x 2200 µm) of the FPI has been measured to be better than ± 7 nm (Fig. 5 left). It is a total curvature of less than 0.5% in comparison to wavelength. The tilt due a possible asymmetric electrostatic force while tuning has been measured by subtracting the topology of the movable mirror from the topology of the mirror in rest. The result depicted in Fig. 5 (right) shows a difference in height of about 15 nm over the optical active region.

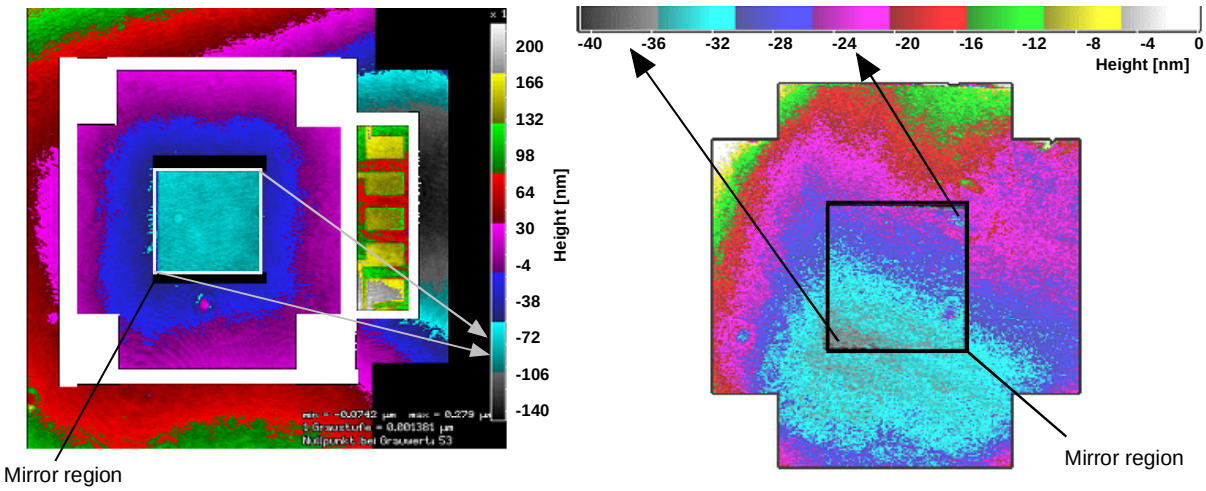


Fig. 5. Result of topography measurement by a phase shift interferometer, without deflection (left) and deviation from straight vertical translation (right)

First samples have been tested regarding transmission behavior. They consist of layer 4 and layer 3 and two quarter wavelength stacks only. The FWHM is about 100 nm with maximum transmission of 0.55 (Fig. 6). Because this version does not prevent the mirror tilt by the parallel spring suspension we assume a tilt between layer 3 and layer 4 is the reason for the relatively low transmission. Consequently the parallel spring suspension and an active tilt control are necessary.

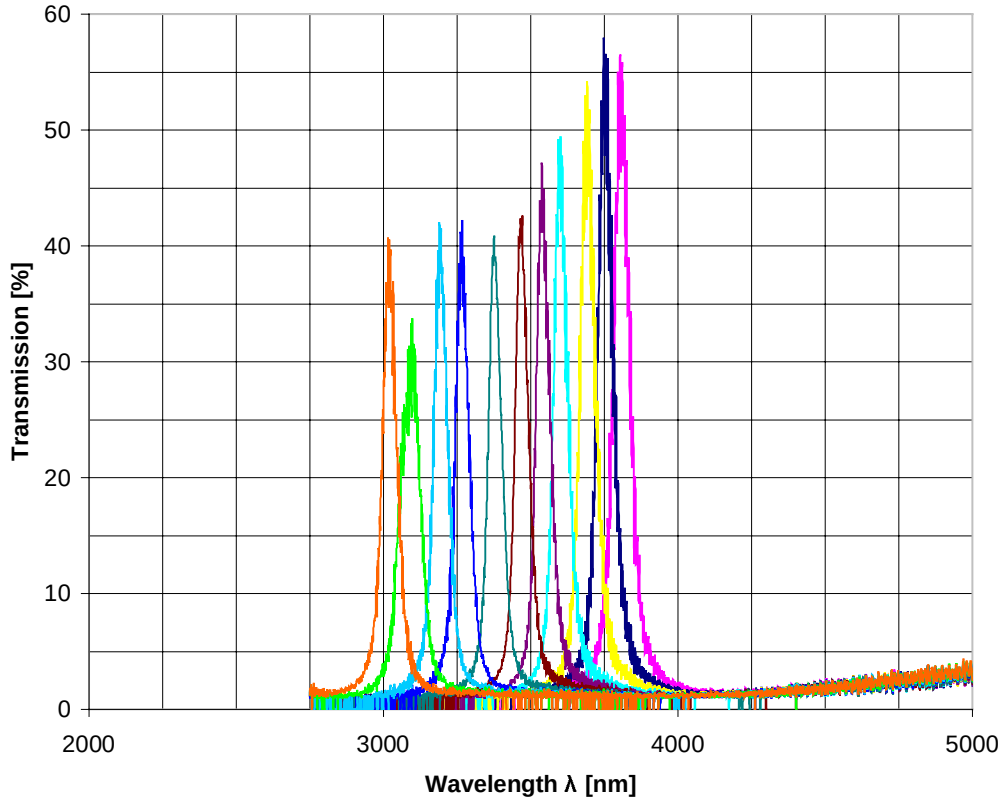


Fig. 6. Transmission at different driving voltages (from right to left: violet 0V, dark blue 5V, yellow 7V, light blue 9V, dark purple 10V, brown 11V, dark green 12V, blue 13V, light blue 13,5V, green 14V, orange 14,2V)

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