

# MEMS-Packaging

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A microsystem is defined as a miniaturised system. In particular also called 'intelligent' system it comprises several micro-components which integrate different individual functions into one completely optimised structure. This is achieved through the integration of electrical, mechanical, optical, chemical, biological, magnetic or other processes on a single chip or a hybrid circuit. Miniaturisation allows the reduction of both weight and volume and enables new functionalities. Due to this high degree of integration it is not possible to define a general package usable for all MEMS (see footnote: packaging definition). There is rather a large spectrum of different versions of packages. Essential requirements to the packages are:

- Protection against harsh environment
- Routing of different electrical potentials
- Hermetic sealing
- Screening of electrical and magnetic fields
- Heat dissipation
- Adapted thermal expansion coefficient
- Resistance against high operation temperature
- Minimization of mechanical stress
- Integration of electrical, mechanical, optical, chemical, biological, magnetic or other processes

A classification of MEMS packages can be done by distinguishing the integration degree on which the packages are realized (see Fig.1).

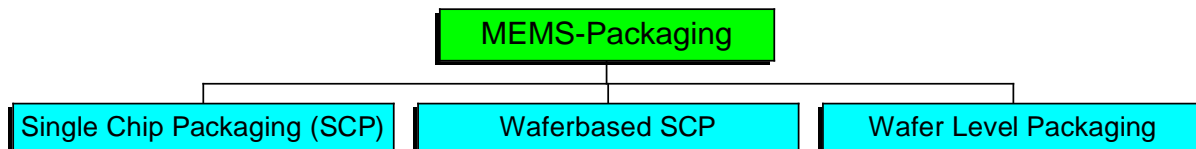


Fig 1. Classification of MEMS Packaging

The packaging method is named single chip packaging (SCP) if typical integrated circuit standard packages or modified standard packages like TO-packages, ceramic packages or pre-formed injection moulded packages are used for single MEMS chips. The sealing techniques (soldering, welding, clogging, shedding) for these packages are compatible with the technology steps used for packaging of microelectronic devices. The wafer-based chip scale package is a technique where single chip covers are mounted on pre-fabricated wafers for example with pick and place equipment resulting in a substrate which can be machined again on wafer level after the packaging of single chips.

A relatively new field of packaging activity is the wafer level packaging (WLP) dealing with the integration of electrical, mechanical or also other components on wafer level. Presently there are manifold solutions of MEMS devices where the MEMS component is connected with an external electronic component. Usually ASIC's with an especially adapted electronic module are used for the fabrication of such systems. But the manual fabrication outlay for the assembly of such MEMS systems is unjustifiable high in consideration of an increasing miniaturization and a high volume production. Additional substrate carriers and bus or redistribution systems reduce also the reliability of the whole system. Therefore the development of concepts for an automatic continuous processing of the pre-fabricated devices and an optimisation of the packaging technologies concerning a high volume production - if possible on wafer level - is necessary in near future.

Suitable bonding and conducting techniques on wafer level connecting the bonded wafer electrically will contribute to fabricate innovative solutions. Two possible solutions for mounting of micromechanical and microelectrical components are demonstrated in figure 2 and 3.

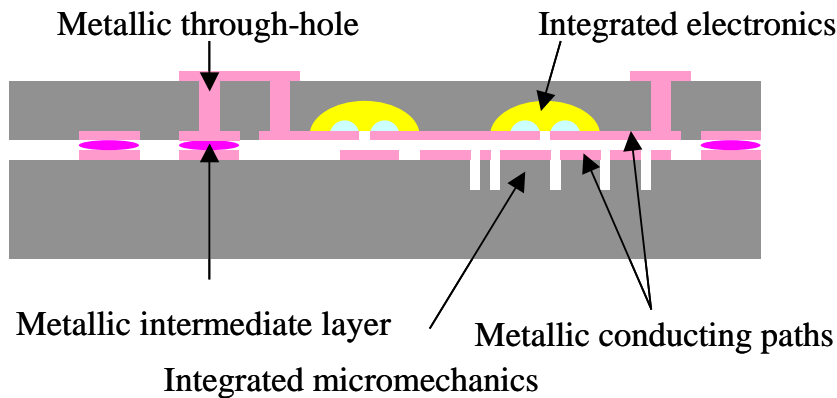


Fig. 2: Mounting concept for micromechanical and microelectrical components by metallic interlayers

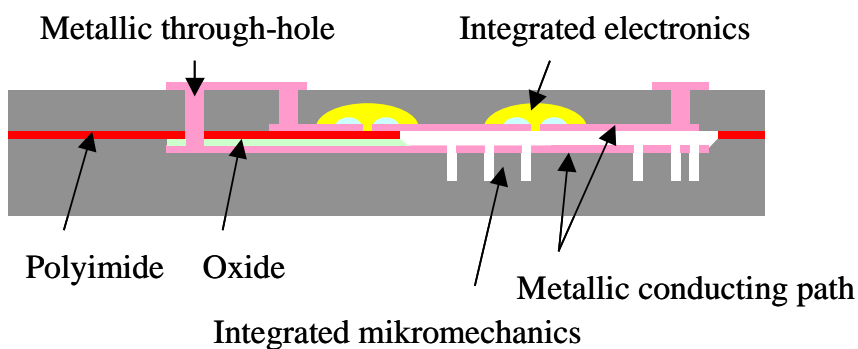


Fig. 3: Mounting concept for micromechanical and microelectrical components by interlayers made of polyimide

The term ‘wafer bonding’ comprises all bonding techniques suitable for the contacting of at least two wafers with or without an intermediate layer. The most common techniques are the silicon direct bonding [1], anodic bonding [1], eutectic bonding [2], glass-frit bonding [3] and adhesive bonding. The following overview (fig. 4) will serve to classify the different techniques. Both the creation of electrical contacts between the mechanical, optical, electrical and fluidic components and the creation of interfaces to the outside contacts are of vital importance if the MEMS is meant to function properly.

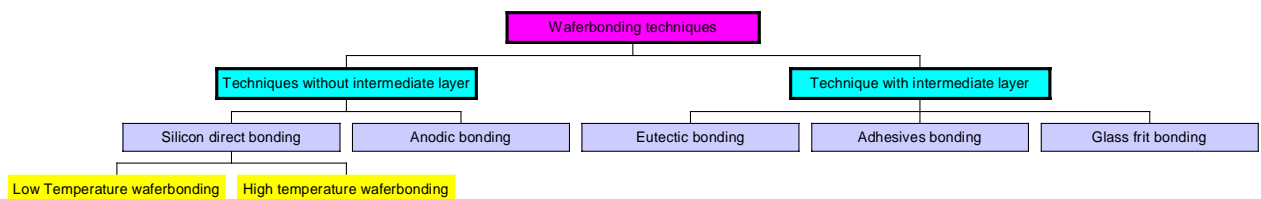


Figure 4: Overview to wafer bonding techniques

Depending on the manufacturing technology used for the individual components (e.g. bulk or surface micro-machining for micro-mechanical components) one of a wide range of different contacting systems needs to be applied. The most important requirements for these contacting techniques are:

- the electric potential inside the component has to be conducted outside
- low levels of ohmic transition impedance need to be realised
- parasitic capacities and inductances must be avoided
- the hermeticity of the component must not be compromised
- high levels of long-term stability should be ensured

The contacting of micro-mechanical components often requires the use of electric feed-throughs via the bonding locations, generally created by wafer bonding, or electric through-platings through the upper or lower sealing elements of the micro-mechanical component. Technology versions are the machining of the wafers by ultrasonic- or laser beam drilling or by RIE (reactive ion etching). Electric contacts can be established by filling the drilled holes with conductive adhesive or by metallizing the interior walls of the holes with either PVD or galvanic processes. Due to the different thermal expansion coefficients of the materials involved, this technique struggles to create hermetically sealed bonds across a wide range of temperatures. If wafer bonding techniques featuring intermediate layers are used, the conducting paths will be embedded into these intermediate layers, creating hermetically sealed contacts. The Figures 5 and 6 show electric feed-throughs which have been conducted through an intermediate connecting layer applied through screen-printing. The bonding partners had been connected to each other through glass-frit bonding.

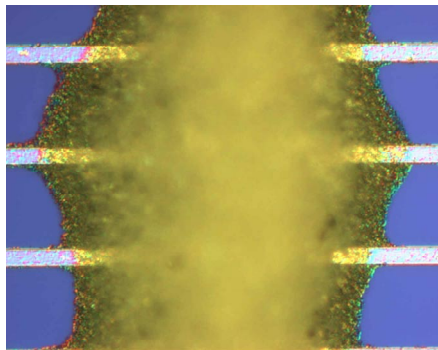
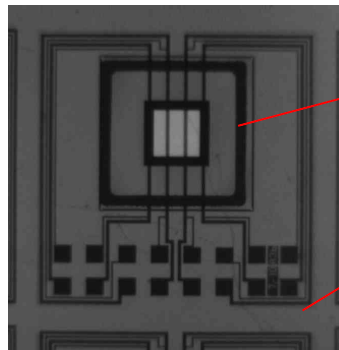


Figure 5: Glass paste printed over conducting paths



Printed bond frame, made of glass paste

Capped MEMS device by glass frit bonding

Figure 6: IR transmission images of a wafer bonded micromechanical device with electric feed troughs, bonded with use of a printed glass frit paste

## References

- /1/ A. Plößl und G. Kräuter, Wafer direct bonding, Tailoring adhesion between brittle materials, Materials Science and Engineering R: Reports, 1999
- /2/ Jie Yang, H. Kahn, S. M. Philips, A. H. Heuer, Experiment of 4 inch wafers Au-Si eutectic bonding, Fifth Int. Symp. on Semicond. Wafer Bonding: Science, Technol. and Applications V, 1999, meeting abstracts Vol. 997, Honolulu, Hawaii, im Druck.
- /3/ K. Sooriakumar, David J. Monk, Wendy Chan u.a., Fabrication of media isolated absolute pressure sensor, Electrochemical Society Proceedings, Volume 95-27, p.231-237
- /4/ Entwicklung einer Waferverbindungstechnik für vertikal integrierte IC's, C. Landesberger, A. Klumpp, P. Ramm, Proc. Symp. SMT/ES&S/Hybrid (1997), Proc.European workshop materials for advanced Metallisation, p. 94 (1997)

## Packaging-Definition:

The package that the microsystem or device is finally mounted in has to perform many functions. It will enable the user of the device to handle it, and incorporate it into his/her own design. It will allow the attachment of electrical connections, fluid ports, fibre optics, etc, with minimum interference from stray signals, or noise in the environment. It may also need to protect the device in harsh environments, preventing it from mechanical damage, chemical attack, or high temperatures. In many cases when considering electronic devices, the package must also prevent light falling on the device, since the generation of charge carriers by photoelectric effects will appear as noise. In the case of light sensors, however, the package may be designed to concentrate light in a particular spot. (Source: Danny Banks at the University of Surrey)