Solar cell processing steps applied on RIE textured silicon surfaces

K. Erler, A. Mrwa, K. H. Diefenbach, S. Denissov, T. Werner, G. Ebest

1. Introduction

Silicon solar cells require a surface texturisation to attain improved conversion efficiencies. Surface textures diminish reflection losses and cause an oblique coupling of light into silicon. The number of generated minority charge carriers increases, less of them recombine en route to the pn-junction and hence the cells current is enhanced.

Alkaline solutions exposing crystallographic (111) planes are usually used for the production of inverted pyramid textures in monocrystalline (100) silicon. In respect of multicrystalline substrates these etches are less practicable for texturing due to the various crystallographic grain orientations. The application of etches based on HF-HNO_3 induces difficult reproducable results.

Mechanical texturing techniques require wafers with sufficient stability. These methods are not applicable specially for thin, warped, and fragile materials, like EFG (edge defined film fed growth) silicon. However, the EFG wafer production is a cost effective and raw material saving technique. In comparison to Czochralski growth and ingot casting it avoids sawing losses and decreases the amount of required silicon feedstock in this way [1].

Reactive Ion Etching (RIE) based on chlorine or SF_6/O_2 was found to be an alternative texturing method for monocrystalline and multicrystalline silicon wafers. Since chlorine gas is toxic, the usage of SF_6/O_2 gas is more advisable.

RIE is a dry, contactless, and stress-free processing technique, suitable for manufacturing of nanometer scale texturisation. Under appropriate conditions a rough surface with low reflectance is formed [2, 3]. During the RIE process about (3...10) µm silicon are removed from the wafer. The number of recombination centres in the region nearby the surface is increased by the rough and enlarged surface, nonvolatile reaction products as well as damages in the crystal lattice caused by the bombardment of ions. Therefore the RIE surface texture has to be optimized to attain an improved conversion efficiency [4]. In [5] was reported, that by incorporating of improved cleaning and damage removal etch treatments, a nearly damage-free silicon surface is recovered without significant reflection losses.

RIE based on SF_6/O_2 gas was applied on EFG silicon wafers to investigate the usability of this texturing process. Following the plasma texturing typical cost effective solar cell processing steps were applied, accompanied with SEM (scanning electron microscopy) investigations as well as lifetime and optical measurements.

2. RIE texturing of EFG wafers

The texturisation was performed in a parallel plate reactor Alcatel GIR 220 (anodized aluminium). By modification of the process conditions different surface structures could be manufactured: Fig. 1 shows several typical textures produced with process times of 1, 10, or 15 minutes. After applying RIE for 1 minute the surface texture consists rarely of peaks. It is characterized by joined risings.

A process time of 10 minutes led to distinct peaks, possessing irregular altitudes and distances. Application of 15 minutes RIE and etching of roughly 7 µm silicon enlarged their scale.

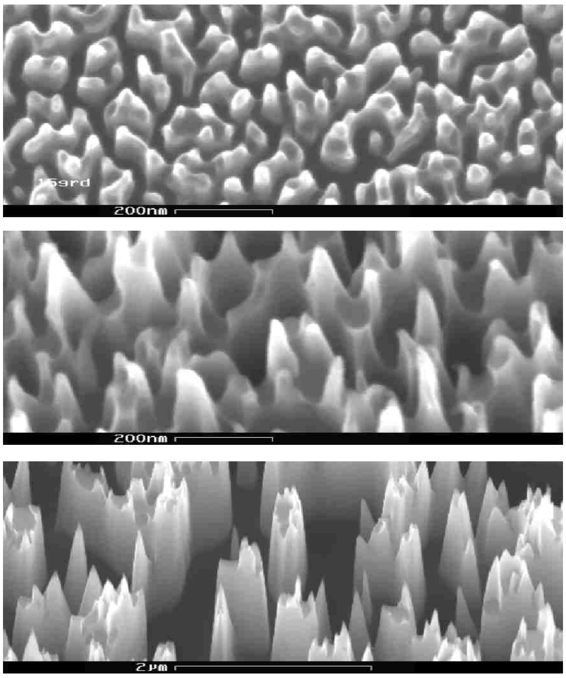

Figure 1: SEM pictures of microstructures after applying 1, 10, or 15 minutes reactive ion etching (from top to bottom with increasing process time)

3. Reflectance of textured surfaces

Spectral reflectance measurements were carried out by means of an adjusted Bruker IFS/66 spectrometer in combination with a xenon light source and an Ulbricht sphere (Optosol). This device allows measurements of the hemispherical (total) reflection as well of its diffuse fraction. The direct reflection is simply the difference of both. Partly the measurements were performed parallel and perpendicular to the wafers growth direction, respectively.

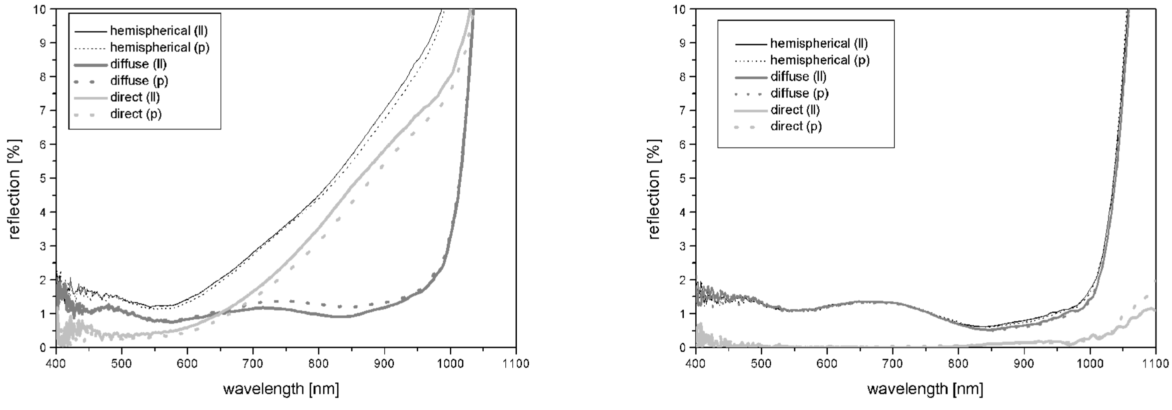

Figure 2: Reflectance of an EFG-wafer after RIE with process times of 1 minute (left) and 10 minutes (right), leading to textures as represented in Fig. 1-top and middle, respectively (|| -parallel / p-perpendicular to growth direction)

In the wavelength range (400...1100) nm untreated EFG-wafers have a mean value of hemispherical reflectance as high as 35 %, consisting of 5 % diffuse and 30 % direct reflected light. The reflectance of RIE-textured EFG-surfaces depends on the process conditions, especially the duration of the plasma process plays an important role. The reflection coefficient after RIE with a process time of 1 minute (Fig2 left) is still increased in comparison to 10 minutes processing (Fig.2 right). The differences of the direct reflection components are remarkable in the near infrared wavelength range (700...1000) nm:

4. Application of solar cell processing steps

4.1 Spin-on doping

The phosphosilicate glass layer was fabricated by means of dynamic spin-on doping technology. After 15 minutes prebake at 200°C the surface was investigated by means of a SEM (see Fig.3).

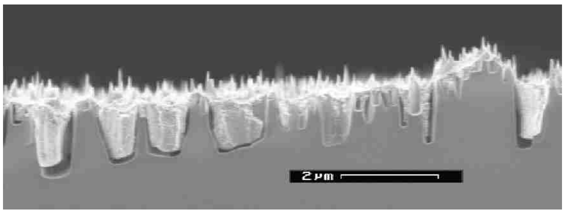

Figure 3: SEM picture of phosphosilicate glass after spin-on dopant deposition on a RIE textured EFG substrate

The phosphosilicate glass covers the wafer surface and is able to fill spaces between narrow peaks, beside hollows with high aspect ratios. During the prebake the phosphosilicate glass shrinks due to the evaporation of solvents.

4.2 Diffusion

The diffusion process was carried out by means of RTP (Rapid Thermal Processing) in a gas flow consisting of 90% nitrogen and 10% oxygen using a process temperature of 875°C. This process step was applied to 10 strongly textured EFG silicon wafers corresponding to Fig.1-bottom and, for comparison purposes, to 4 nontextured EFG wafers. After diffusion the phosphosilicate glass was stripped off by wet-chemical etching in hydrofluoric acid.
MWPCD (microwave photoconductance decay) measurements before and after RTP reveal that the effective minority charge carrier lifetimes increase for both, textured and nontextured wafers. The increase is spread over (5...110)% for the textured and (37...97)% for the non-textured wafers. Obviously this effect is caused by phosphorus gettering.

4.3 Passivation / Annealing

To get an adequate open-circuit voltage a sufficient passivation of the surface is necessary. After phosphorus diffusion textured samples were coated with silicon nitride (SiN_x) by means of plasma enhanced chemical vapour deposition (PECVD) at 350°C. The layer thickness corresponded to 80 nm on a planar surface.
The fabrication process of solar cells is completed by firing through the screen printed metallisation paste. Since the annealing step influences the density of the silicon nitride layer and therefore its reflection behaviour several samples with different texturisations were annealed in nitrogen atmosphere. In Fig. 4, left an example for the effects of a SiN_x coating on a less textured wafer solely as well as annealed in nitrogen atmosphere is represented. For defect removal purposes the sample was additionally isotropic etched in SF_6-plasma. The above mentioned process steps affect predominantly the direct reflection. After SiN_x coating the direct fraction of reflectance was increased in the range (530...930) nm where the

hemispherical reflectance reached partly values above 10%. Annealing changed the optical properties of the coating and a decrease of the reflectance below 4% could be observed.
Medium textured surfaces show another behaviour (see Fig. 4, right). After deposition of SiN_x the reflectance is reduced, especially in the near infrared range. Annealing causes an additional improvement.

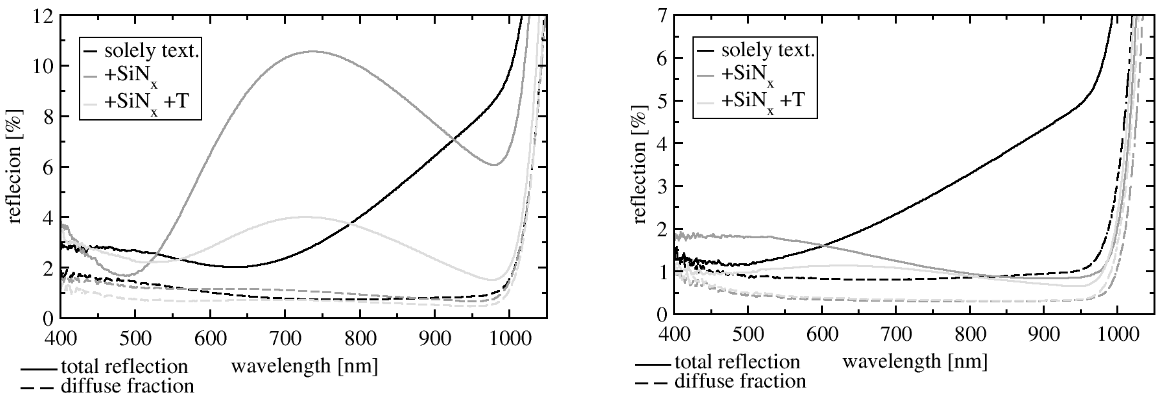

Figure 4: Reflectance of RIE-textured surfaces with less and medium texturisation (left- 1 minute process time, right- 3 minutes process time), additional SiN_x coating (+SiN_x) and annealing (+SiN_x+T)

Strongly textured surfaces (like Fig. 1- bottom) on the other hand change their reflectance scarcely after the deposition of the SiN_x layer and annealing.

5. Conclusions

RIE is a useful tool to achieve a texturisation of EFG silicon wafer surfaces. Even less textured surfaces reduce the hemispherical reflectance below 4% in the wavelength range (400...1000) nm. Their reflectance could be noticable reduced by applying further typical solar cell processing steps, like antireflection coating/ passivation and annealing.

6. Acknowledgements

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