Subproject C5: "Development and characterisation of a high aspect ratio vertical FET sensor for motion detection"

- **Prof. Dr. Gunter Ebest**
- **Prof. Dr. Thomas Gessner**

Authors: A. Bertz, W. Bräuer, S. Buschnakowski, S. Heinz, R. Schuberth

Nowadays inertial sensors for car dynamics stabilization, acceleration detection, human body motion monitoring are popular MEMS applications. Additionally motion/position detection is often required for actuators too (xy stages, switches, etc.). At present these systems are usually based on piezoelectric or capacitive sensors. While especially the latter principle is already used for mass production of inertial sensors an increase of the signal/area consumption ratio is desired. That's why alternative approaches have been presented looking for a direct integration of mechanical and electronical principles [1,2].

A novel vertical field effect transistor for signal conversion from the mechanical to the electrical domain is manufactured. The channel resistance between drain and source is influenced by a movable gate working as a sensing unit.

The system consists of a laterally moving spring-mass-system (Fig. 1, Fig. 2). There are two arms at the seismic mass. Transistor regions are located at the end of the arms. The moving mass (silicon) is acting as a gate electrode. The air-gap between the channel and the gate electrode decreases/increases due to the deflection of the mass caused for example by the moment of inertia. A displacement of the mass changes the air gap of the vertical FET influencing the capacitance of the gate insulator. The capacitance of the gate insulator can be expressed as a series connection of the air-gap capacitor with the oxide capacitor. In addition to the vertical FET signal the movement is also detected capacitively by comb electrodes at both sides of the seismic mass for comparison. Further comb electrodes are used to control the working range. Thus a variable electrostatic force decreases/increases the gap between the channel and the mass (gate).

To find out the relationship between the geometric dimension and the sensitivity of the structure, the performance of the sensing element is simulated using a process and device simulator. An analytical model is used to evaluate the dimensionally optimised arrangement between the transistor and the spring-mass-system in order to design a vertical FET with maximum sensitivity. The simulator data are compared with measurement results from fabricated sensors.

A high aspect ratio technology (Fig. 3) represents the base technology for the fabrication of the sensor structures. Using a five mask process, laterally movable structures with n-type and p-type doped layers are fabricated. The process flow will be presented later more in detail.

The output current of a fabricated vertical FET (non optimised) increased approximately from 0 nA to 30 nA by 8 µm gate deflection at a bias of V_{ds}= 1 V and V_{gs}= 5 V with a senor area of 90 µm x 10 µm. Exemplary the Fig. 4 and Fig. 5 illustrate the I-U-characteristics of the vertical FET.

A new issue of the vertical FET is the symbiosis of an active transistor device and a micromechanical structure forming a micro electro mechanical system (MEMS). Main advantage of the vertical FET is the higher signal-to-noise ratio with respect to capacitive sensor systems and therefore simplification of the signal conditioning circuitry. The measured results show that the signal per sensor area is about fifty times higher compared to capacitive sensors.

References:

[1] Weinert, A.; Berggren, M.; Andersson, G. I.: *A low impedance sensing technique for vibrating structures.* Transducers '99, Seddi, Japan, 1999.

[2] Smith, J. H. et al: *Intelligent Microsystem: Strategy for the Future*. Semiconductor International, Vol. 21, No. 4, April 1998, 93-98.

[3] Haronian, D.: *Direct Integration of solid state sensors with MEMS*, mstnews, Februar 1999.

[4] Haronian, D.:*A low cost micro-inertial and flow sensor based on the Direct Integration technology*. Advanced Micro-systems forAutomotive Applications 99, Springer Verlag, 1999.

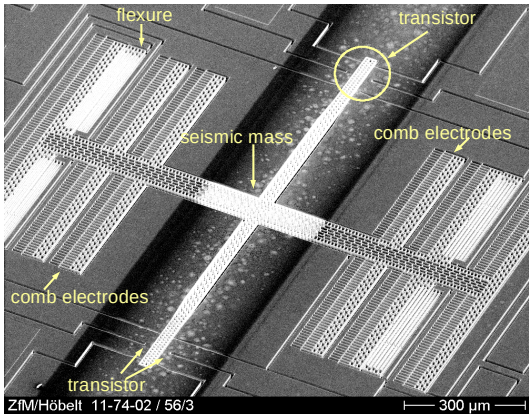

Fig. 1: SEM view of the vertical FET

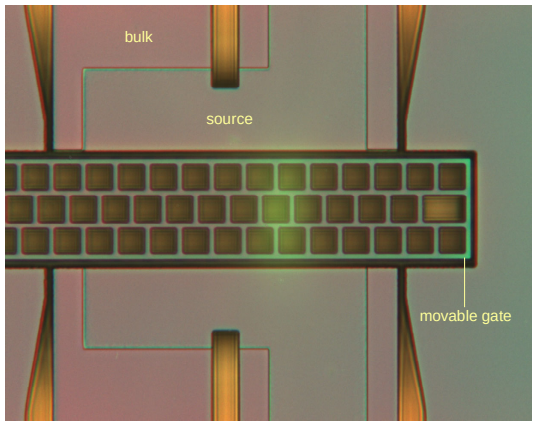

Fig. 2: Light-optical microscope view of the transistor

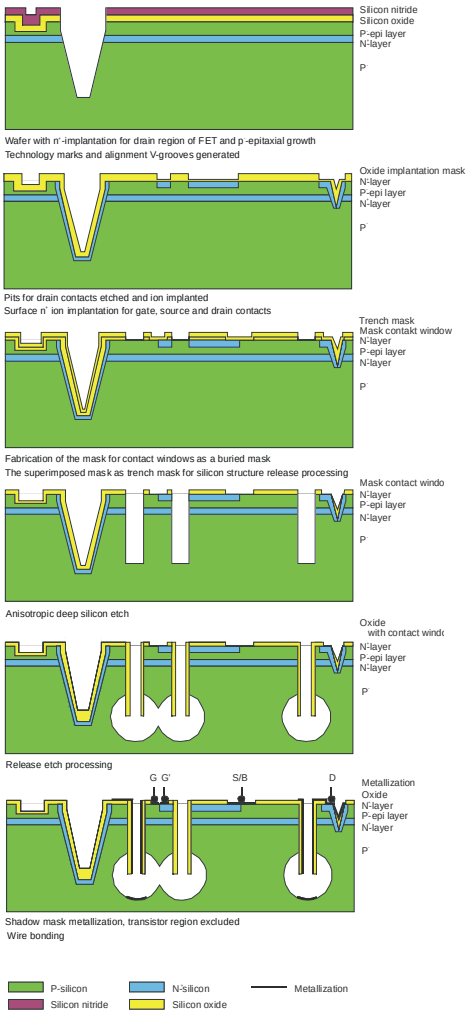

Fig. 3: Technology process flow

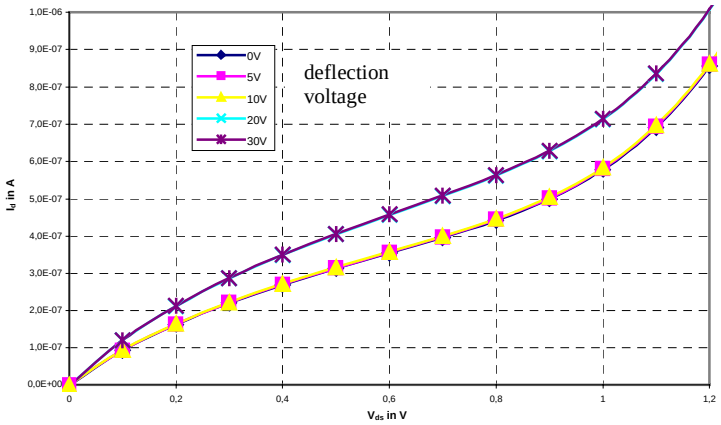

Fig. 4: I-U-characteristic depending on deflection voltage

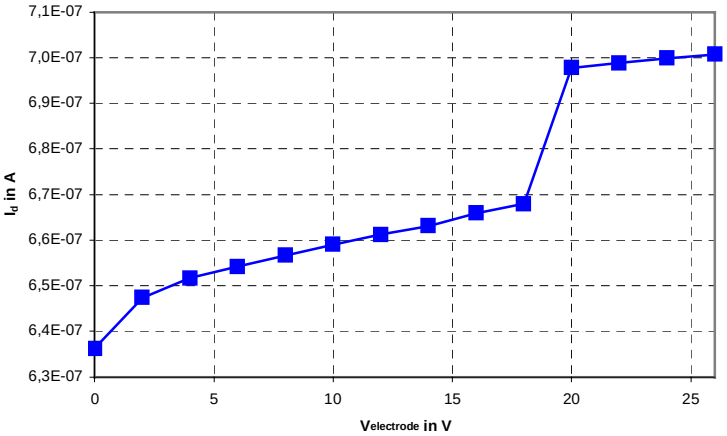

Fig. 5: Transfer characteristic at V_{ds}= 1 V