Development and characterisation of ultrathin CVD WN_x diffusion barriers for Copper metallization

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Diffusion barriers are fundamental elements in integrated circuits to prevent the interaction of copper interconnects and the dielectric as well as silicon. However, the continuously shrinking device dimensions in the future IC generations require a very thin and efficient barrier.
The technical basis to perform WN_x CVD is a tungsten CVD chamber at the commercial cluster tool PRECISION 5000 (Applied Materials), which provides the opportunity to integrate barrier and copper CVD. The plasma enhanced CVD using $WF_6/N_2/H_2$ gas mixture was chosen from a number of possible methods to produce tungsten nitride films. Nitrogen and hydrogen require high temperature to react in thermally excited process. Consequently, it is essential to use plasma enhancement to reduce the deposition temperature.
Three WN_x layers have been developed with different compositions (RBS and XPS investigations). The compositions result from the variation of the total gas flow and the ratio of the N_2 and H_2 flow to WF_6. In the as-deposited state the layers show no differences for the electrical resistivity (see table 1). They have also an amorphous like microstructure which impedes grains boundary diffusion and is a highly advantageous structure for barrier films (Fig. 4).

Table I: *Composition of WN_x barriers with gas flow parameters and N/W ratio and electrical resistivity*

	N_2/WF_6	H_2/WF_6	Total flow [sccm]	N/W	ρ [μΩcm]
WN_x1	80	80	520	0.24	205
WN_x2	110	50	520	0.28	220
WN_x3	80	80	2500	0.25	210

But after a heat treatment in vacuum the films show different crystallisation behavior, investigated with grazing incidence X-ray diffractometry (see Fig. 1-3). Annealing at 450°C/1h and 550°C/1h did not yield significant structural changes, whereas the 600°C/1h anneal resulted in a crystallisation of WN_x1 and WN_x2, indicated by the emergence of crystalline Bragg peaks corresponding to α-W and β-W_2N. Only minor distinctions occur in the diffraction patterns for WN_x1 and WN_x2. For films with the composition of WN_x1, the crystallisation proceeded during anneals at 600°C/4h and 600°C/16h, i.e. the crystalline peaks continued to grow at the expense of the amorphous socket. In the layer stacks with the WN_x2 barrier already after the 1 h anneal at 600°C no further crystallite nucleation/ growth could be inferred from the diffraction patterns.
The barrier films of WN_x3 composition showed crystalline Bragg peaks of α-W and β-W_2N at the amorphous hump not before 600°/4h. Both peaks are broad indicating a very small size of the crystallites. The retarded crystallisation results probably from more pronounced amorphous state because of the high total gas flow realized with a high Ar flow.
To give a realistic estimation about the thermal stability of a diffusion barrier on a dielectric it is necessary to prove small amounts of copper migrating into the SiO_2. With GI-XRD and cross sectional TEM no Cu diffusion was proved before and after the crystallisation of the amorphous WN_x films for all 3 compositions. As real device structures MIS capacitors with the barrier WN_x3 were prepared. After different annealing steps the structures have been examined to find electrical irregularities using HF-capacitance-voltage (HF-CV), capacitance-time (Ct) and triangular voltage sweep (TVS) measurements.

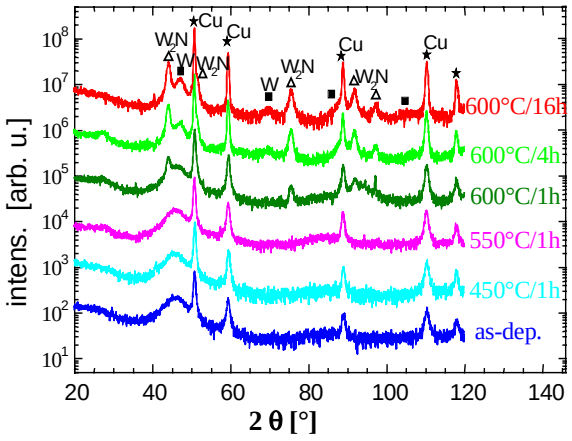

Fig 1: GI-XRD pattern of WN_x1 after annealing (Cu radiation)

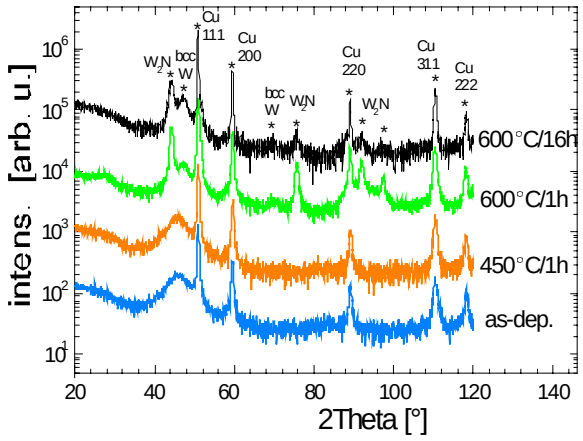

Fig 2: GI-XRD pattern of WN_x2 after annealing (Cu radiation)

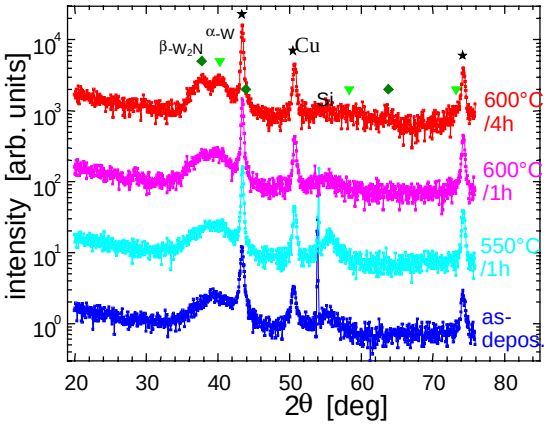

Fig 3: GI-XRD pattern of WN_x3 after annealing (Co radiation)

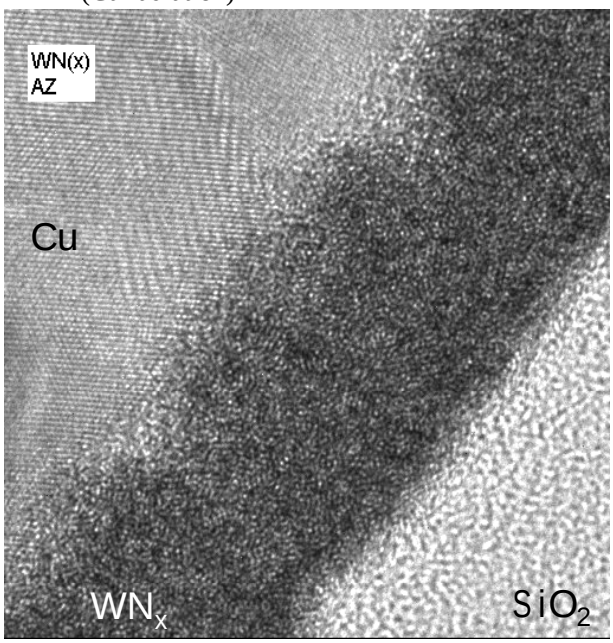

Fig 4: XTEM image from 10 nm WN_x3 in the as deposited state, amorphous structure

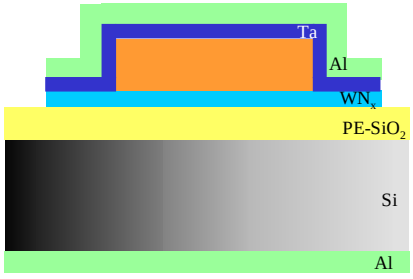

Fig. 5: MIS capacitor as test device

To prepare the MIS capacitors the WN_x3 films with 10 nm thickness were deposited on Si substrates with 100 nm PECVD oxide with TEOS as precursor. Afterwards a copper layer of 500 nm thickness was deposited in a PVD process, with a short vacuum break of 2 minutes. Then the copper and the barrier films were patterned and covered with a 40 nm PVD Ta film to suppress a possible surface diffusion of copper (see schematics in Fig. 5). The area of a capacitor structure was 1 mm^2. To provoke barrier failures at moderate times annealing steps up to 550 °C were performed in forming gas (95% Ar + 5% H_2) for the investigation of the capacitors . The MIS capacitors were annealed for 60 min and analyzed after every annealing step using HF-CV, Ct or TVS measurements to find changes in the electrical behavior. CV measurements on samples with copper on thermal SiO_2 *without barrier* show clear irregularities in the electrical behavior, see Figure 6. After the 350 °C annealing step the flatband voltage is shifted about +0.1 V, which could be a healing up effect caused by the hydrogen content in the forming gas. With annealing at elevated temperatures V_{FB} is shifted to lower voltages, with the total values –0.75 V after 500 °C and –1.15 V after 550 °C. The content of sodium was measured to be

$7 \cdot 10^9$ cm^{-2} and is therefore not able to produce the measured shift. With the oxide thickness of 100 nm and the assumption that copper is a monovalent acceptor the shifts in the flatband voltage of –0.75 V and –1.15 V give, subtracting the contribution of the sodium contents of $7 \cdot 10^9$ cm^{-2}, the copper shares of $1.4 \cdot 10^{11}$ cm^{-2} and $2.2 \cdot 10^{11}$ cm^{-2}, respectively. If the copper ions are two-valent the content decrease simultaneously. After the 550 °C annealing step the capacitors show a strong decrease in the oxide capacitance. This effect is assumed to be caused by a copper diffusion into the oxide layer. With these results the diffusion of copper into the SiO_2 at elevated temperatures is proved. The HF-CV measurement method shows a high sensitivity to ions in the insulator and a low detection limit for copper contents.

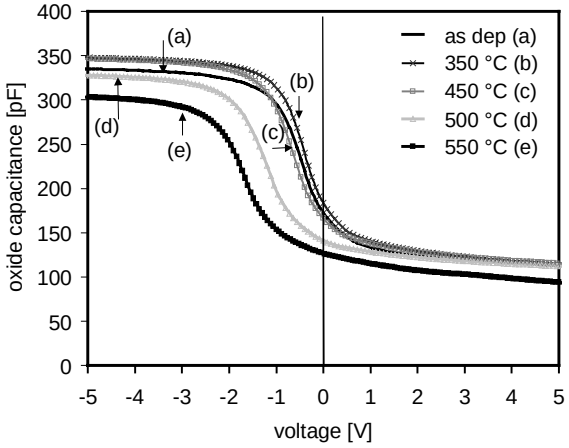

Fig 6: Part of CV-curves measured on capacitors with the film stack p-Si/thermal SiO_2/Cu

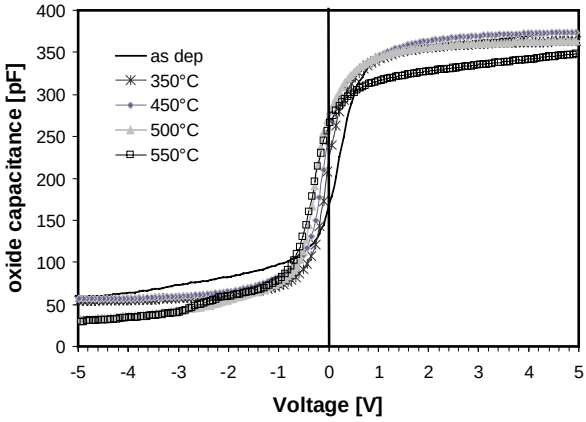

Fig 7: Part of CV-curves measured on capacitors with the film stack n-Si/PE-SiO_2/WN_x3/Cu

The same measurements on capacitors with the layer stack *100 nm PE-oxide/10 nm WN_x3/500 nm Cu* is shown in figure 7. After the 450 °C heat treatment a slight shift toward the negative site was observed. The amount of this shift has the same order of magnitude than the value for the reference samples with aluminium metallization. Therefore the shift is not explainable with a copper diffusion into the SiO_2. The sodium content in the samples is measured by TVS with a maximum value of $5.5 \cdot 10^9$ cm^{-2} and is as well not a reason for observed flatband voltage shifts. After the 500 °C annealing a clear decrease of V_{FB} was measured. The amount of –0.58 V lies one order of magnitude higher than the aluminium reference. Subtracting the contribution of the sodium contents of $5.5 \cdot 10^9$ cm^{-2}, the copper content after the 500°C annealing is $1.3 \cdot 10^{11}$ cm^{-2}. This value is nearly the same as the content for the diffusion without a barrier layer, which leads to the conclusion that the diffusion barrier failed after this heat treatment. The lowering of the capacitance after the 550 °C annealing step could result from the changes in the dielectric constant as a result of into the SiO_2 diffused copper or the geometry of the capacitor top electrode, which are caused by delamination effects of the contact area of the WN_x.
With WN_x3 a ultrathin barrier material is available, which is electrical conductive and thermal stable up to 600°C/1h. The layer structure is dense and amorphous, the highly desired microstructure without grain boundaries as fast copper diffusion paths. With analytical methods no significant diffusion of copper was detected. Using a combination of TVS, HF-CV and Ct measurements it is possible to analyse the complete MIS structure for copper diffusion. Despite a lot of reference layer stacks, not all effects were explainable and the definition of the barrier failure is difficult. The results of the electrical measurements of a MIS structure are more complicated to expound and interpret, than barrier test structures using pn- and Schottky diodes, which on the other hand have limited application relevance for most copper metallization.

The results presented were gained within the BMBF project “Ultrathin diffusion barriers” in collaboration with the partners AMD Saxony and Leibnitz-Institut für Festkörper- und Werkstoffforschung Dresden (see chapter 4.1).