Integration of SiO_2 Aerogel as ultra low k dielectric (ULK) into Copper Damascene Interconnects for RF Devices

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On-chip integration of passive devices like inductors, capacitors, resistors, transmission lines etc in the BEOL of advanced RF-CMOS, BiCMOS and Bipolar devices is becoming more and more attractive in order to reduce the total number of components which are required for wireless products like e.g. mobile phones. In order to minimise power consumption of the chips and to optimise the performance of passive devices, effective reduction of parasitic capacitances (e.g. parasitic coupling with the substrate or with surrounding metal lines, plates or pads) is a key challenge. Replacing standard SiO_2 by low-k or ULK dielectrics might be an attractive and effective approach to achieve the required reduction of parasitics.
In the performed feasibility study, an ultra low-k (ULK) mesoporous SiO_2 aerogel dielectric (SAGel, k=2.2) has been successfully integrated in selected levels of a Cu multilevel metallization of RF demonstrators. According to the ITRS-roadmap [1], a typical 90 nm CMOS technology will have a hierarchical architecture with at least four narrow spaced metal levels with minimum dimensions, at least two levels with moderate dimensions and at least one fat metal level with even larger lateral dimensions. Especially for RF applications, there might even be more than one level with such relaxed feature sizes, which house passive components like inductors. As our study is finally evaluating the impact of ULK integration on inductor performance, we used an architecture with relaxed geometries typical for such upper levels, although they are called metal 1 and metal 2 in this report, respectively. As a model demonstrator, a 2 LM Cu damascene metallization with a 20 nH spiral inductor in the top level (M2) is used.

Ultra low k (ULK) Dielectric – Deposition Process and Properties

SiO_2-Aerogel (SAGel) is derived from a conventional sol-gel-process starting from the precursor TEOS (Tetraethylorthosilicate) mixed with solvent, water and catalyst. The mixture is spun on the wafer and dried after gelation at normal pressure. On this way, silica films with high porosity (~50%) and mean pore radius of 3.4nm are obtained. The process flow and the properties have been already described in detail in former publications [2, 3]. Some selected properties of SAGel are summarised in Table I.

Table I. Properties of SAGel films

Dielectric constant	2.0 - 2.2
Leakage current density in A/cm²	2E-10 (@1 MV/cm)
Field breakdown voltage	3 MV/cm
Thermal stability	> 400 °C
Youngs Modulus	1.5-3.5 GPa (Berkovich, 0.1 mN)
Film Stress	60 MPa
Thermal Conductivity W/mK	0.14 ± 0.02

ULK Integration scheme

Several RF demonstrator groups with dielectric substitution in different levels were prepared. The ULK dielectric SAGel was applied to M1 and M2 level. Partially the via level V1 was additionally substituted by Black Diamond™ (BD, Applied Materials) with a k-value of 3.0. The motivation for BD instead of SAGel in the via level was the challenging preparation of SAGel films thicker than 800 nm. The architecture and the cross-section scheme of the various demonstrators D1, D2, D3 is schematically shown in Figure 1. A demonstrator with same structure and silicon dioxide as dielectric in each level was prepared as reference.
Several integration issues like ULK adhesion and patterning, resist stripping and metal CMP have been successfully addressed and corresponding process optimisations were achieved. Compared to integration in SiO_2, some process steps needed severe optimisations, others (like cleaning and H_2-based strip) had to be developed new as indicated in Table II. The development of an Ar plasma pre-treatment of the ULK surface [4], a double hardmask approach, a mild H_2/N_2 stripping process and a metal CMP process with reduced downforce have been essential. Successful integration of the advanced ULK dielectric is shown by SEM investigations and by electrical evaluation of line and via resistances and leakage currents. The DC parameters compare well with a corresponding Cu/SiO_2 reference. The impact of ULK integration in selected levels of a 20 nH RF inductor was investigated and an improvement of the quality factor Q by approx. 10 % and an increase of the resonant frequency by approx. 20 % have been found after replacing SiO_2 by ULK in one metal level beneath the inductor.

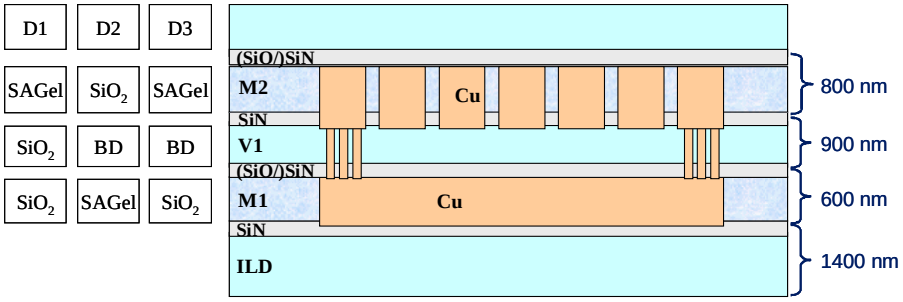

Figure 1. Architecture and cross-section scheme of the RF demonstrators (inductor windings located in M2 level).

Table II. Process flow for SAGel integration indicating optimised and new process steps compared to SiO_2 integration

Process flow	unchanged	optimised	new
Oxygen plasma treatment			x
Spin on (SAGel deposition)			x
Ar-plasma treatment			x
Cap layer deposition			x
Lithography	x		
Etch hard mask 2		x	
H_2 resist strip			x
Etch hard mask 1 / SAGel / barrier SiN		x	
Barrier deposition	x		
Metal deposition	x		
CMP		x	

Patterning

For patterning SAGel, a dual hard mask concept was followed [5, 6]. A silicon nitride cap layer (HM1) and a SiO_2 layer (HM2) were deposited on the ULK dielectric film (see **Figure 2**). By stopping etching right at the SiO_2/SiN (HM2/HM1) interface, the SAGel was protected during photoresist stripping. Opening of HM1 and etching of SAGel is continued by a process not impacting the ULK using CF_4/Ar chemistry . All etch processes were performed on a PLASMALAB 100 tool (Oxford Instruments), using ICP and RIE processes in combination.

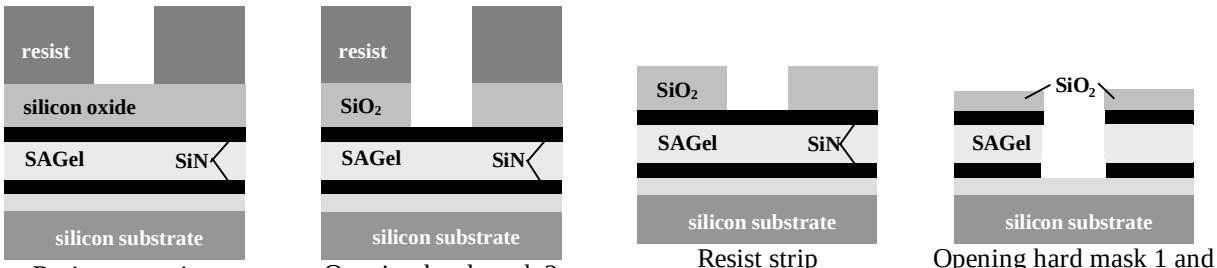

Figure 2. Hard mask concept for patterning porous SAGel

Copper and barrier CMP on ULK dielectric

The main focus when integrating a brittle ULK material with low elastic modulus, reduced mechanical stability and weak adhesion is to develop a CMP process with reduced polishing pressure without loss in removal rate. A two step CMP process was chosen using commercial slurries (Cabot) containing H_2O_2 as well as SiO_2 and Al_2O_3 abrasives for Cu and Ta(N) CMP, respectively, followed by a post CMP clean. Based on the process of record for Cu/SiO_2, a Cu-CMP process was developed with lower downforce in order to reduce the friction force between polishing pad and wafer. Combining a decrease of the H_2O_2 concentration in the polishing slurry with a optimisation of the other CMP parameters, a polishing process using downforces ≤ 2 psi with acceptable rate and reliable stop on the Ta-barrier was developed. In combination with an advanced method for endpoint detection required for such low downforces (based on light absorption, independent of friction force), an SAGel compatible copper polishing process was made available. The Ta(N) CMP process was also optimised by reducing the downforce to a level equivalent to the newly developed Cu CMP process and by optimising the H_2O_2 concentration in order to end up with acceptable polishing times and to compensate most of the Cu line dishing, which occurred during Cu CMP. Finally, a CMP process resulted with dishing comparable to Cu/SiO_2

damascene technology and good selectivity towards the cap layer (Figure 3), which did not promote adhesion issues. Figure 4 shows an example of the finally prepared two metal level demonstrators with the inductor, which is always in M2 level, perfectly integrated in SAGel ULK dielectric.

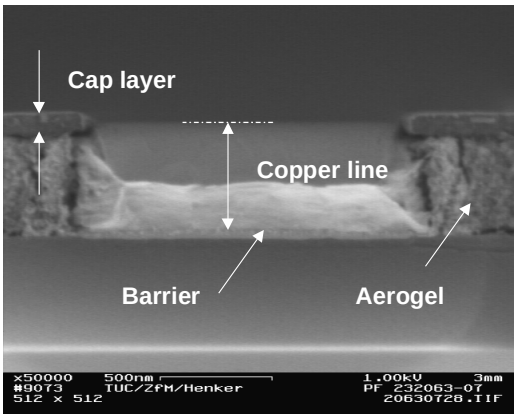

Figure 3. Single copper line after Cu and Ta/TaN CMP

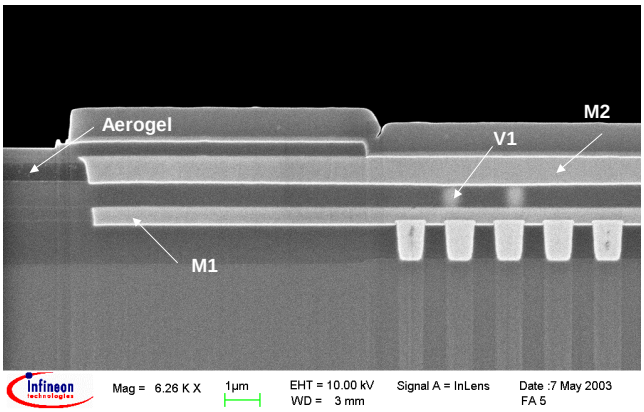

Figure 4. FIB image of 2-metal layer demonstrator. Detail: M2 in SAGel and Al-pad

DC characterisation

All demonstrator lots D1, D2, and D3 were characterised with standard DC measurements to verify the feasibility of our integration approach and to assess the metallization with respect to opens, shorts, leakage or other defects in comparison with a Cu/SiO_2 reference. Figure 5 shows the box plots for resistances of M1 meanders (30 mm length) with 1 µm width and spacing for the three different ULK samples in comparison with the reference. Except for the D1 sample, the line resistance and the spread are comparable to the reference, indicating that the target thickness of 600 nm was hit with acceptable uniformity. No low or high flyers have been detected indicating a low defect density comparable to the reference. Sample D1 shows a significantly larger spread. This is due to the fact that this sample group was prepared using oxygen containing etch and strip chemistry, leading to the larger spread of line resistances and also a somewhat higher defectivity. The leakage of metal 1 comb/meander structures (1.0 µm width and spacing, 30 mm long) is shown in Figure 6. All sample groups including the one with SAGel in metal 1 level (D2) exhibit leakage values below 0.01 nA. Also the spread of data is acceptable.

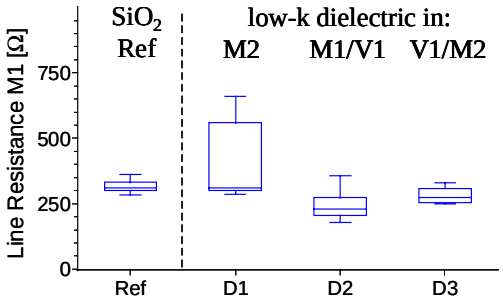

Figure 5. Metal 1 line resistances for meander structures with 1.0 µm width and spacing.

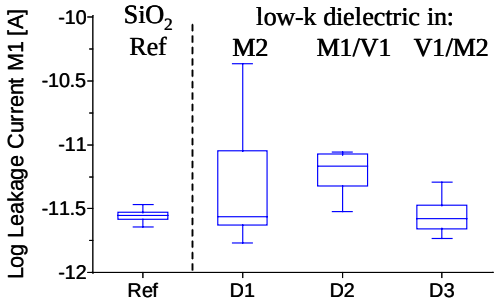

Figure 6. Leakage current of a 30 mm comb/ meander structure with 1.0 µm width and spacing at metal 1 level.

In summary we conclude from the DC measurements for all sample groups with SAGel and Black Diamond™ full electrical functionality in all levels with resistance and leakage data which are close to the expected values and which compare well with the SiO_2 reference.

RF assessment

The results of the performed RF assessment of the demonstrators are exemplarily shown for the impact of dielectric substitution for the variant D2. As a measure for the impact of low-k material on the performance of inductors we used the Q-factor. A common definition of the Q-factor is given in Eq. 1, where Z is the impedance. Typically a plot of the Q-factor vs. the frequency can be divided into two parts. At frequencies below the maximum of the Q-factor (Q_{max}) the Q-factor rises linear with a certain slope which is mainly determined by the DC resistance of the inductor. At frequencies above Q_{max} the Q-factor decreases due to high frequency losses caused by parasitic capacities, eddy currents and the skin effect. At the resonant frequency (Q=0) parasitic capacities dominate the Q-factor. This frequency typically limits the frequency range of applications for the

inductor. In the frequency range above f(Q_{max}) we expect benefits of low-k materials concerning the Q-factor and the resonant frequency since the parasitic capacitance is reduced with reduced k-values.

$$Q = \frac{\mathrm{Im}\{Z_{11}\}}{\mathrm{Re}\{Z_{11}\}} \quad (1)$$

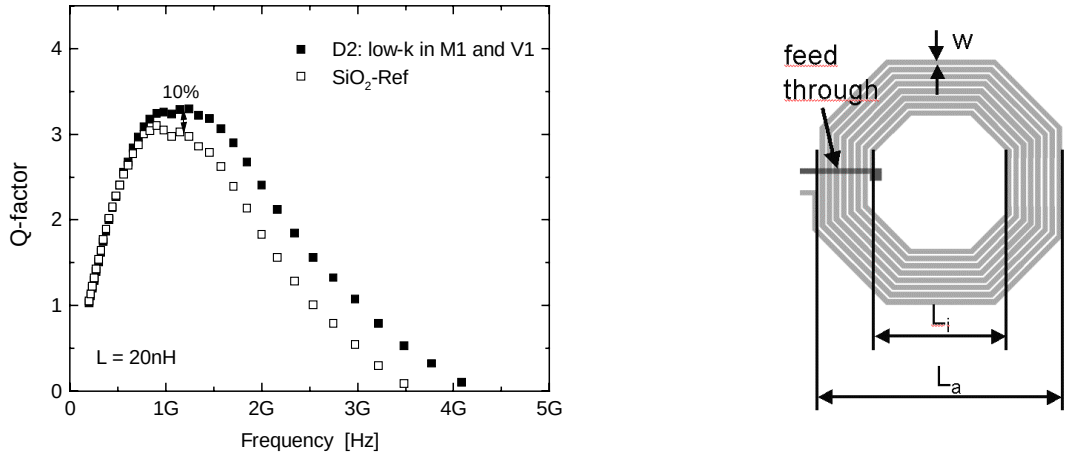

Figure 7. Measurement of Q-factor vs. frequency for a 20nH inductor (type D2) and the corresponding inductor scheme with inner diameter L_i, outer diameter L_a and line width w.

The influence of low-k material in metal 1 and via 1 level on the inductor performance is presented in **Figure 7**. The maximum Q-factor of the SiO_2 reference demonstrator is about 3.0. This value is reached at about 1 GHz. Selected substitution of SiO_2 by low-k materials leads to an improvement of about 10% for Q_{max}. The resonant frequency shifts from 3.5 GHz to 4.3 GHz, which is an improvement of about 20%. The slope of the Q-factor at low frequencies is the same for both demonstrators. This indicates that both demonstrators have the same metal thickness. This is essential to make sure, that only the change in k-value is responsible for the improvement of the Q-factor.

Conclusion

Porous SAGel has been successfully integrated into RF devices at different metal levels by modifying the process flow and carefully optimising the ULK related processes like deposition, patterning and metal CMP. The physical and DC assessment showed no negative impact of ULK integration on relevant interconnect parameters and fully functional two level metallization was achieved by introducing porous ULK material in selected metal levels. An improvement of the Q-factor and an increase of the resonant frequency by substituting SiO_2 with ULK has been demonstrated for one typical representative. ULK dielectrics will be preferably integrated in the lower, densely packed levels of future advanced multilevel metallization in order to improve RC characteristics. Thus, RF properties of inductors integrated in the top level will immediately benefit due to reduced parasitic substrate coupling associated with ULK integration. The total impact of replacing SiO_2 with ULK in all relevant levels for various inductor layouts on quality and resonant frequency will be determined with the support of simulations based on these first experimental results and will be published in the near future.

Acknowledgement

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