Device Characterisation for high-voltage circuits

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Introduction

The characterisation and modelling of integrated electronic devices are important topics in the research activities of the working group „Microsystem Electronics“ at the professorship of electronic devices (LEB).

High value polysilicon resistors take over several functions in integrated high-voltage circuits, e.g. voltage dividers. Two important features are electrical strength and proper functioning at maximum occurring power dissipation. These demands exist beside high linearity and small size. Because of parasitic elements, additional AC properties interact the circuit function.

Polysilicon resistors become valuable for special applications but their temperature and voltage dependence have to be considered. Matching techniques with common centroid layout and dummy structures are used to minimize the tolerance gap [1]. These dummies have no electrical purpose but legalize differences in etching rates of the polysilicon. Larger openings grant more access to the etchant. Therefore, outer devices get a greater degree during etching.

Electrical behaviour

The resistors are devices of a silicon on insulator (SOI) technology. Therefore, the tub underneath the resistors is insulated by oxide and an individual substrate voltage can be set per resistor. Fig. 1 shows a schematic device cross section. The p-doped poly-Si has a sheet resistance of 11 kΩ/sqr. All samples were fabricated by alpha microelectronics gmbh Frankfurt/Oder.

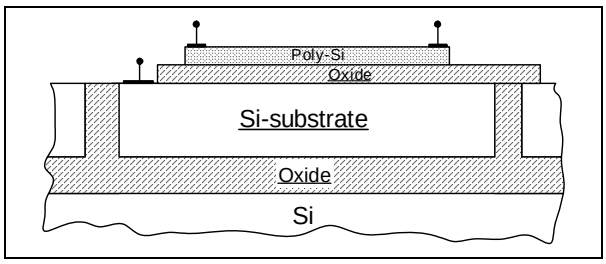

Fig. 1: Cross section of the poly-Si resistor

The DC characteristics of the high-ohm resistors were measured by a HP4062UX parameter test system. Its maximum applicable voltage with two source-monitor-units (SMUs) in series is 400 V. The temperature was varied from -40 °C up to +180 °C. Continuous measurements were compared with pulsed measurements. Both methods gave identical results, so self-heating is negligible.

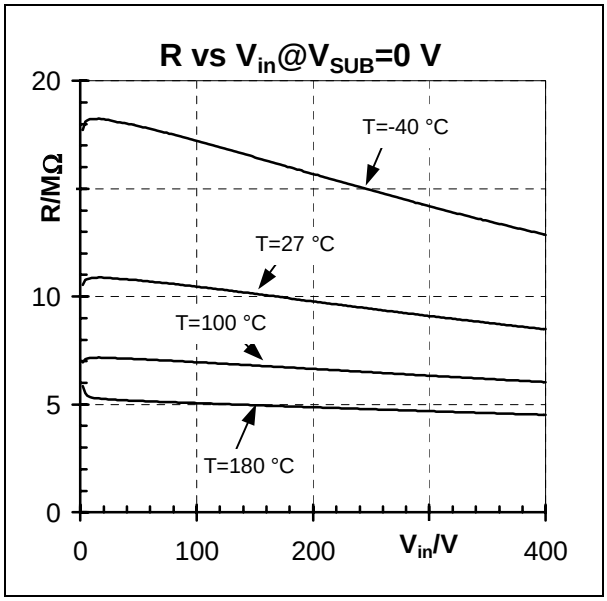

Fig. 2: DC behaviour at different temperatures

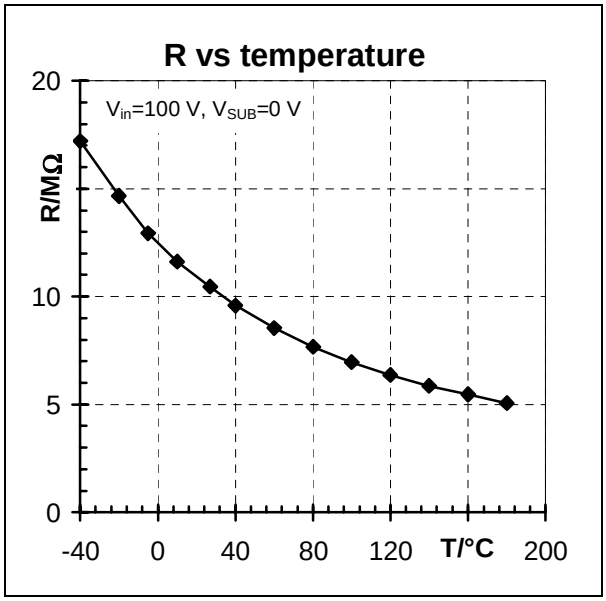

Fig. 3: Temperature behaviour of a 10 MΩ poly-Si resistor

Fig. 2 shows the DC behaviour of a 10 MΩ poly-Si resistor. The absolute value and the influence of an applied voltage are decreasing with increasing temperature. As mentioned before, this is not due to self-heating effects. The temperature dependence of the resistor at a fixed voltage is shown in Fig. 3. With rising temperature the intrinsic carrier density rises, so the resistance is reduced. Equation (1) describes the temperature behaviour of the intrinsic carrier density [2].

$$n_i^2 \sim T^3 \cdot e^{-\frac{E_G(T)}{k_B \cdot T}} \quad (1)$$

Resistors with different width W to length L ratios, but same nominal value were measured to investigate the influence of the applied voltage. It was shown that a longer and wider resistor is less sensitive to an applied voltage. Therefore, the resistance is a function of the electric field strength. This knowledge leads to a design consequence. It is not possible to have a linear resistor with minimal geometric size. The circuit designer has to make a trade-off between the geometric size and nonlinearities of the resistor.

A simple resistor model, for example an implementation in SPICE, is not sufficient for the modelling. This simple model does not show a dependence on the applied voltage just on the temperature. The most compatible way to overcome this issue is a behaviour modelling via a sub circuit. The scalable macro model with physical and empirical approach consists of a voltage controlled current source. The function is represented by equation (2).

$$I = 2 \cdot d \cdot (W - 2 \cdot \Delta W) \cdot IF \cdot A \cdot T^2 \cdot e^{\left(-\frac{\phi_b}{k_B \cdot T}\right)} \cdot \sinh\left(\frac{q \cdot V \cdot L_K}{2 \cdot k_B \cdot T \cdot (L - 2 \cdot \Delta L)}\right) \quad (2)$$

A ..... Richardson constant
d..... sheet thickness
E_G ..... energy gap
I ..... current
IF ..... idealization factor
k_B ..... Boltzmann constant
L ..... length
ΔL ..... edge displacement length
L_K ..... mean grain length
n_i ..... intrinsic carrier density
q ..... elementary charge
T..... absolute temperature
V..... applied voltage
W..... width
ΔW .... edge displacement width
ϕ_b..... barrier height at grain boundaries in eV

In poly-Si with light and medium doping concentration, the current flow is mainly determined by grain boundaries. The resistance of the grains themselves is negligible. Trapping of carriers at the grain boundaries causes the creation of potential barriers. Hence, the effective mobility of the carriers is reduced. The overcoming of the potential barriers is mainly a thermally activated process. The so-called thermic emission was firstly described by Seto [3].

The optimization of the model parameters was performed with the MS-EXCEL solver. An effective error of 4 % could be achieved over the entire temperature and voltage range. The maximum error was determined with less than 15 %.

Fig. 4 shows that the resistance also depends on a transverse field. This dependency can be explained by accumulation and depletion effects in the poly-Si. Due to the low doping concentration, the quantity of free carriers is strongly determined by the intrinsic carrier density that is a function of temperature.

The described effect is not covered by the actual model yet. Further investigations will enable a model improvement and include the influence of a transverse field.

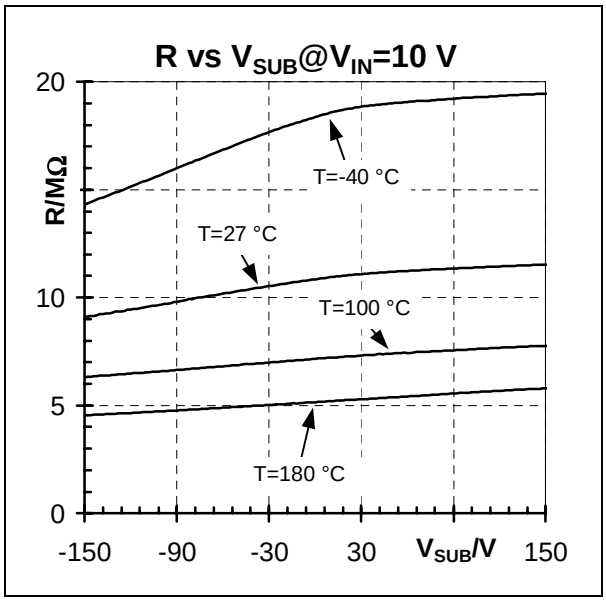

Fig. 4: Influence of a vertical electrical field

High value resistors in feedback loops

Fig. 5 shows a block diagram of a high-voltage amplifier. The feedback loop consists of the resistors R1 and R2. Of course, the influence of parasitic elements due to the substrate is not negligible. The equivalent circuit is shown in Fig. 6. C_{SUB} is the substrate capacitance, C_{Stray} represents capacitive coupling between input and output, and C_p along with R_p describe the probe impact. The compensation capacitor C_{Comp} displaces the frequency response to a high-pass behaviour (Fig. 7). This displacement compensates a transfer function pole of the high-voltage amplifier circuit.

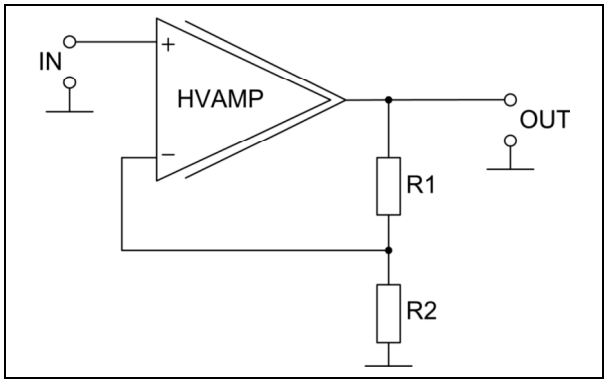

Fig. 5: Simplified block diagram of a high-voltage amplifier with feedback loop

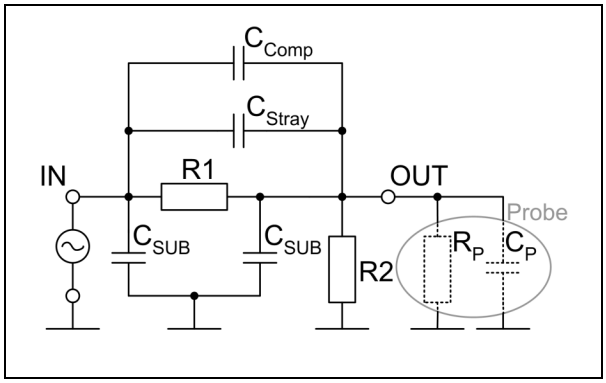

Fig. 6: Equivalent circuit of the feedback loop

High-voltage amplifier circuits will be developed to drive capacitive loads such as micro mechanical mirror-arrays. The electrical strength has to be above 300 V. The size of one high-voltage amplifier has to be small enough to integrate 16 or more amplifier stages on one chip.

The feedback loop, consisting of resistors R1 and R2 (Fig. 5), needs a large chip area. About 420 µm × 150 µm excluding the size of four pads were used in the test circuit (Fig. 8). The power dissipation of the feedback loop is 9 mW. The measured fluctuations of resistance caused by mismatch amounts approximately 1.9 %. Fluctuation of resistance caused by impact of electrical field is about 4.7 % or 18 % depending on substrate connector is grounded or on the high-voltage rail. This result shows the importance of electrical shielding of high-voltage polysilicon resistors. The aspect of matching has a slight part by comparison. A possibility of electrical shielding with minimized resistor fluctuation is an interrupt shield electrode with a stepwise voltage increase.

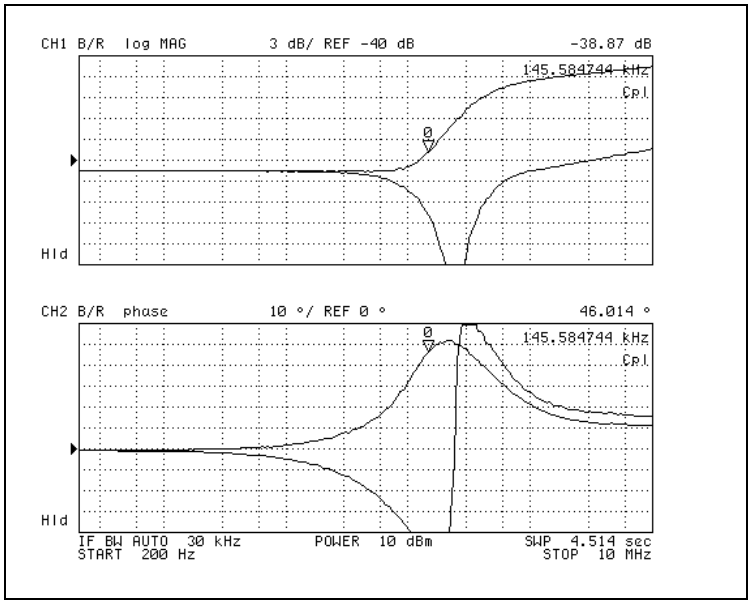

Fig. 7: Measured frequency and phase response of a feedback loop

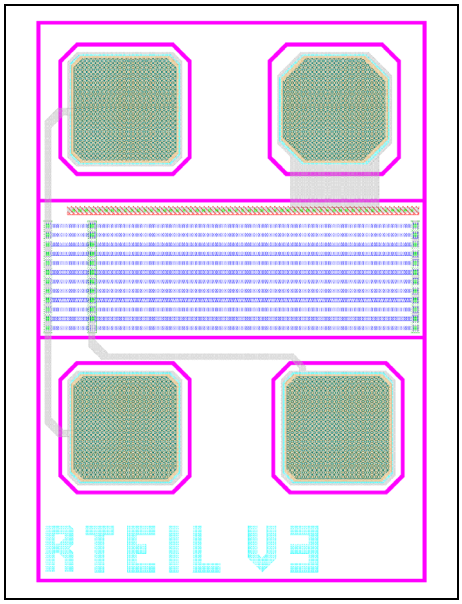

Fig. 8: Layout of a feedback loop test circuit

However, electrical shielding of resistor area increases capacitive coupling and decreases the bandwidth of signal transmission. Therefore, a trade-off has to be made between power dissipation, linearity and critical frequency.

Conclusion

An analysis of high-ohmic polysilicon resistors for high-voltage applications was presented. The focuses of the discussion are the experimental characterization and the modelling of high-ohmic polysilicon resistor structures. A scalable macro model represents the physical reality especially in terms of temperature behaviour. Thereby, modelling techniques like sub circuits were used.

References

[1] A. Hastings: The Art of Analog Layout, Prentice Hall, 2000.
[2] M. Shur: Introduction to Electronic Devices, John Wiley & Sons Inc., 1996
[3] J.Y.W. Seto: J. Appl. Phys. 46, 5247 (1975)