Interface between porous ultra low-k materials for 45 nm node and diffusion barrier - pore sealing approaches

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1 Introduction

One of the main challenges for integrating porous low-k dielectrics into Copper damascene interconnect schemes is the interface between the conducting diffusion barrier and the etched porous material at the trench and via sidewalls. It has been shown, that different issues exist for barrier deposition onto the porous material:

- Precursor penetration into open-pore dielectrics during either barrier CVD or ALD,
- Resulting barrier deposition in the surface-near region or even in the whole porous dielectric,
- Formation of a porous or less dense barrier at porous surfaces (PVD, CVD) causing decreased barrier efficiency.

To overcome these problems pore sealing has to be performed at the trench and via sidewalls. Different approaches exist to achieve smooth and/or sealed sidewalls of porous dielectric materials after etching:

- Deposition of a CVD dielectric liner of minimum thickness and subsequent spacer formation by etching [1].
- Deposition of a very thin spin-on dielectric sealing layer.
- Post-etch burnout (PEBO) of porogen in the dielectric: The porogen contained in the dielectric is usually removed after deposition by annealing and leads to the formation of the porous structure. Special porogens (e.g. in pSiLK) are modified during dielectric etch at the sidewall of the patterns, where they are exposed to the etching chemistry. A porogen removal (burn out) after etching leads to decomposition of the porogen only at not exposed locations leaving the porogen at the sidewall in place. This results in a smoother and sealed non-porous sidewall.
- Solid first™ or post-CMP burnout: The porogen contained in the dielectric is removed after CMP. For this case the dielectric is dense during integration which is important for CMP and exhibits a dense and non-porous sidewall after etching.
- Sealing of the sidewalls during etching by formation of sidewall passivation layers and/or plasma impact.
- Sealing of the sidewalls by plasma treatments after patterning.

In the examinations described in the following we applied pore sealing by using a CVD dielectric liner for porous spin on dielectrics with different pore size.

2 Experimental

A SiO_2 aerogel with a pore size of ~ 7 nm and a porous MSQ with ~ 3 nm pore size was deposited by spin on with a PECVD SiN cap layer to prevent interactions between photoresist and the porous material. The low-k dielectrics were patterned using reactive ion etching in an ICP discharge with CF_4 and Ar. After etching the photoresist was stripped by using an H_2/N_2-plasma. PECVD SiO_2 was used as liner material because it has the lowest k compared to SiC and SiN. The TiN barrier was deposited from TDMAT followed by a N_2/H_2 plasma treatment using one to 8 cycles of TiN deposition and plasma treatment. The process is described particularly in [2, 3]. Fig. 1 shows the cross-sections of the investigated samples.

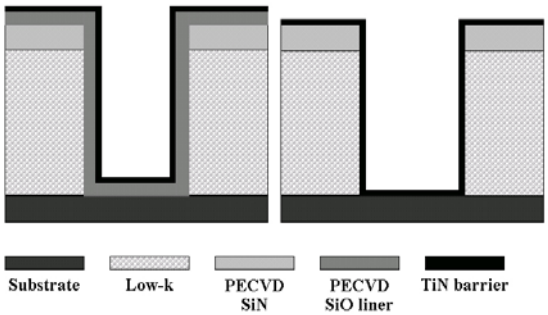

Fig. 1: Investigated porous low-k samples with (left) and without (right) CVD liner for pore sealing

3 Investigation of the TiN/porous dielectric interface

TEM and EDX line scan were done for samples of 10 nm TiN with and without 20 nm CVD liner, to determine the depth of penetration of TiN into aerogel (7 nm pore size) and MSQ (3 nm pore size) at the sidewall of the structures.

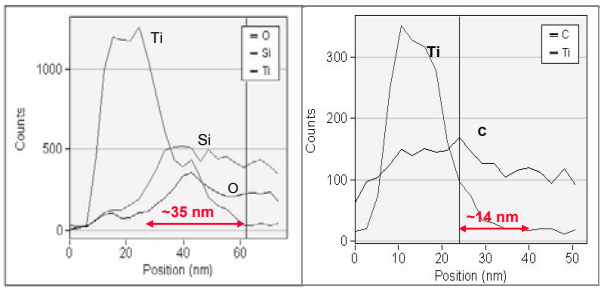

Fig. 2: EDX line scan of a TiN/Aerogel interface:at the surface (left) and at the trench sidewall(right)

Figure 3 shows EDX line scans of TiN/aerogel interface on top of the non-patterned dielectric and at the sidewall of an etched trench pattern (without CVD liner). At non-patterned samples Ti was detected in the dielectric up to a depth of 35 nm [4]. The Ti signal in the aerogel decreases down to the detection limit at a depth of ~ 14 nm at the Ti/aerogel interface at the trench sidewall. This may be due to a partial pore sealing by aerogel etching or photoresist stripping. Furthermore the highest carbon signal was measured at the interface (Fig. 3, right) indicating a possible formation of a sidewall passivation layer during ULK etching using a photoresist mask as reported in [5]. A CVD liner showed no additional improvement in preventing TiN prenetration.

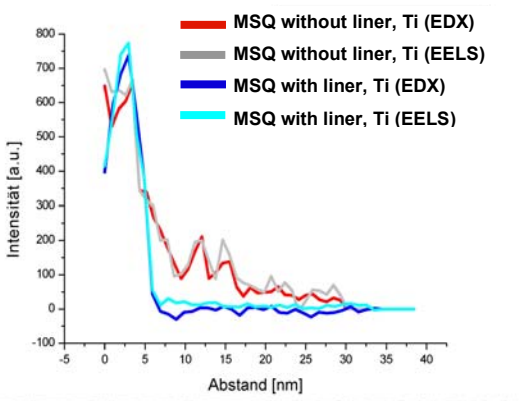

Fig. 4: EDX and EELS line scan of a TiN/porous MSQ interface with and without PECVD SiO_2 liner

EDX/EELS line scans of samples of TiN on porous MSQ show the positive impact of the CVD liner (Fig. 4). Without CVD liner the Ti signal in the MSQ decreases down to the detection limit at a depth of ~ 14 nm. This makes no difference to the respective aerogel sample and indicates no impact of the dielectric pore size on TiN precursor indiffusion. For the sample with CVD liner nearly no TiN penetration was detected. The Ti signal decreases abruptly just after the TiN/CVD liner interface. The reason is an improved pore sealing by the CVD liner due to the smaller dielectric pore size of the MSQ leading to a lower sidewall roughness and therefore improved barrier film growth.

3 Summary

The impact of different ULK material pore size (3 and 7 nm) on TiN diffusion barrier integrity was investigated. In addition, a SiO_2 CVD liner was used for pore sealing. It was detected that a smaller pore size facilitates better CVD liner and TiN barrier growth which results in a better barrier integrity. For SiO_2 aerogel with 7 nm pore size the CVD liner has no effect for the samples of 10 nm TiN with and without CVD liner. For the ULK material with 3 nm pore size an obvious improvement was found using the SiO_2 CVD liner. Furthermore a reduced TiN penetration into the aerogel dielectric compared to non-patterned samples was detected. This is believed to be caused by a partial pore sealing during ULK etching using a photoresist. Further investigations are in progress to prove this assumption.

4 References

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