Extraction of k_{eff} of multilayer intermetal dielectric stacks by FEM simulation

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1 Introduction

The continuous reduction of geometrical dimensions in microelectronics is the reason for a super proportional increasing of unwanted electrical effects, working against a further acceleration of IC clocking. Dominant forces are parasitic capacitances between, and the resistivity along, the metal lines in backend interconnect systems (characterized by the R·C time delay). Substitution of aluminium by copper reduces R, because of the higher conductivity offered by copper. The reduction of C is basically possible by reducing the k-value of the inter- metal- and inter-layer dielectrics.

$$C = k_0 \cdot k_{eff} \cdot \frac{A}{d} \qquad (1)$$

Newly developed films with a lower k-value (low-k materials), than the conventionally used SiO_2 for dielectrics (k=4.2), have been introduced more or less successfully in copper-damascene technology in the last few years.
These films have generally reduced density and polarizability and are often porous which implicates deteriorated mechanical, thermal and chemical properties. For damage-free treatment during process steps like patterning or resist stripping, or to improve adhesion, additional films are necessary. In the end, these functional layers influence the effective k-value between the metal interconnects. Characterization of low-k material requires indication of the true working k-value (k_{eff}) of the functional stack consisting of low-k and additional layers.

2 FEM simulation of k_{eff}

Figure 1 shows a schematic cross section of a damascene architecture. The low-k material is vertically and horizontally enclosed by several other dielectric materials needed for poresealing and patterning processes. The effective k-value of the low-k material, SiO_2 spacer, hard mask and stop layer should be estimated at all. The k-value of every single layer is known.

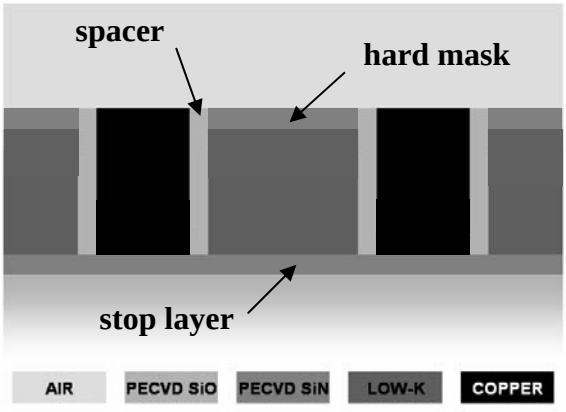

Fig. 1: Schematic cross section of a damascene architecture with application of a spacer material

Via application of a static FEM analysis, the resulting capacitance C_{all} between the two copper lines within this system was calculated. A sample of the formed field with its equipotential lines is shown in figure 2.

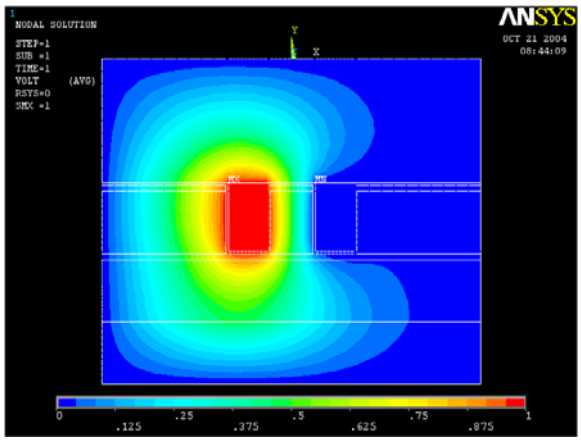

Fig. 2: Equipotential lines simulated via FEM analysis

In the the next step, the simulation model was simplified. All functional layers concerning to the low-k material were merged and furnished

with the same k-value k_{mat}. By the usage of a binary search algorithm the k_{mat} was determined, which results in the same C_{all} for the modelled simlified architecture. In figure 3, the according k_{eff} is the k-value of the intersection point of both graphs.

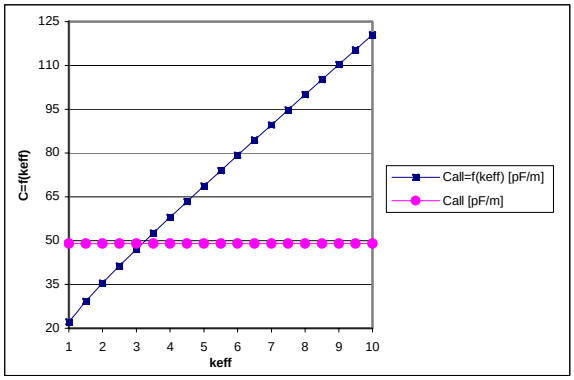

Fig. 3: Simulated C_{all} (multilayer and merged dielectric stack)

The chosen procedure of simulation allows observation of the behaviour of the system without paying attention to the leakage field. We can truly estimate the influence of the electrical properties of additional layers, of the geometrical dimensions and of the architecture itself. In figure 4 the interconnect distance and interconnect width were changed.

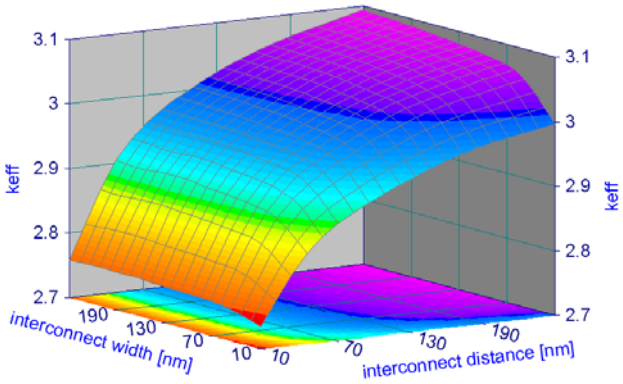

Fig. 4: Example for the effect of variation of geometrical dimensions on k_{eff}

Additionally to the described simulation approach, these FEM analyses were used to verify electrical measurements on prepared samples. The real geometrical dimensions are necessary as an input for the interconnect system to be modelled. FIB preparation combined with SEM is a suitable technique to determine the geometrical parameters at cross sections. An example of such a preparation is shown in figure 5.

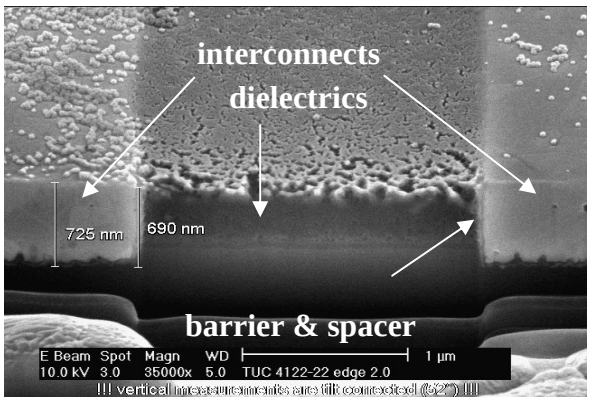

Fig. 5:FIB preparation of a copper damascene architecture

The porous spin on SiO_2 Aerogel, developed at the Centre for Microtechnologies, was used as dielectric, CVD TiN as barrier, Copper as interconnect and PECVD SiO_2 as spacer material.