# The Bonding and Deep RIE (BDRIE) technology approach for high aspect ratio sensors and actuators

**K. Hiller[1], M. Küchler[2], M. Dienel[1], T. Gessner[1,2]**
[1] Chemnitz University of Technology, Center of Microtechnologies, Chemnitz
[2] Fraunhofer Institute Reliability and Microintegration, Department Micro Devices and Equipment, Chemnitz

## 1 Introduction

For several years, high aspect ratio technologies based on deep dry etching have been used and commercialised e.g. for fabrication of inertial sensors. The typical height of structures varies between 12 µm (epipoly-surface technology) and up to 50 µm for SOI, SCREAM and other related technologies. These technologies use isotropic underetch steps in order to release the movable structure, therefore a lot of design restrictions concerning the size and arrangement of gaps and beams exist, movable structures must have the typical holes for underetching, and the size of the vertical gap is restricted to some microns. Alternative approaches use dry etching steps in combination with bonding processes. The basic idea of BDRIE, characterised by bonding of two wafers with pre-patterned vertical gaps and subsequent RIE trench etching of the active layer, has already been described before (e.g. [1]). We have investigated two special approaches with some variations of this Bonding and Deep RIE technology, which are described and discussed below.

## 2 BDRIE APPROACHES

Both glass and silicon can be used for the basic wafer. Fig. 1 shows the scheme of the anodically bonded silicon-glass compound (BDRIE A). The silicon layer contains the movable structure as well as drive and detection electrodes for lateral movement. Wire bonding pads on top define the electrical contact areas. A flat groove for vertical movement and detection has been etched from the backside of the silicon wafer prior to bonding. The glass wafer contains detection electrodes for vertical movement. The access to these underlying electrodes can be provided either by contact holes or by pressure contacts to the silicon islands. These areas are electrically insulated by air gaps in lateral direction and the glass substrate in vertical direction. Hence, depending on the gap size, the parasitic capacitance is very low. With this approach it is possible to create HARM structures which can be actuated and sensed both in lateral and vertical direction.

For the directly bonded silicon-silicon compound (Fig. 2), the groove is preferably etched into the silicon basic wafer. Thick thermal oxide layers are used for vertical insulation and air gaps for lateral insulation. Although the integration of vertical detection electrodes would be possible with a high effort, we have not tested this option, therefore this approach is suitable for structures with lateral drive and detection capacitors.

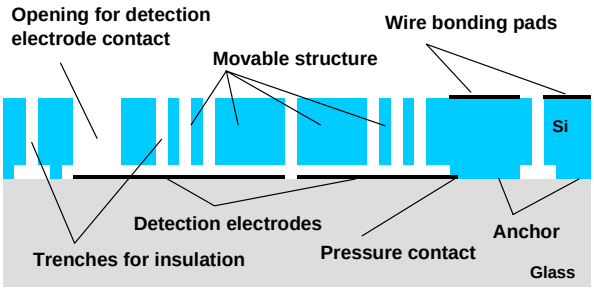



*Fig. 1: BDRIE A: Silicon-glass*

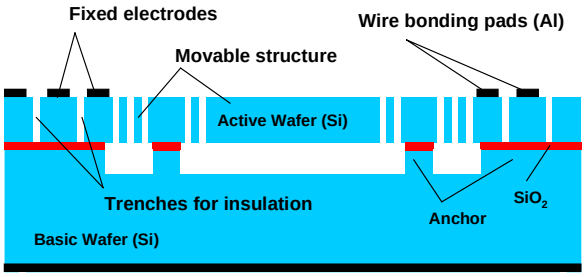



*Fig. 2: BDRIE B: Silicon-Silicon*

### 2.1 Wafer bonding

The wafer bonding processes for basic and active wafers have been carried out using a commercial wafer bonding equipment (SB6, Karl Suss). In case of anodic bonding, we used Pyrex glass for

the basic wafer. A patterned aluminium bond electrode on the backside of the glass, forming a grid structure aligned to the chip frames enables a reduction of bond voltage down to about 300 V. Bond temperatures were in the range of 360 ... 400°C. For direct bonding we normally utilise a hydrophilic regime: RCA cleaning, pre-bonding at room temperature with a bond tool pressure of 3 bar, and subsequent high temperature annealing (1000°C, 5 hours). With both processes we have successfully bonded minimum (anchor type) areas of (100 x 100) µm² and chip frames of 150 µm. During the bond process the pre-etched cavities are sealed. Several investigations [2] have shown that it is advantageous to seal the cavities in vacuum at a pressure of about 1 mbar.

## 2.2 Active layer thickness

The active layer thickness is suitable in the range from 30 µm to 300 µm with an optimum value depending on the specific application. Due to the specific of the BDRIE process, some limiting conditions must be taken into account, too. Before trench etching, the active layer forms a membrane over the recess, which undergoes a deflection depending on the thickness, the gap area and the pressure inside the cavity (see Fig. 3) [2]. This deflection should be as small as possible [nm range], especially in case of high temperature annealing, when silicon can undergo a plastic deformation, which is irreversible. Therefore during high temperature annealing a thick wafer is required.

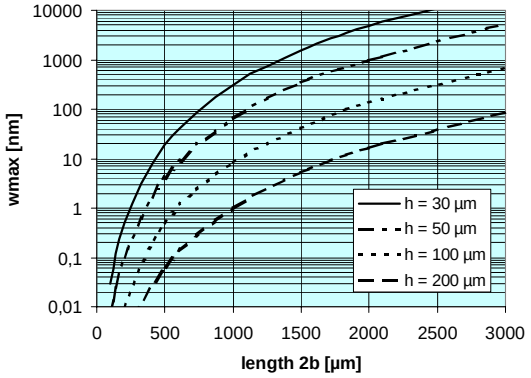



*Fig. 3: Maximum deflection in the middle of a square* with side length 2b ( pressure difference of 1 bar)

Thinning of the active layer can be achieved

a) by grinding and polishing,
b) by etching and polishing
c) by bonding of an SOI wafer and etching the handle wafer.

Both methods b) and c) have been tested successfully. During thinning, the maximum deflection is increased, but should not exceed 1 µm in order to enable the stepper lithography for the trench mask. In case the recess is too large, special support posts (anchor type) can be introduced (see Fig. 2).

## 2.3. Trench etching into cavity

The trench etching process should provide a highly anisotropic etch behaviour and a good homogenity, a sufficient selectivity to mask and moderate etch times. Nowadays the time multiplexed deep etch (TMDE) technique is widely applied, which is based on a repetitive sequence of deposition and etching steps. During deposition $C_4F_8$ is used to form sidewall passivation, whereas $SF_6$ is used to perform etching. This work was performed using a Surface Technology Systems multiplex ICP. The high density ICP plasma source is powered by an rf generator supplying 1 kW at 13.56 MHz. Bias is generated at substrate electrode by means of a pulsed rf generator operating at 380 kHz (LF processes, especially for wafers including isolating substrates). The trench profile of the LF precision process, which can be used for a layer thickness up to 100 µm, is shown in Fig. 4.

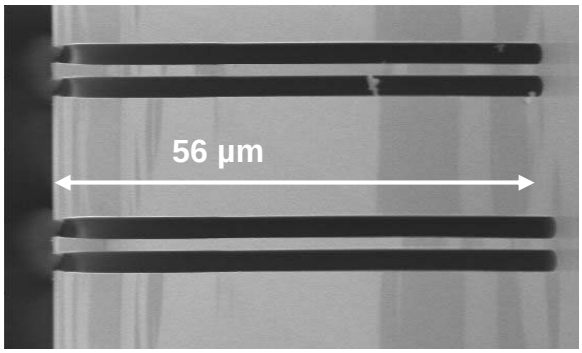
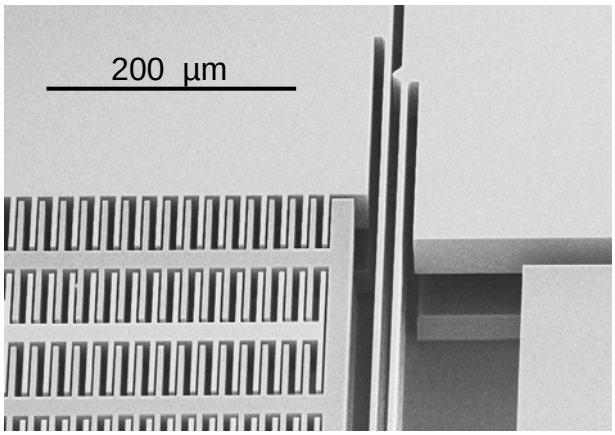
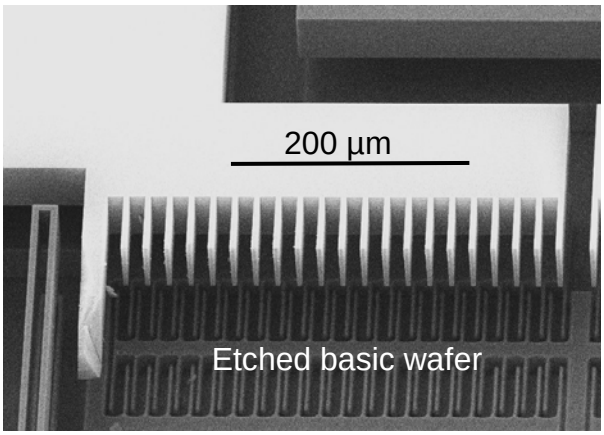



*Fig.4: Trench profile of the precision LF process* (*Sidewall angle 90.2 … 90.3°)*

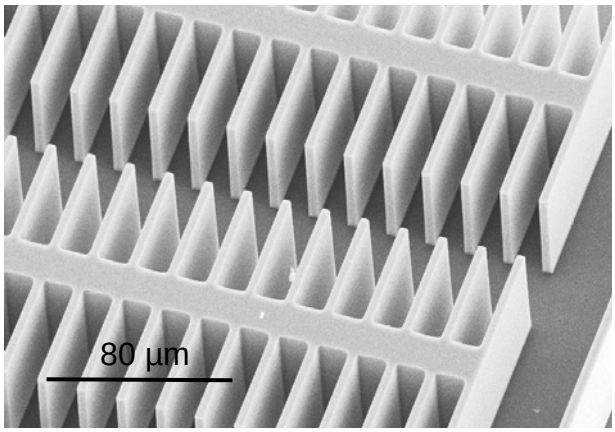
The trench etching process has to be continued until all trenches have reached the cavity, thus way the structure is released. Usually, due to the aspect ratio depending etching (ARDE), the wider trenches reach the cavity first. When the process goes on, the silicon substrate of the basic wafer is etched, too. In case of a glass substrate it is useful to introduce a conducting screen electrode underneath the trenches in order to avoid backscattering of the ions and backside etching [2]. Fig. 5 shows SEM pictures of typical structures fabricated with the Silicon-Silicon BDRIE approach.



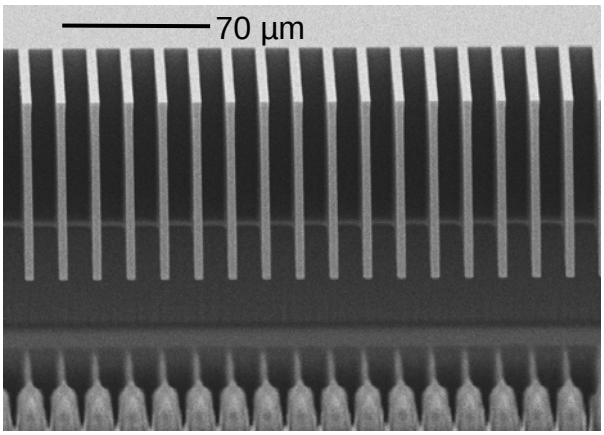

a) top view




b) view on bottom after removing of structure




c) view on backside of structure (50 µm thickness)




d) view on fixed part of a comb drive (75 µm thickness)

*Fig. 5: SEM pictures of fabricated structures (acceleration sensor)*

## 3 Applications

The BDRIE approach can be applied for all types of inertial sensors, e.g. acceleration sensors, gyroscopes, vibration sensors and resonators, but also for actuators like torsional micromirrors.

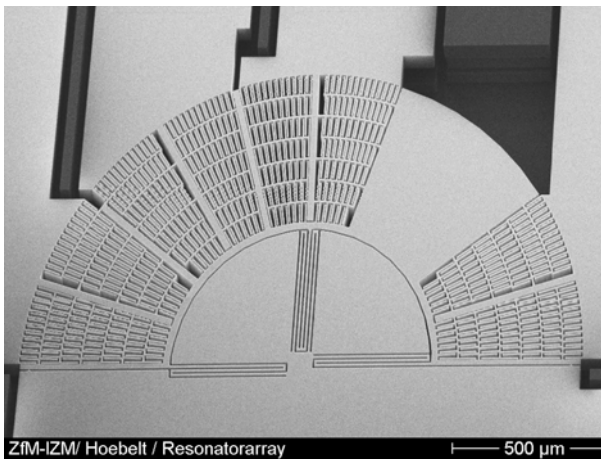



*Fig 6: Acceleration sensor*

For example of silicon-silicon compounds, Fig. 10 shows part of an asymmetric central fixed acceleration sensor [3]. In this example, the structure height is 50 µm, the smallest trench width is 2 µm and the maximum free standing membrane (area around the moving segment) is about (1.6 x 1.6) mm².

BDRIE structures can be packaged e.g. using a silicon cover wafer and either polymer bonding, direct bonding or glass frit bonding [2].

### References

[1] Capuz, C.; Ridley, J. (Honeywell International Inc.): *Thin Silicon micromachined structures*, international patent publication WO 02/051743 A3, 2001

[2] Hiller, K. et al.: Bonding and Deep RIE – a powerful combination for high aspect ratio sensors and actuators, submitted to SPIE 5715, San Jose (CA), Jan. 2005

[3] Billep, D.; Dienel, M.: *Acceleration sensor*, German patent DE 10 2004 046 411.1, 2004