Fabrication of SOI substrates with buried silicide layers for BICMOS-applications

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A new approach for fabrication of special SOI substrates offering the possibility of high performance CMOS and high performance bipolar technology on the same SOI substrate will described. The new substrates consist of a buried silicide layer on top of the buried oxide covered with a thin silicon film for the device fabrication.

There are two versions to prepare a SOI substrate with a buried $CoSi_2$ layer. The first technology, is a combination of the cobalt-salicide [1] process and a technique, which includes different CMP-processes and a wafer bonding step. This means the first technology includes a modified BESOI regime and has several similarities with the BESOI process, described in [2]. The process flow is shown in fig. 1.

The starting point for the first version is a commercial SOI wafer with 1 µm buried oxide and a 300 nm thick Si device layer. After the removal of the native oxide 30 nm cobalt and 8 nm Ti were deposited without a vacuum break. The conversion of the cobalt film into a $CoSi_2$ includes two RTA steps and one wet chemical process. The process results in a structured $CoSi_2$ film on silicon and is known as cobalt salicide process. To get plan surfaces for the bonding process, 500 nm PECVD-SiO_2 were deposited and the steps were removed using an oxide CMP process. The final thickness after the CMP process was 250 nm. All CMP processes were performed using an Applied Materials Mirra polisher. Afterwards the wafer was bonded to a handle substrate deposited with 250 nm oxide by high temperature silicon direct bonding. The result is the structure presented in fig. 1. The handle wafer with oxide is on the bottom and on the top is the SOI-substrate with the buried $CoSi_2$ layer. To finish the SOI-substrate it is necessary to remove the former handle wafer of the SOI-substrate. In a first step the handle wafer of the SOI substrate was grinded back to a final silicon thickness of 20 µm. The last 20 µm were selective etched to the buried oxide of the SOI substrate using a spin etch tool. In a next step the buried oxide of the SOI substrate is etched back chemically in diluted HF. In the last step a silicon CMP process removed the surface roughness of our new SOI substrates.

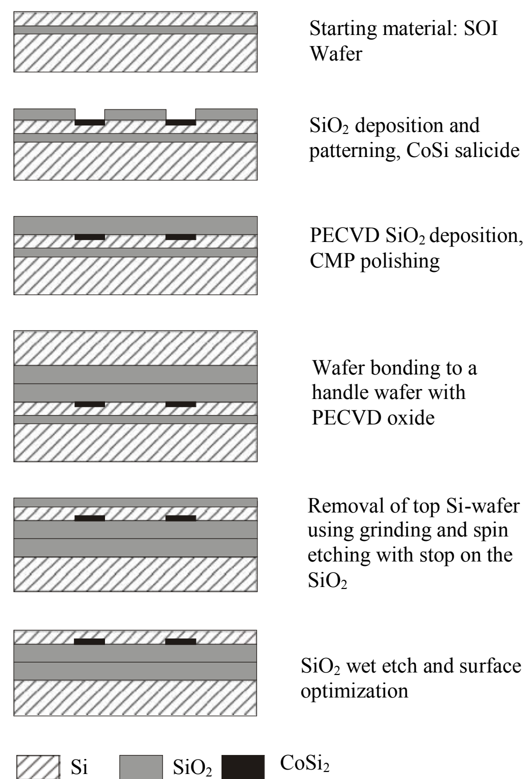

Fig. 1: Process flow to prepare a SOI substrate with buried silicides using the modified BESOI regime

The second version to fabricate SOI substrates with buried silicide is a combination between cobalt salicide process, silicon layer transfer by hydrogen implanted layer splitting (HILS) and silicon direct wafer bonding. The process flow is shown in fig. 2.

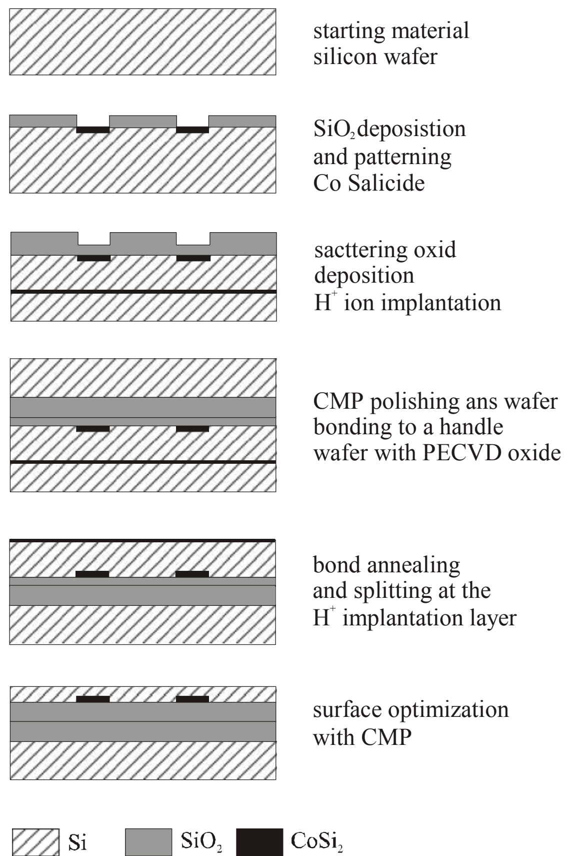

Fig. 2: Process flow to prepare a SOI substrate with buried silicides using the hydrogen implanted layer splitting regime (HILS)

An IR image of a bonded wafer pair is shown in fig. 3. We tested LP-CVD and PE-CVD SiO_2 to find the most suitable interface material for the wafer bonding process. The best results were obtained with PE-CVD SiO_2. But it is necessary to anneal the wafers before the bonding process. This step was performed to suppress hydrogen out gazing during the bond annealing. After the bonding process an annealing at 800 °C for 4h in N_2 is necessary to improve the bond strength.

The roughness of the $CoSi_2$/Si interface was measured with AFM after the removal of the silicide with 35 % HF solution. The measurements show a roughness average value of 11nm.

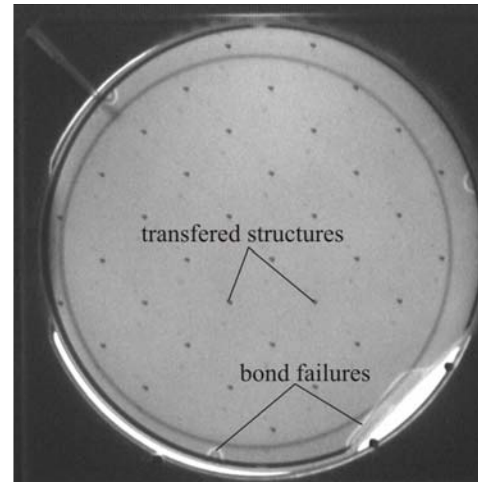

Fig. 3: IR image of a bonded wafer pair

A cross section through such a structure is shown in fig. 4. It can be seen that the $CoSi_2$ surface is moving into the silicon because the large silicon consumption during the cobalt silicidation.

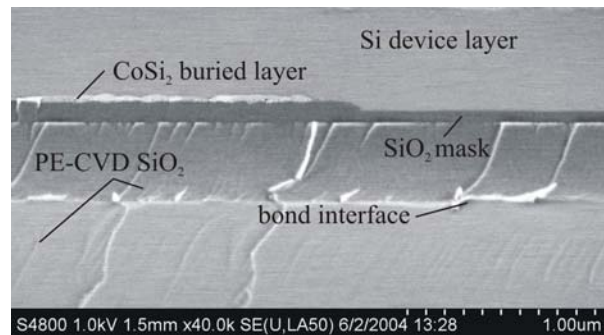

Fig. 4: SEM cross section of the SOI substrate with buried $CoSi_2$

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Key words

Silicides, SOI, silicon direct wafer bonding, hydrogen implantation