Annual Report 2004

Center for Microtechnologies (ZfM)

Editors:
Prof. Thomas Gessner
Dr. Wolfgang Seckel

Postal address: **Reichenhainer Str. 70**
D – 09107 Chemnitz

Contents

1 Preface

As in preceding years, the Center for Microtechnologies in close cooperation with the "Micro Devices and Equipment" Department Chemnitz of the Fraunhofer Institute for Microintegration and Reliability (FhG-IZM) in Berlin has further consolidated its position as a Center of Excellence in the fields of microelectronics back end technologies and microsystem technologies.

The key to our success was an interdisciplinary cooperation of several chairs within the ZfM. Based on this idea, ZfM's primary mission is to provide an intellectual and working environment that makes possible education through teaching and research in areas that require or may benefit from advanced ULSI-interconnect technologies, Si-nanotechnology and new developments and ideas in the field of MEMS by using microfabrication technologies. ZfM's technology laboratories provide a complex of modern microelectronics laboratories, clean rooms and microfabrication facilities.

Meanwhile the Fraunhofer IZM Department Micro Devices and Equipment Chemnitz exists more than 5 years. The successful integration of MEMS packaging, MEMS system development and equipment as well as process simulation in cooperation with the ZfM has become more and more apparent.
This issue was demonstrated at the Colloquium "Centre of Competence for Micro- & Nanosystems" - 5 years Fraunhofer IZM, Dept. Micro Devices and Equipment, Chemnitz – in August 2004.

We are very pleased that Prof. Dr. Josef Lutz was elected as a new member of the board of directors of the ZfM.

It is my pleasure to summarize some of the scientific highlights of 2004:

- Development of a low-k compatible H_2-based resist stripping process
- Establishing CMP equipment & process for advanced process development and material assessment in Cu / barrier CMP on porous low-k dielectrics
- Development & investigation of ultrathin ternary CVD diffusion barriers (Ti(Si)N, W(Si)N)
- First prototypes of two-axis inclination sensors based on AIM technology successfully fabricated.
- Silicon gyroscope chips from Chemnitz have been sucessfully implemented and tested within a miniaturised LITEF demonstrator for avionic applications.
- A novel 24 kHz scanner with very high optical performance has been developed and successfully tested. It is applicative for horizontal laser deflection in head up displays.
- A micro friction vacuum gauge has been qualified for operation within a temperature range of room temperature up to 350 °C.
- Frequency selective sensors for structure born noise on base of a MEMS chip have been developed. Samples for 2 kHz, 3.5 kHz, 4.5 kHz and 6 kHz are available.
- Development of new software modules for parametric model generation of MEMS based on variational Finite Element techniques.

- System integration of frequency selective sensor arrays for vibration monitoring at cutting tools.

- A new substrate based on SOI technology with buried silicides usable for high performance RF microelectronic devices was developed successfully and is been transferred for industrial application.

- A bulk micromachined ultrasonic transducer is designed and fabricated. Compared with similiar products, this newly developed transducer has the advantages of uniform cavity, consistent elements, and reliable vibration membrane.

- Resonant structure implemental for low pressure measurements inside of hermetically sealed micromechanical devices have been fabricated.

- Tunable infrared filter based on Fabry-Perot-Interferometer suitable for gas analysis systems have been improved.

- Miniaturized dual detector NIR-spectrometer based on micro mechanical scanners with integrated gratings appropriate for substance analysis in gaseous, liquid and solid state has been developed.

- Within the frame of projects NanoCMOS and Skalar the in-house multi-purpose simulation environment T2 has been extended to multi-scale simulation of thin film deposition using advanced PVD and of planarization of oxide films for Shallow Trench Isolation (STI).

The 2004 Annual Report of the Center for Microtechnologies provides an overview of the facilities, staff, faculty and students associated with the ZfM, as well as a description of many of the ongoing research projects which make use of the ZfM facilities.

These developments, which are based on close links with industry and cooperation with German as well as international institutes, contribute to an advanced education for our students. We kindly acknowledge the support of the Federal Ministry of Research, the German Research Foundation, the Saxon Ministry of Science and the European Commission.

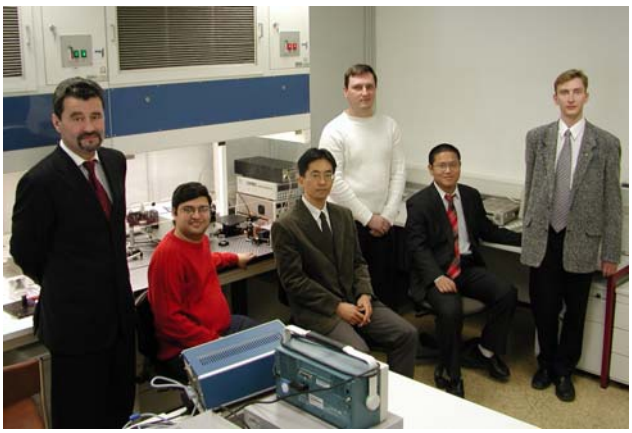
As always, we are driven by our triple aims of excellence in education, scientific and technological research and by providing a comprehensive range of research and development services to industry.

I would like to thank all my colleagues, the scientific fellows and technicians for all their dedicated work.

I look forward to participating in the promising development of new devices and concepts through the use of silicon technology.

Thomas Gessner
President of the Center for Microtechnologies

International cooperations



Prof. Thomas Gessner together with international students and co-workers

From left:
Srihari Sankisa, University of Nevada, Reno, USA – IAESTE program;
Yukito Sato, Ricoh Ltd., Sendai, Japan – Scientist;
Wladimir Kolchuzhin, University of Novosibirsk, Russia – PhD;
Chenping Jia,University of Xian, China – PhD;
Alexej Schaporin, University of Novosibirsk, Russia - PhD

Prof. Gessner – guest of "75th anniversary of Chongqing University", China

Prof. Li Xiaohong, President of Chongqing University

Prof. Zhu Jialin, Chairman of Chongqing Association for Science and Technology

Delegation of Brazil

Mr. Hernan Valenzuela
Brazilian Ministry of Development, Industry and Foreign Trade (SUFRAMA), Coordination of Institutional Relations for Technological Affairs (COART)
meets members of our university and of the FhG

Colloquium
"Centre of Competence for Micro- & Nanosystems"
- 5 Years Fraunhofer IZM, Dept. Micro Devices and Equipment, Chemnitz -

August 10, 2004

Dr. Peter Seifert, Lord mayor of Chemnitz congratulates Prof. Gessner on his birthday

2 Organization

Center for Microtechnologies

Prof. Dr. Wolfram Dötzel
Prof. Dr. Gunter Ebest
Prof. Dr. Joachim Frühauf
Prof. Dr. Thomas Gessner
Prof. Dr. Josef Lutz
Prof. Dr. Dietmar Müller
Prof. Dr. Christian Radehaus

Our scientific research focuses on microsystem technology, microelectronics, as well as opto-electronics and integrated optics. In these fields, the Chemnitz University of Technology has had a tradition and experience of more than 30 years.
The research comprises ULSI metallization technologies, fabrication and application of micromechanical components, modeling, simulation and design of processes, devices, components, circuits and test structures down to the nanometer range, as well as single electron tunneling technologies, nonlinear photonic materials and fiber optics.
In education, the specified and related topics are taught in the basic and main courses. The institute offers the specializations Electronics/Microelectronics, Microsystem/Device Technology and Mechatronics.
The equipment is provided for the institute in combination with the Center for Microtechnologies and comprises a complete silicon wafer line, mask making equipment, commercial software and hardware for simulation and design, as well as extensive analysis and semiconductor measurement technology.
The Center for Microtechnologies facilities include 1000 m² of clean rooms (about 30 % of them class 10 to 100) with equipment for mask and wafer processes.

Visit our homepage: **http://www.zfm.tu-chemnitz.de**

Chair Microsystems and Precision Engineering
Professur Mikrosystem- und Gerätetechnik
Prof. Dr.-Ing. Wolfram Dötzel
phone (+49 371) 531 3264
fax (+49 371) 531 3259
e-mail: doetzel@etit.tu-chemnitz.de
www.infotech.tu-chemnitz.de/ ~microsys/index.html

Chair Electronic Devices
Professur Elektronische Bauelemente
Prof. Dr.-Ing. Gunter Ebest
phone (+49 371) 531 3125
fax (+49 371) 531 3004
e-mail: ebest@etit.tu-chemnitz.de
www.tu-chemnitz.de/etit/leb/

Chair Microtechnology
Professur Mikrotechnologie
Prof. Dr. Dr. Prof. h.c. mult. Thomas Gessner
phone (+49 371) 531 3130
fax (+49 371) 531 3131
e-mail: Thomas.Gessner@zfm.tu-chemnitz.de
www.zfm.tu-chemnitz.de

Chair Power Electronics and Electromagnetic Compatibility
Professur für Leistungselektronik und elektromagnetische Verträglichkeit
Prof. Dr.-Ing. Josef Lutz
phone (+49 371) 531 3342
fax (+49 371) 531 3327
e-mail: Josef.Lutz@etit.tu-chemnitz.de
www.tu-chemnitz.de/etit/le

Chair Circuit and System Design
Professur Schaltungs- und Systementwurf
Prof. Dr.-Ing. habil. Dietmar Müller
phone (+49 371) 531 3195
fax (+49 371) 531 3193
e-mail: mueller@infotech.tu-chemnitz.de
www.tu-chemnitz.de/etit/sse/

Chair Opto- and Solid-State Electronics
Professur Opto- und Festkörperelektronik
Prof. Dr. rer. nat. Christian Radehaus
phone (+49 371) 531 3086
fax (+49 371) 531 3004
e-mail: cvr@zfm.tu-chemnitz.de
www.tu-chemnitz.de/etit/opto/

Group for Material Science
Arbeitsgruppe „Werkstoffe der Elektrotechnik / Elektronik“
Prof. Dr. rer. nat. habil. Joachim Frühauf
phone (+49 371) 531 3178
fax (+49 371) 531 3202
e-mail: joachim.fruehauf@e-technik.tu-chemnitz.de
www.infotech.tu-chemnitz.de/~wetel/wetel-home.html

Center for Microtechnologies (Scientific Institution)
Zentrum für Mikrotechnologien (ZfM)
President: Prof. Dr. Dr. Prof. h.c. mult. Thomas Gessner
phone (+49 371) 531 3130
fax (+49 371) 531 3131
e-mail: Thomas.Gessner@zfm.tu-chemnitz.de
www.zfm.tu-chemnitz.de

3 Memberships

Prof. Wolfram Dötzel

Vice President for Research of Chemnitz University of Technology, since October 2003
Member of the Academy of Science of Saxony, Leipzig / Germany
Member of acatech (Council of Technical Sciences of the Union of German Academies of Sciences and Humanities)
Gesellschaft für Mikroelektronik und Mikrotechnik (VDI/VDE-GMM)
ESPRIT III – Network „NEXUS“

Prof. Gunter Ebest

Vertrauensdozent „Studienstiftung des Deutschen Volkes“

Prof. Thomas Gessner

Member of „Scientific Advisory Board of the Federal Republic of Germany “ (01.02.1998-31.01.2004)
Member of the Academy of Science of Saxony, Leipzig / Germany
Member of acatech (Council of Technical Sciences of the Union of German Academies of Sciences and Humanities)
Member of “Senatsausschuss Evaluierung der Wissenschaftsgemeinschaft Gottfried Wilhelm Leibnitz” (WGL)
Member of the Board of „KoWi“, Service Partner for European R&D funding, Bruessel
The Institute of Electrical and Electronics Engineers, Inc. (IEEE) , USA
The Electrochemical Society, USA
„Advisory Professor“ of FUDAN University: honorary professor, 1st June 1999
„Advisory Professor“ of Chongqing University: honorary professor, 1st July 2003
Referee of the German Science Foundation (DFG-Fachgutachter) „Systemtechnik“

Prof. Josef Lutz

International Steering Committee of the European Power Electronics and Drives Association (EPE), Brussels
Member of the Advisory Board of the Power Conversion Intelligent Motion Conference (PCIM), Nuremberg
International programme committee of the International Seminar on Power Semiconductors (ISPS), Prague

Prof. Dietmar Müller

Member of the Academy of Science of Saxony, Leipzig / Germany
Member of acatech (Council of Technical Sciences of the Union of German Academies of Sciences and Humanities)

Prof. Christian Radehaus

Optical Society of America (OSA)
The Institute of Electrical and Electronics Engineers, Inc. (IEEE), USA
The American Physical Society (APS)
Deutsche Physikalische Gesellschaft (DPG)

Fraunhofer Institute Reliability and Microintegration
Branchlab Chemnitz
Department: Micro Devices and Equipment

Director: Prof. Thomas Gessner ***Management: Prof. Thomas Otto***

Since 1998 a strong co-operation exists between the Fraunhofer Institute for Reliability and Microintegration (FhG-IZM, Berlin) and the Center for Microtechnologies. Accordingly the department "Micro Devices and Equipment" (MDE) was founded to combine the packaging know-how of the FhG-IZM with the silicon MEMS devices of the Center for Microtechnologies.

The research activities of the department MDE are focused on the following topics:

- *Development of MEMS*: Sensors (kinetic, pressure, force, chemical) and actuators (scanner) are transferred into the system level (e.g. micro spectrometer).

- *Development of advanced technologies* like CMP (chemical mechanical polishing) and 3D-patterning by deep silicon etching as well as increasing the core competence in *MEMS packaging* (chip and wafer bonding including combinations of new materials and bonding at low temperatures)

- *Process and equipment simulation:* The goal is the improvement of deposition and etch rates, uniformity and fill behavior of vias and trenches by optimizing process conditions and reactor design.

- *MEMS design and simulation*:
  - New reduced order modelling features of MEMS provide efficient means for data exchange from component models to circuit and system simulation environment.
  - Novel frequency selective vibration sensor arrays have been successfully integrated into a user programmable vibration measurement unit for wear state monitoring.

One special task of the new assembly technologies development is the combination of silicon micromechanics with down scaled traditional precision mechanics enabling new devices and new low cost fabrication technologies. This is a main challenge in order to push the activities concerning the development and implementation of microsystems for small and medium size enterprises in a short-term period.

In general the strategic alliance between the Fraunhofer Institute for Reliability and Microintegration, department MDE and the Center for Microtechnologies as described ensures strong synergies in the technology and device development.

Nanotechnology Center of Excellence "Ultrathin Functional Films"

The Center of Excellence "Ultrathin Functional Films" (UFF), distinguished by the Federal Ministry of Research (BMBF) as a nation-wide center, is coordinated by Fraunhofer-IWS Dresden. It joins 51 enterprises, 10 university institutes, 22 research institutes, and 6 corporations into a common network. Nanotechnology is one of the key technologies of the 21st century. In order to channel the research results already available at institutes and universities as well as the growing demand from industry, the Nanotechnology Centers of Excellence (CE) had been established in 1998. The Center for Microtechnologies is an active member within this center, especially in the field of microelectronics related topics.

Contact: Office of Center of Excellence "Ultrathin Functional Films"
at Fraunhofer-IWS Dresden
Dr. Ralf Jaeckel
Phone +49 (0) 351 / 25 83 444, Fax +49 (0) 351 / 25 83 300

Activities within the frame of Nano-CE-UFF are subdivided into 6 Working Groups (WG), every one of which is administered and coordinated by one member:

WG 1: Advanced CMOS
WG 2: Novel components
WG 3: Biomolecular films for medical and technological purposes
WG 4: Mechanical and protective film applications
WG 5: Ultrathin films for optics and photonics
WG 6: Nano-size actorics and sensorics

The Working Groups, in which the Center for Microtechnologies is mainly involved, are described shortly in the following:

Advanced CMOS

Structural widths of about 100nm are state-of-the-art in CMOS technology. A reduction down to below 50nm within 10 years, for further miniaturization, is envisaged by the International Technology Roadmap for Semiconductors ITRS (by Semiconductor Industry Association (SIA) and SEMATECH). Along with this trend, higher frequency and reliability are required. This implies novel developments in materials and processes for both the active elements and the interconnect system, including advanced equipment for larger Si-wafer production. High k dielectrics will be applied to ensure further scaling of effective gate oxide thickness. Most present-day interconnect systems are made of contacts (e.g. titanium or cobalt silicide), barrier layers (TiN, TiW), isolating interlayers (SiO_2 and low-k dielectrics like FSG, OSG), interlayer connections and conducting paths (Al-alloys and Copper). Copper with its high conductivity and stability with respect to electromigration has been introduced as conductor material leading to higher frequency and reliability. This requires the availability of suitable barrier layers suppressing interdiffusion and reactions. The barrier layers must not affect the conductivity of the paths remarkably, which requires ultra-thin films. Interfaces and nanometer scale effects become increasingly important.

Head of the Working Group: Prof. Dr. Thomas Gessner
Chemnitz University of Technology

Novel components

The continuing trend towards miniaturization of integrated circuits has given rise to increasing efforts to supplement and gradually replace conventional CMOS-technologies by nanotechnologies and nanoelectronics in near future. The latter include magneto-electronics, and single electron devices, nanocluster storage elements, and resonant tunneling elements, among others.

Head of the Working Group: Prof. Dr. Christian Radehaus
Chemnitz University of Technology

4 Research activities of ZfM in cooperation with the FhG-IZM-branchlab Chemnitz

Fields of research

- Design and fabrication of microelectronical and micromechanical elements and arrays
- ULSI metallization
- High temperature stable metallization
- Analysis of micromechanical systems
- Development and application of design tools and methods for micromechanical components and systems & coupled field analysis
- Coupling of microsystems and instrumentation (mechanical, electrical, thermal and substantial interfaces)
- Function, principles and modelling of electronic devices (test structures, parameter extraction, model building)
- Microelectronic circuit design (read out- and controlling circuits for sensors and actuators)
- MIS – solar cells (manufacturing, analysis, measuring and modelling) & multicristalline solar cells
- Electronics for micro-electromechanical systems (MEMS)
- Development of infrared measurement systems
- Nanoelectronics
- Integrated Optics
- Colour measurement

Subjects of research

- Microfabricated scanner arrays
- Acceleration sensors
- Electostatically driven torsion actuators with one or two DOF
- AIM technology
- High temperature applications of MEMS, e.g. gas sensor for exhaust measurement
- Vibration monitoring based on Si-sensor arrays
- Sensor / actuator systems for high precision scanning with a large vertical range
- Gyroscopes
- Wafer bond techniques / SOI – substrat fabrication / MEMS wafer level packaging
- Simulation of micromechanical and microelectronical components, materials databases
- Design tools for microsystems and microelectronics
- Macromodels for simulation of micromechanical components using PSpice
- Design and fabrication of integrated optical waveguides on silicon
- Fiber-optical communication systems
- Single Electron Tunnelling Technologies
- Colour measurement and sensors
- Orientation dependent etching of silicon: Development of etchants and determination of etch rates, design of etch masks and simulation of etch process, development of new structures by multi-step etch processes
- Geometrical measurement on microstructures
- Plastic deformation of silicon-microstructures
- Copper metallization
- Low k dielectrics
- Equipment and process simulation for microelectronics
- Development of probing equipment for 1/f measurements
- Microwave Device and Circuit Design and Simulation
- Reliability analyses

4.1 Current research projects

BMBF Project „Verbesserung der Performance von IC´s durch Integration von Kupfer und low-k Dielektrika - PERFECT“

Project Manager:	Prof. T. Gessner
Partners:	Infineon Technologies AG Munich, DaimlerChrysler AG Ulm, Dresden University of Technology, University of Hannover
Project duration:	01.11.2000 - 28.02.2004
Project goal:	Application of Copper interconnects for mobile communication IC´s, power devices and micrometer wave devices; Integration of organic low k dielectrics into Copper Damascene metallization

BMBF Project „Modular Optical Analyser System (MOPAL)“

Project manager:	Prof. T. Geßner
Partners:	Endress+Hauser Conducta GmbH & Co. KG, COLOUR CONTROL Farbmesstechnik GmbH, SENTECH GmbH, Micro System Research Center of Chongqing University (VR China)
Project duration:	01. 08. 2004 - 31. 07. 2007
Project goal:	Development and realization of an economical, efficient and universally applicable modular optical miniature analysis system for the spectral range from 300 nm – 10 µm.

BMBF Project "New printing technologies: Development and characterization of technological and electrical parameters for polymer-based printed electronics (PEP)"

Project leader:	Prof. A. Hübler, TU Chemnitz, Lehrstuhl PMT
Partners:	BTU Cottbus; Universität Potsdam
Project duration:	01. 01. 2002 - 31. 12. 2004
Project goal:	Development of high-volume printing technologies and characterization of printed electronic devices.

BMBF Project "Entwicklung von Technologieplattformen von Silizium-Mikrosystemen im Netzwerkverbund (InnoRegio)"

Project leader:	Mr. M. Krusche, AMTEC GmbH Chemnitz
Partners:	GEMAC mbH Chemnitz; FhG-IZM Chemnitz, FhG-IWU Chemnitz
Project duration:	01. 05. 2002 - 30. 06. 2004
Project goal:	Development of technology platforms for silicon microsystems in a regional network.

BMBF Project "Silicon igniter (SilAnz): Preparation of HfH_x-based igniter chips"

Project leader:	Dr. Laucht, TRW Airbag Systems GmbH Aschau/Inn
Partners:	CiS Institut für Mikrosensorik gGmbH Erfurt; Siegert TFT GmbH Hermsdorf; TU München; ZfM-TU Chemnitz
Project duration:	01. 01. 2003 - 31. 01. 2006
Project goal:	The goal of the project is the preparation of HfH_x thin films for igniter chips.

BMBF Project „IPQ (IP Qualification)“

Project manager:	Prof. D. Müller
Project duration:	01.07.2001 - 31.03.2004
Project goal:	The methodologies and tools developed in the project IPQ are targeted on significant improvements in quality assurance in the development and application of Intellectual Property (IP). This includes the development of new methods for IP specification, intelligent IP retrievel, techniques for (semi)-automatic IP adaptation as well as contributions to IP standardisation activities.

BMBF Project "Visualisierung mit halbleiter-basierten RGB Lasern im Automobil- und Consumerbereich - VISULASE"

Project leader:	OSRAM Opto Semiconcuctors GmbH
Partners:	FhG-IZM Chemnitz, ZfM, FhG-IOF Jena, Robert Bosch GmbH, ELOVIS GmbH
Project duration:	01. 10. 2004 - 30. 09. 2007
Project goal:	The goal of the project is the development of a complex micromechanical system for a head-up display in a car.

BMWi Projekt „Optimization of the multicrystalline solar cell process by means of RTP and RIE“

Project manager:	Prof. G. Ebest
Partners:	RWE Schott Solar, Alzenau
Project duration:	01. 04. 2001 – 30. 04. 2004
Project goal:	Proof of rapid thermal processing and reactive ion etching for solar cell fabrication

BMBF Project „Electronic compensation of fabrication tolerances of microsystem products demonstrated for a multi sensor for navigation (EKOFEM)“

Project manager:	Prof. T. Gessner
Partners:	LITEF GmbH Freiburg, GEMAC mbH Chemnitz, FhG IZM, Department Chemnitz
Project duration:	01. 10. 2001 – 31. 12. 2004
Project goal:	Development of electronic compensation methods of fabrication tolerances and their application for a high precision silicon multisensor (acceleration and angular rate measurement)

BMBF Project „Isolation schemes for ultra high RF-circuits“ (Isosurf)

Project manager:	Dr. B. Trui, Atmel Germany GmbH
Partners:	Atmel Germany GmbH, IMS chips Stuttgart, FZ ISG Jülich, FhG IZM Department Chemnitz, TU Ilmenau, TU Ulm
Project duration:	04/2003 – 04/2006
Project goal:	Fabrication of new transistor structures based on SOI-substrates with buried silicides layers

BMBF Project „Design und Technologie für SOI-CMOS Bauelemente mit Gatelängen kleiner 50nm (MOSTEDE)”

Project manager:	Prof. C. Radehaus
Partners:	AMD Saxony, HTW Dresden
Project duration:	01. 04. 2004 – 31. 03. 2007
Project goal:	Atomic scale modelling of new dielectrics for CMOS technologies

SMWA Project „Mikroelektronisches Zündelement für Insassen - Sicherheitssysteme“

Project manager:	Prof. T. Gessner
Partners:	Flexiva automation & Anlagenbau GmbH, Amtsberg; Fahrzeugelektrik Pirna GmbH
Project duration:	01.10. 2003 – 31.12. 2004
Project goal:	Development of a new airbag igniter

SMWA Project „Modular measurement system consisting of a tunable FPI and IR sensor - MODUL“

Project manager:	Prof. T. Gessner
Partners:	Infra Tec GmbH Dresden, GEMAC mbH Chemnitz
Project duration:	01.09.2003 – 31.08.2005
Project goal:	Development of layout and technology for a micromachined Fabry-Perot-Interferometer; Fabrication of prototypes

DFG Project „Polymere als low-k Dielektrika für Metallisierungssysteme in der Mikroelektronik“ – Polymers as low-k dielectrics for microelectronic metallization schemes

Project manager:	Prof. T. Gessner
Partners:	Prof. M. Bauer, BTU Cottbus
Project duration:	01.02.2002 – 31.01.2004 01.12.2004 – 30.11.2006
Project goal:	Development and characterization of organic ultra low k material with reduced density; Patterning process development and compatibility with copper interconnect processing.

DFG Project „Heißprägen multifunktionaler Kalibriernormale für bildverarbeitende Mikroskope zum Messen von Mikrosystemen und Nanostrukturen“

Project manager:	Prof. J. Frühauf
Partners:	Prof. E. Reithmeier, Universität Hannover
Project duration:	01.10.2004 – 30.09.2005
Project goal:	Hot pressing of calibration standards

DFG Project „Bestimmung und Optimierung des mechanischen Verhaltens von Schichtstapeln mit porösen low-k-Dielektrika“ – Evaluation and Optimization of mechanical behavior of film stacks containing porous low-k dielectrics

Project manager:	Prof. T. Gessner
Partners:	Prof. F. Richter, Chair Solid-State Physics, Chemnitz University of Technology
Project duration:	01.11.2004 - 31.10.2006
Project goal:	Development of fundamental models and software for mechanical characterization technique based on nanoindentation of porous low-k dielectrics. Correlation with CMP loads on porous materials.

Integrated Project (IST) “NANOCMOS”: CMOS backbone for 2010 e- Europe. From the 45 nm node down to the limits

Project leader:	ST Microelectronics SA (F)
Project manager:	Prof. T. Gessner / Dr. S. E. Schulz
Partners:	Infineon Technologies AG (D), Philips Electronics Nederland B.V. (NL), Philips Semiconductors R&D France (F), Philips Innovative Technology Solutions NV (B), IMEC Leuven (B), ST Microelectronics Srl. (I), CNRS (F), CEA-LETI Grenoble (F), Fraunhofer (D), isiltec GmbH (D), Ion Beam Services (F), Magwell (B), ACIES Europe (F)
Project duration:	01.03.2004 – 31.05.2006
Project goal:	NANOCMOS is a project integrating in a coherent structure, activities that in the past have been the object of ESPRIT/IST, JESSI/MEDEA projects in the field of CMOS technologies. It focuses on the RTD activities necessary to develop the 45nm, 32nm and below CMOS technologies. From these technology nodes it will be mandatory to introduce revolutionary changes in the materials, process modules, device and metallization architectures and all related characterization, test, modelling and simulation technologies, to keep the scaling trends viable and make all future IST applications possible. NANOCMOS covers all these aspects. The first objective of the project is the demonstration of feasibility of Front-End and Back-End process modules of the 45nm node CMOS logic technology. The project intents to process as demonstrator a very aggressive SRAM chip displaying worldwide best characteristics. The second objective of the project is to realize exploratory research on critical issues of the materials, devices, interconnect and related characterization and modelling to start preparing the 32/22 nodes considered to be within the limits of the CMOS technologies. The third objective of the project is to prepare the take up of results described in the Objective I and implement a 45nm Full Logic CMOS Process Integration in 300 mm wafers

by the end of 2007. This integration will be part of a separate MEDEA+ project.

Website: www.nanocmos-eu.com

SEA-Project "ACTION : Advanced CVD tool for integration of organosilicated nanoporous films"

Project manager: Prof. T. Gessner / Dr. S. E. Schulz
Project leader: ST Microelectronics, Crolles (F)
Partners: AMD Saxony LLC & Co KG (D), Philips Res. Leuven (B), LETI Grenoble (F), Sematech (USA), TRIKON Technologies (UK)
Project duration: 01.05.2002 – 31.01.2004
Project goal: Provide organosilicated glass (OSG) material with a k-value of 2.2 for interconnect applications for the 90 nm node; Prove cluster tool for full inter metal dielectric (IMD) stack; Demonstrate flexibility for customized dual-damascene stack architectures; Show Cost-effectiveness compared to multi-tool Spin-on Dielectrics (SOD) methods; Demonstrate performance within a 300 mm production environment. Website: www.sea.rl.ac.uk

AIF Projekt "Entwicklung von Siliziumaktoren mit lasertrimmbaren Feder-Masse-Strukturen"

Project manager: Prof. T. Gessner
Partners: 3D-Micromac AG
Projekt duration: 01.05.2004 - 31.10.2006
Projekt goal: Aim of the collaboration is to investigate achievable accuracy and efficiency as well as developing new laser systems and equipment for in-line laser treatment of MEMS.

EU-Project Intelligent Manufacturing Systems: "Optical Characterisation Methods for MEMS Manufacturing - OCMMM"

Project manager: Prof. T. Gessner
Partners: GF Messtechnik GmbH (GFM), FhG.IWU, University of Twente-MESA, Thales Avionique (TH-AV), Yole Développement (YOLE), LioniX (LION), Warsaw University of Technology (WUT)
Project duration: 01. 01. 2001 – 31. 08. 2004
Project goal: Optical Characterisation Methods for MEMS Manufacturing

Industrial Research Contract „Development of precursors for copper deposition "

Project manager: Prof. T. Gessner, Dr. S. E. Schulz
Partners: BASF Ludwigshafen; Prof. Lang, TU Chemnitz , Chair Inorg. Chemistry
Projekt duration: 01.04.2003 - 31.12.2004
Project goal: Development of precursors and deposition processes for copper.

Industrial Research Contract „Fabrication of multi-use acceleration sensors"

Project manager: Prof. T. Gessner
Partners: Fara New Technologies, Xi´an, China, GEMAC mbH Chemnitz
Project goal: Development of an high precision acceleration sensor system and its fabrication technology; Fabrication of prototypes

Industrial Research Contract „Development of silicon gratings for the assessment of optical and tactile surface measuring instruments"

Project manager: Prof. J. Frühauf
Partners: GEMAC mbH Chemnitz
Project duration: 15. 09. 2003 – 31. 01. 2004
Project goal: Etching of silicon gratings with trapezoidal, triangular, rectangular and arched profiles

Stiftung Industrieforschung : „Kalibrierung von Geräten zur registrierenden Härteprüfung mittels mikrotechnisch gefertigter Si-Federkörper als Kalibriernormale“

Project manager: Prof. Dr. J. Frühauf
Project duration: 01. 10. 2003 – 31. 03. 2005
Project goal: Si force standards

DFG Project „VIVA – Low Power System Bus Encoding“

Project manager: Prof. D. Müller
Project duration: 01.07.1999 - 31.03.2005
Project goal: Development and implementation of coder-decoder systems for SOC system busses which minimize under a set of constraints the total power dissipation on a system bus with its coder and decoder implementation through reduction of switching activity on this bus.

Project „Solutions in the field of color image processing“

Project manager: Prof. D. Müller
Partners: Siemens A&D Nürnberg, Sächsisches Textilforschungsinstitut STFI Chemnitz
Project duration: 01.02.2004 - 30.06.2004
Project goal: Evaluation of new algorithms in the field of image processing by using FPGAs and realtime processing, investigation of color spaces and classification for color image analysis.

Service order No. 5 and 6 for master agreement research and development, entered by AMD and Technische Universität Chemnitz

Project manager: Prof. C. Radehaus
Project duration: 01. 08. 2003 - 30. 09. 2004
Project goal: Automation of the software system GOPI modelling CV-characteristics of gate-oxide-structures – within the framework of the GOPI model – to estimate the parameters

Project: "Entwicklung von Packagingtechnologien für Bauelemente in Oberflächen-technologie"

Project manager: M. Krusche, Amtec GmbH
Partners: FhG IWU, TU Chemnitz, Gemac GmbH, Amtec GmbH
Project duration: 05/2002 – 04/2004
Project goal: MEMS packaging for surface micro machined devices

Project: „Prüf- und Qualitätssicherungssystem für die industrielle Fertigung von wafer-gebondeten Mikrosystemen“ (Mikroprüf)

Project manager: Dr. H. Reinecke, Steag microParts GmbH
Partners: FhG IWM Halle, ZfM - TU Chemnitz, X-Fab GmbH, Robert Bosch GmbH, Hegewald & Peschke Mess- und Prüftechnik GmbH
Project duration: 11/2002 – 10/2005
Project goal: Evaluation of different wafer bond techniques and optimization of wafer bond processes.

4.2 Collaborative Research Center No. 379 : (Sonderforschungsbereich SFB Nr. 379) 01. 01. 1995 – 31. 12. 2006

„Arrays of micromechanical sensors and actuators“

The MEMS research field covers several provinces using different microtechnology methods for the fabrication.
The subject of the SFB deals with the well-defined part of the microsystems research:
“The realization of sensor and actuator arrays consisting of a number of single components”.
Thus, results concerning the behavior and new application fields of the devices would be expected. As a vision of the future it is aimed toward a system which combines the arrays with the electronics by microtechnology integration.
Within the focus of interest are the following topics:

- Micromechanical scanning devices (actuators fabricated in bulk and surface micromachining)
- Use of micromechanical basic components, e.g. for ultrasonic arrays and positioning systems, including the application of new materials
- Optimization of the AIM process flow

The following institutions are working together

Faculty of Electrical Engineering and Information Technology
Chair Microsystems and Precision Engineering, Prof. Dr. Wolfram Dötzel
Chair Electronic Devices, Prof. Dr. Gunter Ebest
Group Material Science, Prof. Dr. Joachim Frühauf
Chair Microtechnology, Prof. Dr. Thomas Gessner
Chair Measurement and Sensor Technology, Prof. Dr. Wolfgang Manthey
Chair Circuit and System Design, Prof. Dr. Dietmar Müller
Chair Opto- & Solid-State Electronics, Prof. Dr. Christian Radehaus

Faculty of Natural Science
Chair Semiconductor Physics, Prof. Dr. Dietrich R. T. Zahn
Chair Solid Surfaces Analysis, Prof. Dr. Michael Hietschold

Faculty of Mechanical Engineering
Institute for Print and Media Technology, Prof. Dr. Arved C. Hübler

Fraunhofer Institute „Reliability and Microintegration“, Branchlab Chemnitz
Head of the Institute: Prof. Dr. Bernd Michel

Institut für Mechatronik e.V. Chemnitz, Prof. Dr. Peter Maißer

Subproject A1: Design of Micromechanical Components

M. Dienel[1], D. Billep[1], W. Kolchuzhin[1], A. Shaporin[1], J. Mehner[2], S. Krönert[1], W. Dötzel[1], J. Frühauf[1]
[1]Chemnitz University of Technology, Faculty of Electrical Engineering and Information Technology
[2]Fraunhofer Institute for Reliability and Microintegration, Department Micro Devices and Equipment

1 Development of accelerometer arrays for drift compensation

Micromechanical accelerometers have a lot of different applications. An upcoming field is inertial measurement, which means the tracking of the position and orientation of moved objects with an attached inertial measurement unit. Its position is calculated by integrating the acceleration twice. That's leading to a rapidly rising error in position calculation, in case of a small offset error in the acceleration signal. The aim of the project is to increase the long time stability of these sensors by a novel redundantly designed sensor array.
The basic idea is the arrangement of at least three similar accelerometers as an array in a Silicon chip. The sensors must have different measuring directions that are non-orthogonally aligned. The drift effects in time and temperature are eliminated by calculation of the resulting acceleration, assuming equal influence on every sensor.
The ageing and temperature changes lead to alterations in material stresses and strains which results in variations in the measured acceleration. Hence, a sensor and chip design is needed which provides similar effects on every sensor.

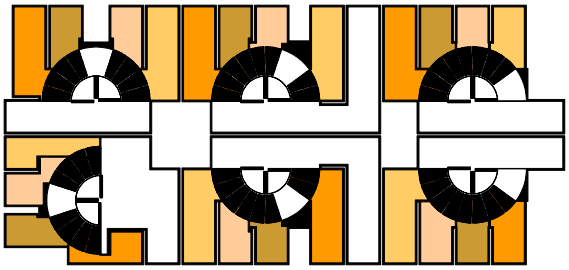


Figure 1: Acceleration sensor chip (similar colours corresponding to similar electrode properties)

Six redundant accelerometers [Fig. 1] are situated on a chip while five are non-orthogonally aligned [1]. Every sensor has one of six possible measuring directions.
The sensor forms a semicircle as shown in Fig. 2. At the outer radius a seismic mass and four capacitive comb segments are affixed. To vary measuring direction the positions of the seismic mass and a comb segment have to be swapped. The advantages are the centred anchor which results in less stress entry and the springs are similarly aligned in respect to crystal orientation for each sensor in the whole chip.

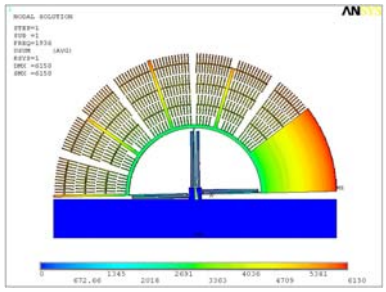


Figure 2: Simulation model of the sensor (1st Eigenmode)

First samples are fabricated in a BDRIE process [2], which provides high aspect ratio combined with high freedom in design [Fig. 3]. The transfer of the design to AIM technology [3] is in progress.

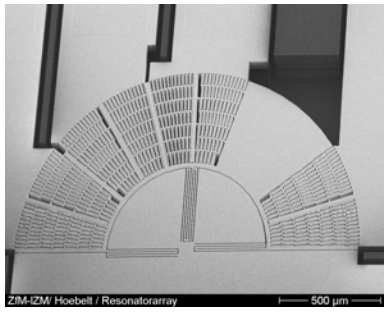


Figure 3: Sensor with seismic mass at 36° position [2]

2 Multiparametric Method Based on FEM for MEMS Electrostatic Problems

Nowadays Finite Element Method (FEM) is used at main CAD for MEMS design. FEM combines high accuracy of the solution, high solution speed, plentiful opportunities in a choice of geometry of a problem and boundary conditions. search of the optimum parameter combinations, are strongly required.

This work is concentrate on a novel technique, based on FEM, which account for parameter variations in a one finite element run. The method flow chart is shown in Fig. 4. As result one can obtain the Taylor vectors of the goal function covering the system response in the vicinity of the initial position with regard to design parameters [5].

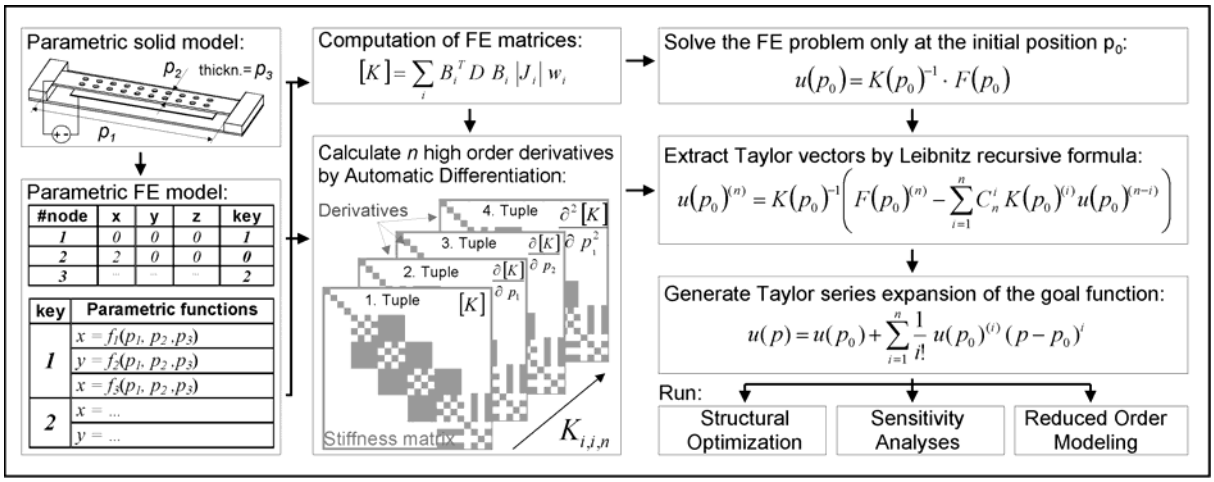


Figure 4: General approach of parametric model extraction for MEMS based on finite element methods.

The parametric models of complex MEMS devices are extracted by numerical data sampling and subsequent function fit algorithms. Each sample point must be obtained by a separate finite element run whereby the change of geometrical dimensions is realized by mesh morphing or re-mesh functionality. Usually one needs between several ten to some hundreds of sample data in order to capture the influence of design parameters accurately which is cumbersome for practical use [4]. Therefore, novel simulation techniques, combining, on the one hand, advantages of FEM and an opportunity to get the solution in analytic form, suitable for

Typical MEMS element – a comb-drive cell (Fig. 5.), was analyzed by this method [6]. The capacity of this structure depending on shift (Δl, Δt, Δh) of the movable electrode in the direction along main axes was obtained. Results of the simulation are shown in Fig. 6.

This method gives an opportunity of getting the results close enough to ones of reference finite element solution. Problem time weakly depends on an amount of variable parameters that gives advantage at work with multiparametric models. This method can be used as a part of ROM tool and as independent tool for structural optimization and sensitivity analysis.

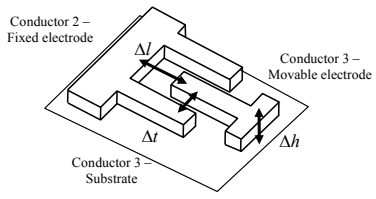


Figure 5: Model of comb drive cell

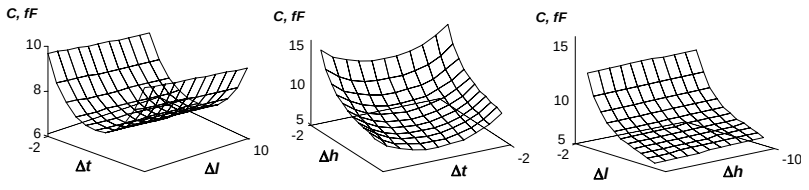
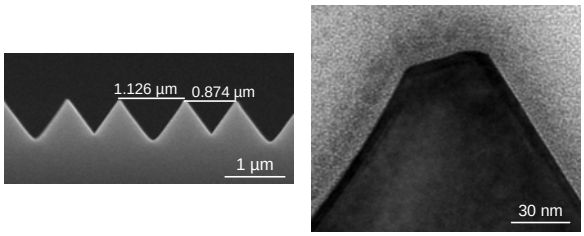


Figure 6: Simulation results.

3 Silicon form elements

3.1 Triangle gratings

The etching of Echelette gratings with a period of 1 µm starting with a mask pattern of 2 µm period and using an interim oxidation is described in the Annual Report 2003, p. 54 and p. 69. Because of this interim oxidation (silicon is consumed) the original windows are widened. Furthermore the oxide reaches into the interface between the nitride and the silicon ("birds beak" effect) diminishing the width of the secondly etched grooves. This technique results in different widths of neighboured grooves fig. 1a. Additionally the "birds beak" effect flats the convex edges of the grating, fig. 7b.



a) Different width of neighboured grooves *b) "birds beak" effect*

Figure 7: Pictures of gratings

The proposed solution to overcome this problem must accept the original period of the mask pattern on expensive {112}-Si wafers. Therefore an alternative solution was tested to produce the halfed period, fig 8. The tests were performed using cheap {100}-Si wafers and mask patterns having different periods (1.6; 2; 4; 5 µm).

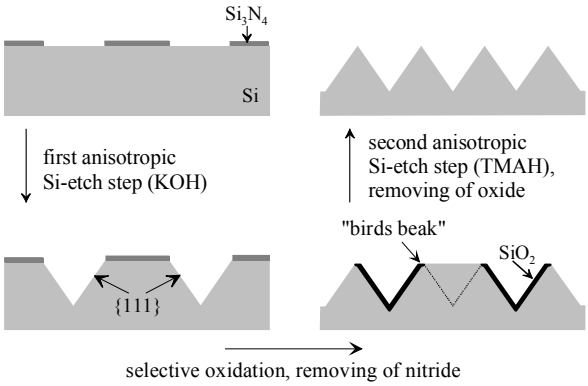
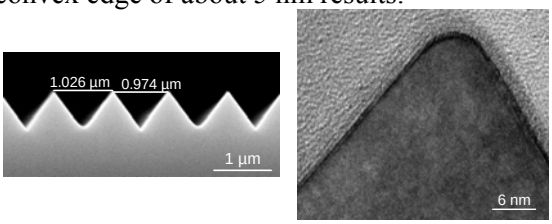


Figure 8: Scheme of preparation

Because TMAH has a lower selectivity and therefore a higher etch rate of the {111}-sidewalls the horizontal differences between two neighboured V-grooves can be adjusted up to ≤ 50 nm by using of TMAH in the second etch step, fig 9a. Furthermore the "birds beak" effect is removed, fig 9b. A very small radius of the convex edge of about 5 nm results.



a) Deviation of the width of the grooves is ≤ 50 nm *b) Convex edge without "birds beak" effect*

Figure 9: Pictures of gratings with improved features

3.2 Silicon solid hinge guide

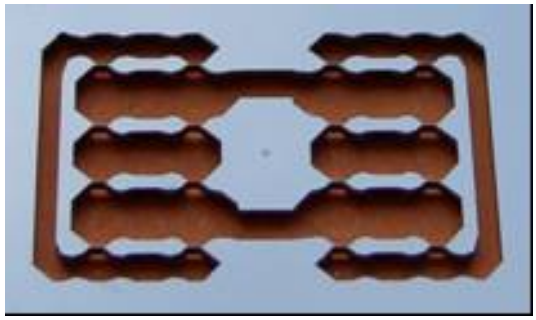


Figure 10: Solid hinge guide out of Si

A solid hinge guide is completely prepared out of silicon by wet anisotropic etching, fig. 10, as a development of the demonstrator in the Annual Report 2003. Using silicon wafers with a thickness of 1120 µm and etching the springs down to a thickness of 30 µm, the guide can be deflected up to ± 1.5 mm, fig 11.

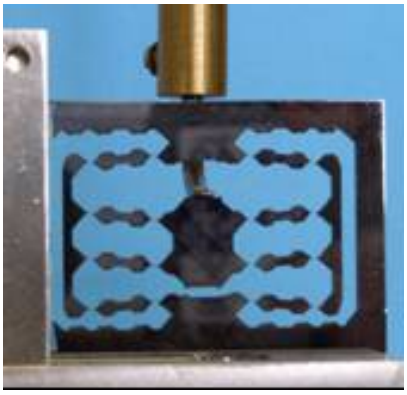


Figure 11: Solid hinge guide deflected up to 1 mm

The transverse stiffness and the in-plane deflection of the solid hinge guide were

controlled. The measurements of the straightness (y-deviation from the translation axis x) using a laser scanning instrument show values in the region of 0.5 microns. This can be improved by a more optimal driving actor.

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[3] Bertz, A.; et al. : *A novel high aspect ration technology for MEMS fabrication using standard silicon wafers*. Sensors and Actuators A 97-98 (2002) pp 691-701.

[4] J. E. Mehner, F. Bennini, W. Dötzel: *CAD for Microelectromechanical Systems, System Design Automation - Fundamentals, Principles, Methods, Examples.* Kluwer Academic Publ., pp. 111-132, 2000.

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Subproject A2: Examination of the Applicability of SystemC-AMS for the Description of MEMS

Markert, Erik; Schlegel, Michael; Herrmann, Göran; Müller, Dietmar
TU Chemnitz, Faculty of Electrical Engineering and Information Technology,
Professorship Circuit and System Design
e-mail: erik.markert@etit.tu-chemnitz.de

1 Introduction

SystemC [1] provides elaborate methods for the description of digital hardware/software systems from functional downto register-transfer level. But today's systems usually also contain analog parts, they are heterogeneous. So an extension of the language as well as of the Models of Computation (MoC) is necessary. A SystemC Study Group currently develops the analog SystemC extension library SystemC-AMS. Now a first version is released by Fraunhofer Gesellschaft EAS/IIS Dresden, including the algorithms planned for phase 1 of the White Paper [2], [3]. Scope of application of this version are communication systems.
This paper discusses whether this version is already qualified for the description of MEMS although this is still planned by SystemC-AMS developers for future versions.
With SystemC-AMS 0.12, a vibration sensor array shall be described. In VHDL-AMS already exists a verified model and was presented in the last Annual Report [4]. There a brief system description can be found.

2 Modeling with SystemC-AMS

In the used SystemC-AMS version two possibilities for describing analog parts exist: conservative networks and static dataflow (SDF) networks.
The single elements of SDF networks communicate via directed data streams. All ports are to be declared as inputs or outputs. In the present version, all feedbacks have to be decoupled by a delay component. Communication systems are usually strong oversampled so on this field of application the delay does not provoke a significant error. It is to be explored if this will be the case in MEMS Design. For the description of transfer functions and differential equations, Laplace Transfer Functions can be used.
Beside SDF-modeling, simple conservative networks may also be described. They can consist of R, L, C, current and voltage sources. For connection to SDF networks, SDF-signal-driven sources and voltmeter may be used.
Mixed forms with digital SystemC 2.0 and hierarchical dispositions are possible.

3 Implementation

3.1 Overall System

SystemC-AMS is an extension of SystemC and therewith of C++, too. So only digital components can be described in SystemC. There the use of edge-sensitive processes offers a gain of simulation time and description effort.
Therefore in the vibration sensor array the fuzzy-pattern-classifier is described using digital SystemC while sensor and selector are pure analog SystemC-AMS components. Hierarchical modules are used for detector and microcontroller. Figure 1 shows the system architecture. In the following the analog module sensor is specified to show the new capabilities of SystemC-AMS.

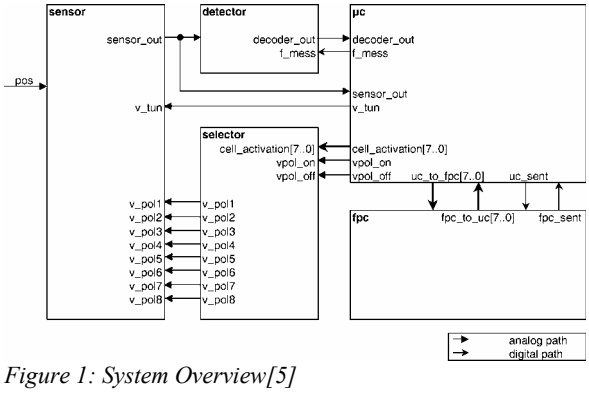

Figure 1: System Overview[5]

3.2 Module Sensor

The sensor converts mechanical signals to electrical ones. For this purpose, it includes a number of spring-mass-resonators which may be activated seperately. The output u_out (SDF-type double) provides a voltage for the following component.

In the used version of SystemC-AMS, it was impossible to describe user-specific conservative behaviour models. This is planned for one of the next language versions. Currently, only linear conservative behaviour in terms of the basic elements resistor, capacitor and inductivity is implementable. By using of C++-heredity other domains can be derivated.
The sensor consists of springs, masses and damps. These mechanical elements (v, F, k, m, c) are converted to electrical values (U, I, L, C, R). The sensor's input is a displacement. But in analogy, the current conforms to the velocity so the input signal must be derivated. The component sensor is structured as shown in figure 2.

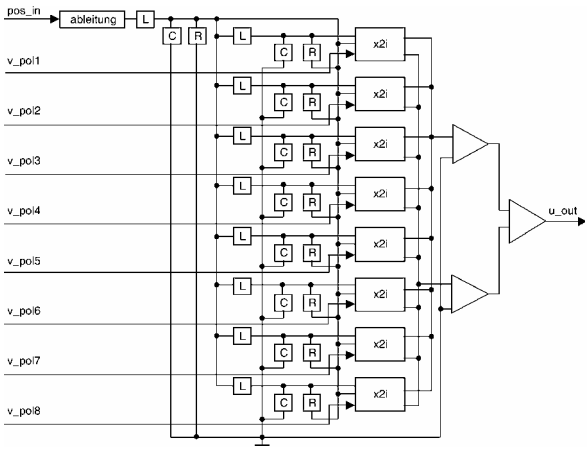

Figure 2: Structure of Sensor Module [5]

Listing 1 shows the description of a spring-mass-attenuator-component in SystemC-AMS.

```
ELSDF_MODULE(fmd) {
  // ----- ports -----
  elec_port in;
  elec_port out;
  elec_port gnd;
  sdf_inport<double> v_tun; //not used
  // ------ parameter ------
  sdf_para<double> m,d,k;
  // ----- components -----
  R* r1; L* l1; C* c1;
  // ----- constructor -----
  ELSDF_CTOR(fmd)
  {
    l1 = new L(this->k); //spring
    l1->a(pos_m);
    l1->b(pos_in);
    c1 = new C(this->m); //mass
    c1->a(pos_m);
    c1->b(gndm);
    r1 = new R(this->d); //attenuator
    r1->a(pos_m);
    r1->b(pos_in);
  };
};
```

Listing 1: Description of a part of the sensor module

4 Simulation Results

For result valuation, it is important to point out again that the used SystemC-AMS version is made for communication systems only, micromechanical problems will be supported in a future version.
Figures 3 and 4 show the voltage at sensor output in SystemC-AMS and VHDL-AMS. Input waveform is a step, all simulation parameters are identical (step height 1 µm, step width 10 ns, integration algorithm trapezoidal).

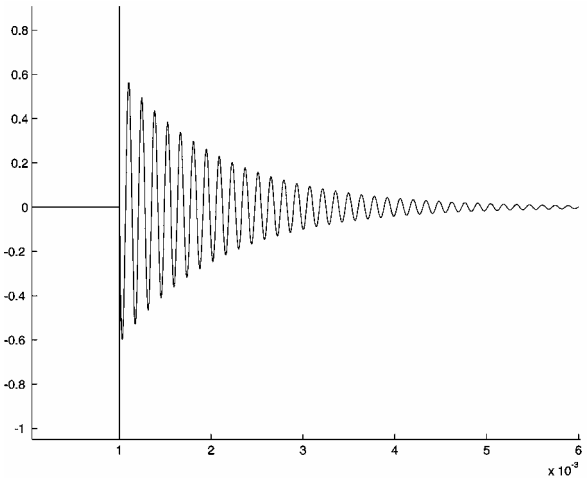

Figure 3: Step response in SystemC-AMS

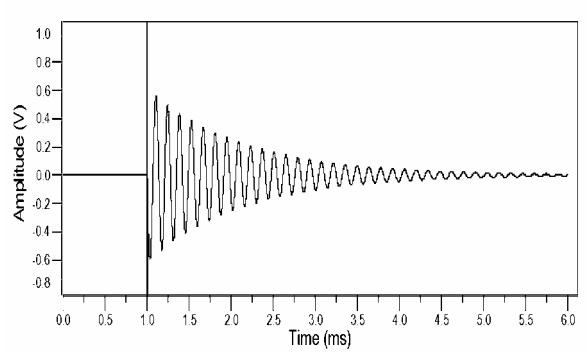

Figure 4: Step response in VHDL-AMS

Both pictures show similar behaviour. But the oscillation amplitudes differ up to 2 %. Reason for this deviation is the one cycle delay in the derivation component in the SystemC-AMS description while VHDL-AMS solves the non-linear equation system. The SystemC-AMS-implementation claims much lesser calculation time (2 min 24 s) than VHDL-AMS (24 min 2 s) on a SunBlade 2900.

The result of the digital fuzzy-pattern-classification is nearly the same. Table 1 shows the affiliation to the attribute classes.

Table 1: classification results

	VHDL-AMS	SystemC-AMS	Δ
Class 1	0.0070686	0.0070696	0.01 %
Class 2	0.0344848	0.0345094	0.07 %
Time	59 min 5 s	8 min 23 s	

Differences between simulation results are negligible small.

5 Conclusion

In this paper the modeling of a vibration sensor array in SystemC-AMS was presented. Field of application of this language's first version are communication systems, but as shown in this paper the language already can be used for MEMS simulation.
The SystemC-AMS simulation results differ only a little from the VHDL-AMS simulation. If further solvers [3] will be included then this gap will diminish. The calculation time is obviously reduced. The results for system-level simulation are identical.
SystemC-AMS offers support for all SystemC- and C++-language elements and concepts. So it is easy to describe digital components with only few description effort. Additionally, software parts can be included directly. The modeling of analog behaviour is still target of language development. At the moment the description effort for MEMS is higher than in VHDL-AMS.

6 References

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Subproject A4: Multiple band sensor arrays for vibration monitoring based on near-surface silicon bulk micromechanics

Scheibner, Dirk[1]; Frömel, Jörg[2]; Mehner, Jan[2] ; Ebest, Gunter[1]; Gessner, Thomas[1]
[1] Chemnitz University of Technology
[2] Fraunhofer-IZM Chemnitz, Department MD & E

1 Introduction

Vibration monitoring has become an important means for wear state recognition of industrial machinery such as cutting tools, bearings, gears, pumps or engines [1]. The majority of mechanical vibration used to identify the wear state is found in the frequency range from a few Hertz to 10 kHz. Currently, piezoelectric wide band transducers combined with signal analysers are usually used to obtain the spectrum. Due to high costs permanent monitoring is limited to extremely expensive machinery or safety related applications.
For the characterisation of the wear state the observation of a few spectral lines is usually sufficient. This fact suggests a narrow band resonance operation of the sensor structure. It amplifies the vibration signal in a small band around its resonance und eliminates other spectral ranges. Advantages of this frequency selective approach are the improvement of the signal-to-noise ratio and simplifications in the signal conditioning circuitry without Fourier transformation. The fixed resonance of such sensors limits their use to applications with well known and constant measurement frequencies. To overcome this restriction, resonance tuning mechanisms are used.
We develop a vibration measurement system based on micromechanical tunable resonators. As sensor structure, a SCREAM- (Single Crystal Reactive Etching And Metallization) [2] fabricated array of tunable resonators is used. Resonance tuning is achieved by electrostatic softening.

2 Frequency Selective Principle

Vibration sensors usually work as wide band transducers far below their resonance. In this frequency range the sensor output is proportional to the acceleration acting on the sensor. In contrast to this common principle, frequency selective sensors operate directly at their resonance. A small band of the incoming spectrum is amplified at the resonance peak of the sensor structure (Fig. 1). Other spectral ranges are suppressed.

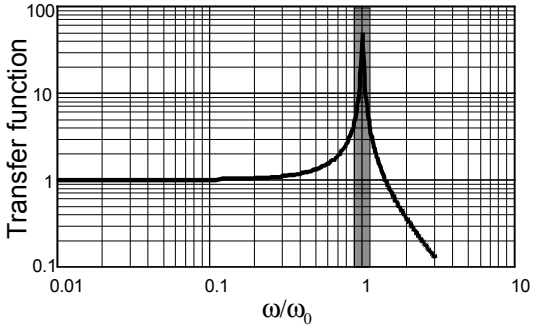

Fig. 1: Frequency selective principle

Advantages of the frequency selective principle are the direct extraction of spectral information without Fourier transformation and the improvement of the signal-to-noise ratio by the quality factor. Furthermore, such a sensor is insensitive to large interfering signals that would overdrive wide band transducers.

3 Resonance Frequency Tuning

Resonance frequency tuning is used to extend the measurement range of a frequency selective sensor.
The structures presented in this paper implement electrostatic softening to vary the resonance frequency. The principle is based on electrostatically generated, amplitude dependent forces acting on the seismic mass (Fig. 2). The total stiffness k_{total} of the tuned resonator is calculated as follows:

$$k_{total} = k_0 - \frac{V_{tun}^{\ 2}}{2}\frac{d^2C(x)}{dx^2} \qquad (1)$$

(V_{tun} - tuning voltage, k_0 - mechanical stiffness, C - total capacitance between stator and seismic mass).

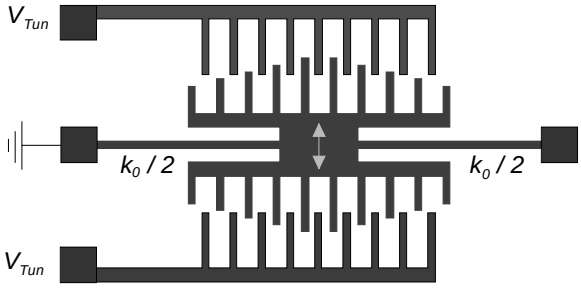

Fig. 2: Scheme of a resonator tuned by electrostatic softening

The forces lead to a softening of the system and therewith to a lowering of the resonance frequency. In this way the resonance frequency and thus the sensitive frequency band are set by a control voltage V_{tun}. To achieve linear sensor characteristics it is essential that the second derivative of the capacitance function $d^2C(x)/dx^2$ is constant over the amplitude range. Otherwise the resonance frequency depends on the signal amplitude. Such nonlinearities implicate large amplitude errors. A quadratic capacitance function implemented by a comb system of linearly varied finger-length using Poly-Si technology is described in [3]. A SCREAM-technology compatible approach using non-overlapping comb fingers is presented in [4].

4 Sensor Structure

The SCREAM-fabricated sensor structures consist of a laterally movable mass supported by four folded flexures. Two different comb systems at the seismic mass are designed either for capacitive signal detection (const. $dC(x)/dx$) or for resonance frequency tuning (const. $d^2C(x)/dx^2$) (Fig.3).

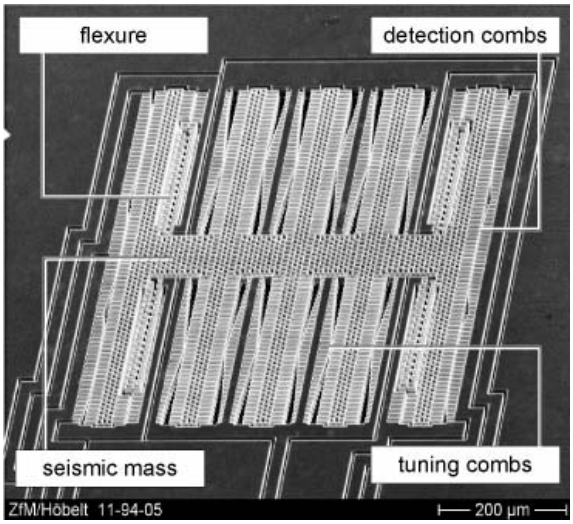

Fig. 3: SEM-view of a resonator structure

The tuning range of a single tunable resonator is limited by the maximum tuning voltage. By grouping eight resonators with stepped base frequencies and overlapping tuning ranges into an array, the frequency range covers 1..10 kHz (Fig. 4).

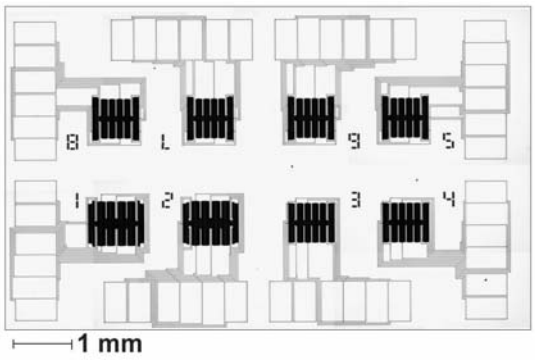

Fig. 4: Tunable resonator array

Damping effects are reduced by providing a low ambient pressure with hermetic sealing of the sensor structure using glass-frit bonding (Fig. 5).

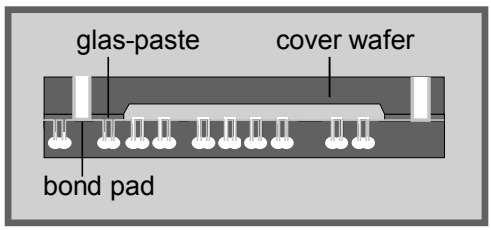

Fig. 5: Hermetic sealing by glas-frit bonding

For a successful use of the sensor it is necessary to protect the microstructure against ambient influences. This is necessary because the structure is damageable to particles and moisture. The protection and the provision of the low pressure are done at the same process step. For this purpose a glass-frit material is used. This material is deposited on a cover wafer with a screen printing process. This allows the creation of frame-like structures around the sensors. The cover wafer has etched contact holes for the electrical contact of the sensor.

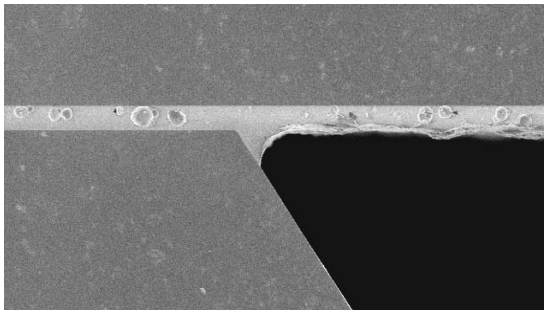

Fig. 6: Joint between silicon wafers using glass frit

To create a firm bond between the sensor wafer and the cover wafer the two wafers are pressed together and heat is applied to them. The heat melts the glass material. The melted glass joins both wafers and the encapsulated cavities hold the same pressure that is applied in that moment in the process chamber. Control of that pressure allows the adjustment of the correct pressure for low damping effects. Fig. 6 shows a SEM picture of a typical joint between silicon wafers using glass frit material.

5 Measurement System

The measurement system contains the micromechanical structure, analog, digital control -and interface (Fig. 7). For low backlash to the object to be measured, the mass of the connected part has to minimized. Therefore a miniaturized system is under development.

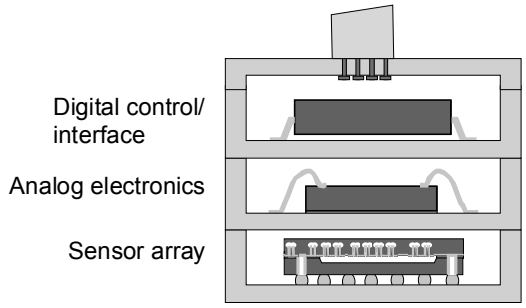

Fig. 7: Scheme of the miniaturized measurement system

6 Conclusions

SCREAM-fabricated resonators are suitable for frequency selective vibration measurements. Electrostatic softening turned out to be an appropriate means for resonance frequency tuning for the range from 1 to 10kHz.
Further work includes a characterization of the fabricated structures. Important aspects are bandwidth, resonance tuning effect and linearity of the resonators. Based on the micromechanical structure, a miniaturized vibration measurement system will be developed and tested in industrial environment.

7 Acknowledgements

The work is done within the Collaborative Research Center SFB 379 which is funded by the German Research Association (DFG).

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Subproject B2: Experimental characterization, modell adaption and reliability: "On the search of charges in MEMS"

Doetzel, Wolfram[1] ; Michel, Bernd[2]
[1]TU Chemnitz, Fakultät für Elektrotechnik und Informationstechnik, Professur für Mikrosystem- und Gerätetechnik
[2] FhG-IZM Berlin, Abteilung MR & MM

1 Introduction

At the characterization of a micro electro mechanical system (MEMS) a plenty of parameters has to be determined. Aside from the geometry and the surface properties like warp and roughness the electro mechanical characteristics are very important technical features. Thereby it could be observed that the presence of charges strongly influences the static deflection and the dynamic behavior of capacitive sensors or actuators [1, 2, 3]. An example to illustrate this effect is the acceleration sensor shown in Fig. 1. The aluminum electrodes are placed on glass wafers. A single crystalline silicon wafer is used to realize the seismic mass and its supporting bending beams. While assembling the wafers by an anodic bonding process voltages up to 400 V have to be applied. The consequential electrostatic force deflects the seismic mass towards the opposite electrode until it hits. To prevent sticking and an electrical short circuit spacers are deposited on both sides of the seismic mass. Because the spacers have to be dielectric materials they carry charges deposited during the bonding process for a very long time. One important property of the acceleration sensor is the static deflection curve. It is obtained by applying a voltage on one capacitor and measuring the capacitance of the opposite capacitor. The same measurement is performed the other way round. The two obtained curves are given in the C-V plot of Fig. 2. They are shifted towards higher voltages. These offset voltages typically are caused by the presence of charges within the sensor. If the charge density changes the static deflection is changing too. Consequently, the characteristic of the acceleration sensor is influenced by charges.
To investigate the behavior of charges in MEMS devices it is necessary to characterize the charge distribution on a sample surface. The information is obtained by measuring the surface potential or the capacitance. Therefore different methods are applicable. For instance Kelvin probe force microscopy [4, 5], electrostatic force microscopy [6] and force microscopy [7] are used to measure the surface potential and capacitance distribution. An overview about electrometers and electrostatic fieldmeters developed at the University of California, Berkley is given in Riehls dissertation [8].

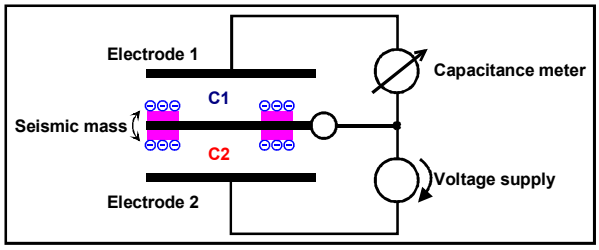

Fig. 1: Characterization of the acceleration sensor

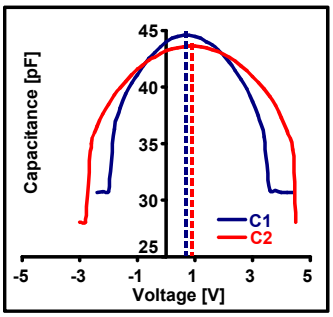

Fig. 2: C-V plot of the sensor

At the Chemnitz University of Technology an electrostatic field sensor was developed that measures the surface potential and the topography simultaneously. The acquisition of the topography enables to control the distance between sensor and sample so that its influence becomes negligible. Compared to the techniques mentioned in [4-7] the realized setup has a very large scan range of some 10 mm^2 which is essentially for the planed investigations. The in-plane resolution is about 50 µm.

2 Sensor and function principle

To characterize the behaviour of charges on dielectric layers in the region of driving or sensing electrodes of capacitive MEMS a measurement technique was developed that is related to the Kelvin method. This means, the effect of the charge induced surface potential is compensated. Fig. 3 shows a scheme of the realized electrostatic field sensor. The micromechanical part is a cantilever-like bending beam with a cubic tip. Its lower surface is the sensing area. A sinusoidal voltage with the frequency ω and an adjustable offset voltage is applied between the cantilever and the sample. The resulting electrostatic force leads to an oscillation of the beam tip that is recorded by a Laser Doppler interferometer.

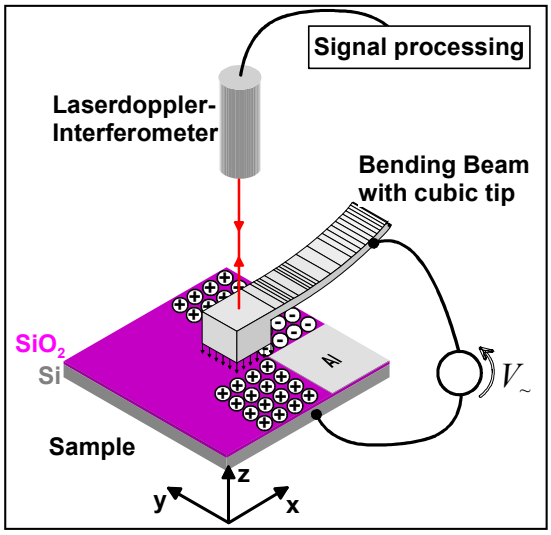

Fig. 3: Scheme of the electrostatic field sensor

The calculation of the electrostatic force on the sensing area will be described using the simplified model of a plate capacitor with a dielectric layer or layer stack on one electrode as shown in Fig. 4.

In assumption of a homogeneous field within the capacitor without interactions with the surroundings the arrangement is electrical neutral, e. g.:

$$\sigma_1 + \sigma_2 + \sigma_P = 0 \qquad (1)$$

Furthermore the Kirchhoff's law is valid and the applied voltage divides into:

$$V_{\sim} = E_1 \cdot d_1 + E_d \cdot d_d \qquad (2)$$

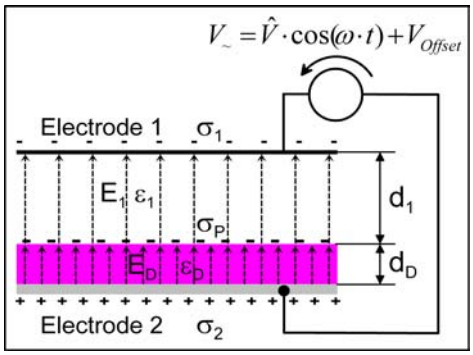

Fig. 4: Simplified model of a plate capacitor

Using (1) and (2) and the usually used equations to calculate electrostatic forces (3) the resulting force on electrode 1 and the sensing area, respectively can be described using equation (4).

$$dF = -\frac{E_1 \cdot dQ_1}{2} \qquad (3)$$

$$F = \varepsilon_0 \cdot \varepsilon_1 \cdot E_1^2 \cdot A$$

with A … the area of the electrode 1

$$F = \frac{\varepsilon_0 \cdot \varepsilon_1 \cdot A}{2 \cdot (\frac{d_D \cdot \varepsilon_1}{\varepsilon_D} + d_1)^2} \cdot [\frac{\hat{V}^2}{2} \cdot (1 + \cos(2 \cdot \omega \cdot t))$$

$$+ 2 \cdot \hat{V} \cdot V_{Offset} \cdot \cos(\omega \cdot t) + 2 \cdot \hat{V} \cdot \frac{d_D \cdot \sigma_P}{\varepsilon_0 \cdot \varepsilon_D} \cdot \cos(\omega \cdot t) \qquad (4)$$

$$+ V_{Offset}^2 + (\frac{d_D \cdot \sigma_P}{\varepsilon_0 \cdot \varepsilon_D})^2 + 2 \cdot V_{Offset} \cdot \frac{d_D \cdot \sigma_P}{\varepsilon_0 \cdot \varepsilon_D}]$$

Because of the linear spring stiffness of the bending beam the motion of the tip of the beam is proportional with the stimulating electrostatic force. Consequently it will deflect statically and dynamically at the frequencies ω and 2ω. On the condition that the applied offset voltage V_{Offset} is equal to $-\frac{d_D \cdot \sigma_P}{\varepsilon_0 \cdot \varepsilon_D}$ the equation to calculate the electrostatic force on electrode 1 reduces to:

$$F = \frac{\varepsilon_0 \cdot \varepsilon_1 \cdot A}{2 \cdot (\frac{d_D \cdot \varepsilon_1}{\varepsilon_D} + d_1)^2} \cdot \frac{\hat{V}^2}{2} \cdot (1 + \cos(2 \cdot \omega \cdot t)) \qquad (5).$$

It is to be seen that the tip of the beam oscillates only at the frequency 2ω. The amplitude at this frequency depends on d_1 and it is used to control the distance between the tip and the sample. Consequently the surface topology is taken into consideration. The applied offset voltage is equal to the surface potential. Furthermore it can be used to calculate the charge density on top of the isolation but therefore the parameters of the dielectric layer like thickness and dielectric constant has to be known (6).

$$\sigma_P = -\frac{V_{Offset} \cdot \varepsilon_0 \cdot \varepsilon_D}{d_D} \qquad (6)$$

3 Results

The samples used for the investigations are similar to MEMS structures. That means, the assembly of silicon, dielectric layer or layer stacks and metal layer is like that of driving or sensing electrodes. The sample shown in Fig. 5 consists of silicon with a 300 nm thermally grown silicon dioxide layer. On top of the dielectric a sputtered aluminum layer is deposited. The experiments are done as follows. The Si-SiO_2-Al capacitor is charged by applying a DC-voltage between silicon and aluminum for some seconds. After that, the potential of the aluminum layer is left free and the surface potential distribution on the Al and the adjacent SiO_2 was measured using the micromechanical electrostatic field sensor.

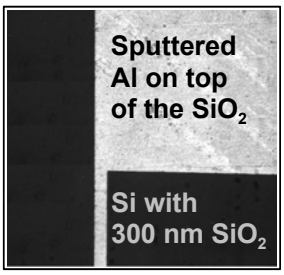

Fig. 5: Sample top view

The measurement results shown in Fig. 6 are obtained after charging the aluminum at +12 V. Fig. 6a is the surface potential distribution of the sample measured immediately after the charging procedure. The potential of the aluminum is +12 V. This is caused by the free charge carrier of the aluminum and the large Si-SiO_2-Al capacitance compared to the capacitance generated by the sensing area of the cantilever and the sample. The adjacent silicon dioxide has a surface potential of about -0.7 V which is a result of experiments performed some weeks before. After 24 hours the measurement was repeated (Fig. 6b). The obtained result strongly differs from the previous one (Fig. 6a). The extracted line scans in Fig. 6c illustrate this change. Depending on time the surface potential on the aluminum decreases while it increases on the adjacent silicon dioxide.

Immediately after performing the measurement shown in Fig. 6b the aluminum was charged at -12 V. The same area of the sample was scanned as before and the results are given in Fig. 7. The surface potential distribution measured 20 minutes after the charging process (Fig. 7a and 7c) shows a rapid discharge of the aluminum to ca. 8.5 V. The results on the silicon dioxide are comparable to those of the last measurement in Fig. 6c (after 24 h). Fig. 7b shows the surface potential distribution after 24 hours. As in the previous experiment, the result strongly differs from that given in Fig. 7a. Fig. 7c shows that the change occurs faster than in the previous measurement (Fig. 6c).

The measurement results show a strong change of the surface potential distribution and consequently of the charge distribution after 24 hours. This can be explained by existence of a thin water film on top of the sample caused by the air humidity. It enables the charge carrier movability on the silicon dioxide surface for in-plane motion. Another reason is the ionization of the adjacent air and deposition of the ions and electrons on the sample. Within the continuation of the experiments the influence of climatic factors e. g. light, temperature and air humidity will be investigated.

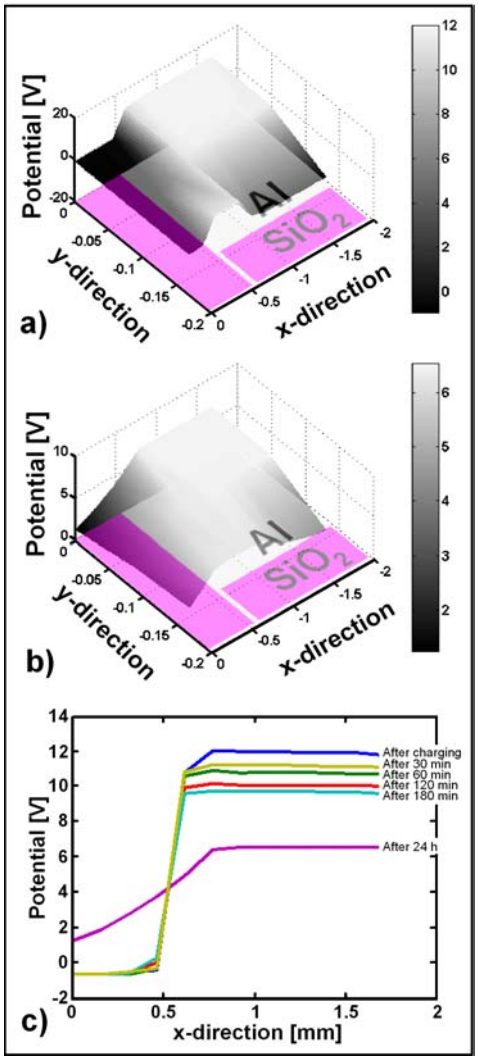

Fig. 6: Measured surface potential distribution after charging the Al at +12 V, a) immediately after charging, b) 24 h later, c) extracted line scan at different times after charging

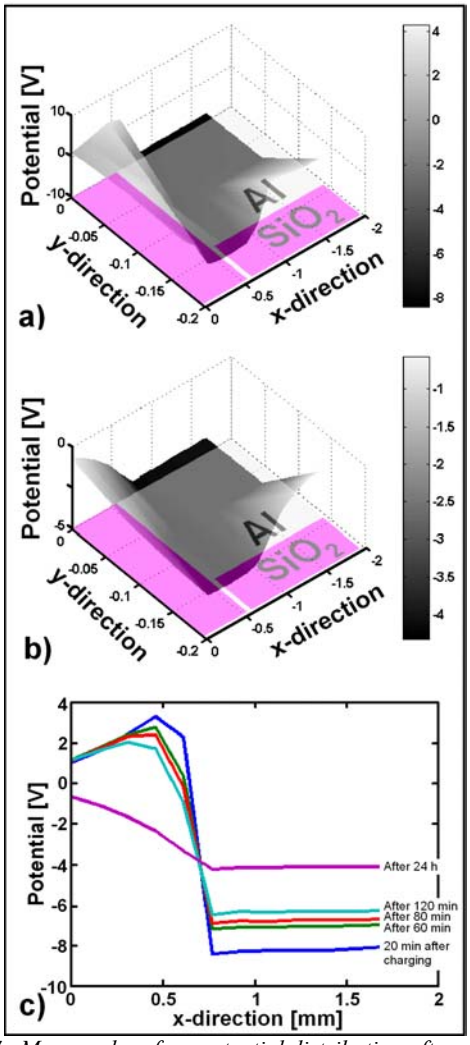

Fig. 7: Measured surface potential distribution after charging the Al at -12 V, a) 20 min after charging, b) 24 h later, c) extracted line scan at different times after charging

4 Summary

The presence of charges strongly influences the characteristics of capacitive MEMS devices. If the charge density changes the static deflection and the dynamic behavior of the sensor or actuator are changing too. Consequently, it is very important to investigate the behavior of charges in MEMS devices to derive rules for the design and fabrication process. The presented micromechanical electrostatic field sensor is used to measure the surface potential distribution which is significant for the charge density. The presented results show the practicability of this sensing technique. It could be demonstrated that after charging a sample the surface potential distribution changes depending on time. Investigations about the influence of climatic factors and the patterning of the dielectric layer are subject of the future work.

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Subproject B5: Development of a Spectral Imaging Technology Based on Microactuators with a Diffraction Grating

Flaspöhler, Martin[1]; Hübler, Arved Carl[1]; Kuhn, Michael[2]; Kaufmann, Christian[2]
[1]TU Chemnitz, Faculty of Mechanical Engineering, Institute for Print and Media Technology
[2] TU Chemnitz, Center for Microtechnologies

1 Introduction

The accurate colour reproduction of an arbitrary original is a common problem in pre-press and the following printing process. The first important part in this workflow is the digitising of the original. The use of state-of-the-art RGB-based image capturing systems, however, is not sufficient for every application. Due to the known theoretical limitations of RGB-techniques, multispectral and spectral methods of image capturing using more than three colour channels have been introduced in the recent years.
Chemnitz University of Technology has presented one of these spectral imaging systems using an oscillating micro mirror with a diffraction grating [1, 2], where each pixel of an original image is recorded in a spectroscopic way. Because of the high oscillation frequency of the micro mirror, very high light intensities are needed. The aluminium layer of the mirror absorbs about 10 % of the incoming light intensity leading to a heating of the mirror surface. To solve this problem, the reflective grating will be replaced by a transmission grating. Therewith absorption losses should not occur, allowing the use of higher light intensities compared to a reflective mirror.

2 Optical design of the grating

The transmission grating will be realised with standard technologies of micro technologies. Therefore it is necessary to find materials which are transparent in the visible part of the electromagnetic radiation and can be structured using lithographic techniques. This leads to very thin layers of silicon dioxide or silicon nitride.
Besides the properties of the layers, the correct grating parameters are also very important. As silicon dioxide and silicon nitride will be used to realise the grating, it is only possible to create rectangular gratings. For this type of grating the main parameters are the grating period and the depth of the grooves. Considering the earlier results with the previous reflection gratings, the final transmission gratings must have a grating period of 1.6 µm. The optimal depth of the grooves depends on the refractive index of the used grating material and the so-called blaze wavelength. Figure 1 shows the calculated optimal groove depth depending on the refractive index of the used material.

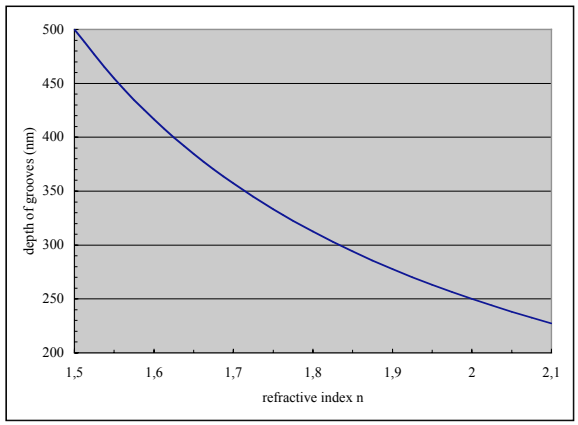

Fig 1: Optimal depth of the grooves versus the refractive index for a blaze wavelength of 500 nm

3 Manufacturing of a microactuator with a transmission grating

The micromechanical element comprises two wafers: a silicon actuator wafer and a glass wafer. Figure 2 shows the manufacturing of the microactuator.
The glass wafer carries the driving electrodes, bondpads and connecting lines. It has a round opening below the actuator for the incoming light beam.

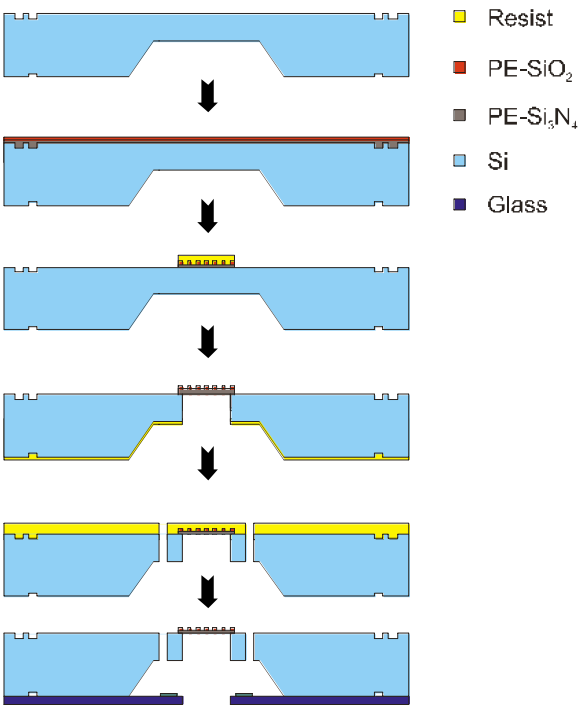

Figure 2: Realisation of micromirrors with transmission grating

The silicon wafer carries the microactuator with the optical transmission grating. The actuator is fabricated by bulk micromachining using a double side polished silicon wafer. At first the silicon membrane for the microactuator is fabricated by wet etching in potassium hydroxide. After that the optical layers, which consist of PE-SiO_2 and PE-Si_3N_4, are deposited on the front side of the wafer. The lower layer serves as the carrier layer, the upper layer is used for the grating. The optical layers were masked using stepper lithography. Then the grating is dry etched only in the PE-SiO_2 layer. After removing the resist on the front side, the whole backside of the wafer is masked with the exception of a round opening in the centre of the membranes. Hereafter the silicon is dry etched,

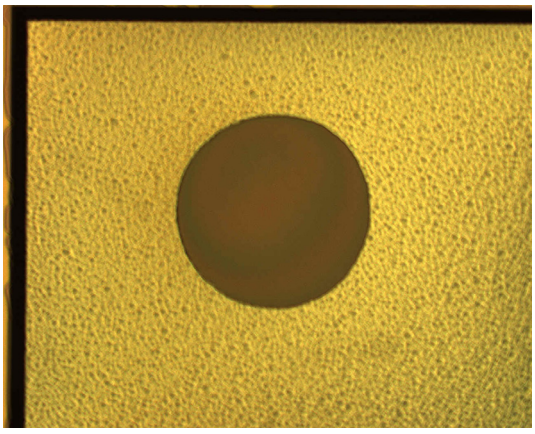

Figure 3: Wet etched silicon membrane with round transparent optical membrane

finishing the spanned transparent membrane with a grating. Figure 3 shows such a membrane; Figure 4 displays it in greater detail.
To fabricate a movable mirror, the silicon is dry etched again from the front side using a resist mask. After removing the mask, the silicon wafer is attached to the glass wafer by anodic bonding. Finally, the wafer is divided into individual actor chips with a diamond saw.

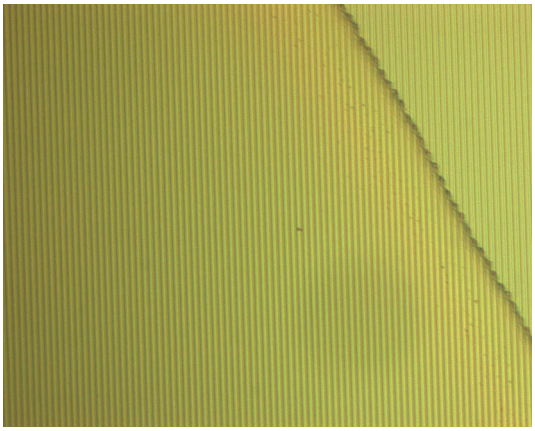

Figure 4: Detail of the optical membrane, partly on silicon (upper right corner), partly spanned

4 Optical Characterisation

The realised optical gratings have to be studied regarding their optical properties. Important parameters are the spectral resolving power and the diffraction efficiency of the gratings. For the first experiments a glass wafer that is 685 µm thick has been used. On one side of the wafer are rectangular gratings with a grating period of 2 µm and a groove depth of 510 nm. They have been structured in a silicon dioxide layer. The used experimental methods and results of the optical characterisation of these gratings are presented below.

4.1 Spectral resolving power

The diffraction properties of a grating are measured using the experimental setup shown in Figure 5. The CCD-line is arranged in the first

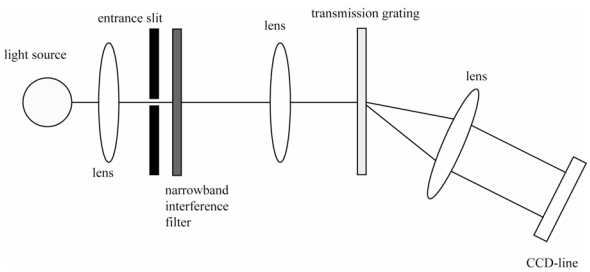

Fig. 5: Schematic experimental setup for the measurement of the spectral resolving power.

diffraction order parallel to the spectrum.
Various narrowband interference filters are placed successively in the optical path in front of the grating. The distribution of the transmission characteristics against the wavelength of each filter forms a sharp Gaussian distribution with a full width at half maximum of about 15 nm. The additional lens after the grating improves the sharpness and intensity of the spectrum on the detector.
The diffracted intensity distributions measured by the CCD-line are shown in Figure 6. The spectral resolving power of the grating is sufficient for a 2-µm grating. Furthermore the Gaussian transmission characteristic of the interference filters is reproduced very well.

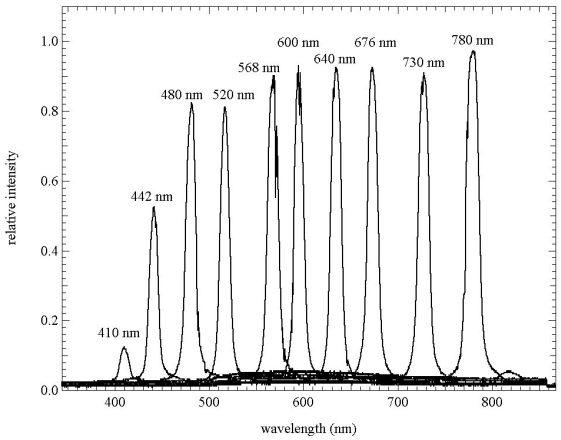

Fig. 6: Relative intensity measured by the CCD-line versus the wavelength for a rectangular transmission grating. The specified wavelengths are the appropriate central wavelengths of the filters.

4.2 Diffraction efficiency

Another important optical parameter is the diffraction efficiency of the gratings. In the image capture device that shall be realised later, the light exposure times last less than 5 µs for each spectral interval. Therefore a small diffraction efficiency of a grating can have a negative influence on the system capability.
The diffraction efficiency is measured using an experimental set-up similar to the one shown in Figure 5. First of all the luminous flux passing through the transmission grating is measured in dependency on the wavelength. Therefore different narrowband interference filters are placed successively in the optical path as described in section 4.1. A photometer is positioned directly behind the grating insuring that the detector collects all of the transmitted light. Afterwards the photometer is positioned in the first diffraction order. The diffracted luminous flux is measured against the wavelength using the different interference filters. The quotient between the diffracted and incident light is the relative diffraction efficiency. The measurement results are shown in Figure 7.
The measured diffraction efficiencies of the first gratings are in a range between 16 % and 29 % depending on the wavelength. Compared to the previous reflection rectangular gratings [3] and the theoretical maximum diffraction efficiency of a rectangular phase grating of 42 % [4], these are already very promising values.

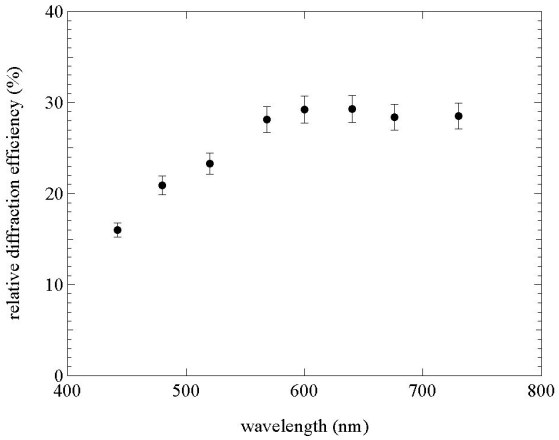

Fig. 7: Relative diffraction efficiency depending on the wavelength.

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Subproject B6: Force sensor arrays for Atomic Force Microscopy

Müller, Anne-Dorothea; Müller, Falk; Hietschold, Michael
Chemnitz University of Technology, Faculty of Natural Sciences, Institute of Physics,
Solid Surfaces Analysis Group, 09107 Chemnitz

1 Introduction

In the project B6 of the SFB 379, cantilever arrays for Atomic Force Microscopy (AFM) are developed. In the first three years of the project till 2003, the general applicability and the function of single devices have been studied. A specialized measurement set-up has been developed which is able to work with the cantilever arrays and to evaluate the signals from two or more cantilevers simultaneously. The main part in 2004 was the application of the new devices for some new physical experiments.
On the way to these experiments, the procedures for tip etching and the materials used to contact the single cantilever membranes had to be improved [1,2]. The following report will shortly consider some basic improvements of the cantilever arrays and then describe their usage in a physical experiment.

2 Cantilever development

2.1 Basic principle

The multiple cantilever devices consist of a silicon membrane and a glass substrate. They are anodically bonded onto each other. While the glass substrate provides an electrode structure (Fig. 1), the silicon is devided into single membranes by sleshes, each of them contacted to a separate electrode via the bonding connection. The movable cantilever parts have about 10 µm distance to the underlaying electrodes.
Each cantilever membrane consists of an actuator part, which allows a slow vertical movement of the tip over a range of up to 6 µm, and a sensor part, which is used for the force measurements to work in the dynamic mode AFM.
Based on geometrical considerations it is possible to form tips at the outermost end of each cantilever.

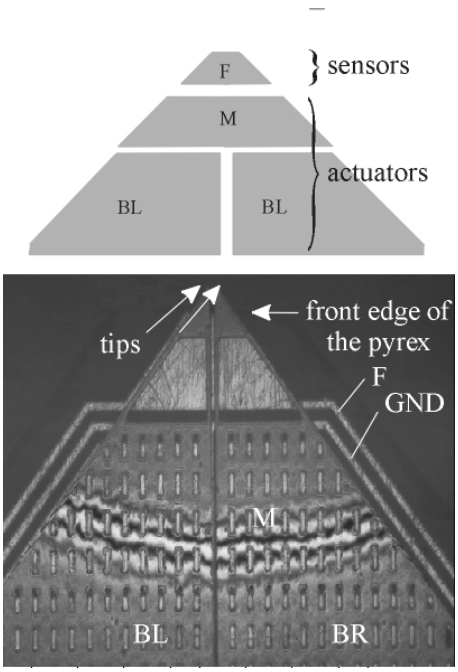

Fig. 1: Sketch of the electrode structure and interference microscope image of a real double cantilever device.

2.2 Tip geometry

The tips are formed by an anisotropic etching of the partly oxidized silicon membrane as shown in Fig. 2. Changes in the processing of the silicon membrane and the usage of serial lithography (wafer stepper) instead of parallel lithography have lead to tip diameters of about 5 nm.

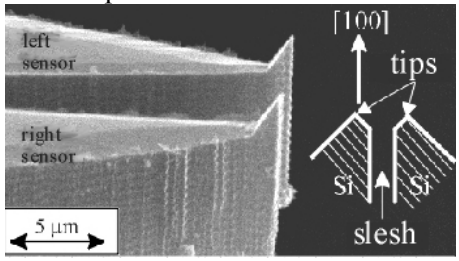

Fig. 2: Scanning Electron Microscopy image of the integrated tips. Sketch of the geometrical conditions for tip formation.

3 Mesoscopic temporary devices

3.1 Temporary devices

The aim of this physical experiment is it, to investigate surface states on semiconducting surfaces by measuring electrical characteristics in an nondestructive way. Our approach is therefore, to use a contacting device with two point contacts, which creates a transistor-like DUT (?) only for the moment the measurement is done. We designate it as a temporary device, because it can be created and cancelled on every surface point. [3]

3.2 Experimental procedure

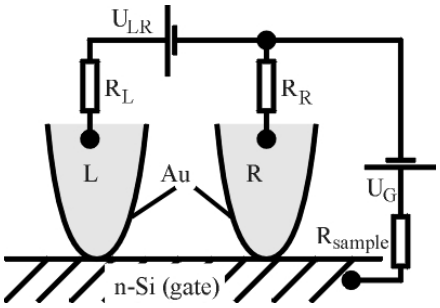

Fig. 3: Schematic drawing of the experimental set-up including electrical connections between substrate and contact tips.

A cantilever device with two gold coated silicon tips has been used to form two point contacts on a silicon surface (Fig. 3). The lateral distance between the tips is 10 µm. They are independently movable in vertical direction and the contact force is defined. While the contacts are closed, a complete set of electrical characteristics of the system is measured.

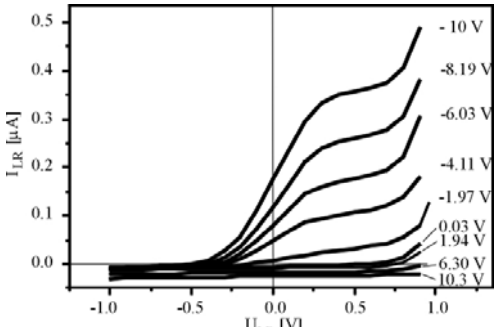

Fig. 4: Experimental data obtained on a hydrogen passivated Si(100)-surface with two gold coated n-Si-tips.

As sample surface, n-doped Si(111) was used. The n-Si/Au-interface should form a Schottky contact with a barrier height of 230 mV. The sample is mounted in the specialized AFM setup and contacted with InGa alloy. The contacts show an Ohmic resistance of less than 300 Ω.
The approach is done in a dynamic mode for each cantilever separately, while the measurements are done in a contact mode regime. In the results shown in Fig. 4, an Ohmic current and a field dependent current are found, demonstrating that the system behaves like a FET.

3.3 Results

The detected curves have been compared with circuit simulations (Fig. 5) in which the temporary device has been emulated as MESFET. In order to obtain simulation results that are close to the detected curves, the contact resistance of the sample had to be increased to over 5 MΩ.

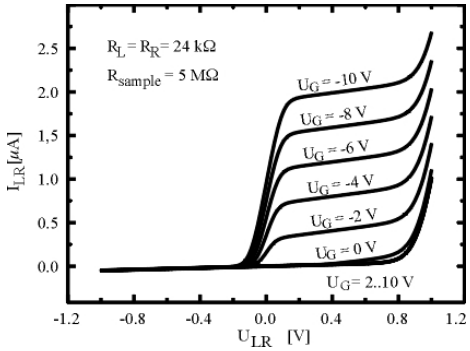

Fig.5: Best fitting simulated curves and parameters used for simulation.

From these simulations together with the measurement results it has been concluded that the coupling between the substrate surface and the bulk material is very weak in the created temporary device. The detected conduction processes take place at the surface or at the interface between Si and SiO_2. The bias dependence of the detected current proves that the current is influenced by the electrical field applied through the bias voltage.

4 Related works

An important task in new physical experiments is the preparation of suitable samples. For the silicon samples used in the descibed experiments, a glove box with clean room conditions has been built up. The samples are prepared in cooperation with the Hahn Meitner Institute in Berlin. Other samples prepared in our group contain special nanostructures for imaging, as porous alumina on silicon [4] or

monolayers of organic molecules on crystalline surfaces [5, 6].

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Subproject C2: A Novel High Aspect Ratio Technology for MEMS Fabrication Using Standard Silicon Wafers

Gessner, Thomas[1,2]; Ebest, Gunter[3]
[1] Fraunhofer-IZM Chemnitz, Department MD & E
[2] TU Chemnitz, Fakultät für Elektrotechnik und Informationstechnik, Professur Mikrotechnologie
[3] TU Chemnitz, Fakultät für Elektrotechnik und Informationstechnik, Professur Elektronische Bauelemente

1 Introduction

The development of a novel CMOS compatible technology for the fabrication of high aspect ratio microstructures (HARMs) is part of the Collaborative Research Center 379. First prototypes of "*Air gap insulated Microstructures (AIM)*" were manufactured and characterized in the third period of the project, presented elsewhere [1, 2].
According to the objectives of subproject C2 within the first year of the last funding period there are technology as well as application issues to be considered. Exemplary a description of the progress achieved will be given in the following.

2 Technology developments

The continuing development in the field of anisotropic silicon etching is resulting in increasing aspect ratios of etched trenches. Especially HARMs technology may profit form these results of research. To transfer the advantages of the increased aspect ratio to the AIM technology, the deposition process of the CF-polymer, the release etch and the final highly parallel isotropic silicon etch process for the removal of silicon underneath the interconnection beams has to be adapted.

2.1 CF plasma polymer for release etching

The deposition characteristic of CF-polymers on the sidewalls of deep silicon trenches depends on the process parameter and is strongly affected by transport mechanism inside the trenches. For high aspect ratio trenches, a breakdown of the passivation layer could be observed while the sidewalls of lower aspect ratio trenches are free of any defects (Fig. 1).

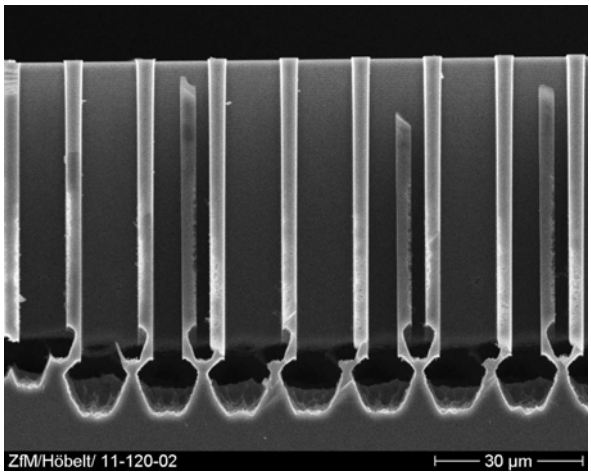

Fig. 1: Aspect ratio depending quality of the passivation layer consisting of a CF-polymer

2.2 Process optimization

For the fabrication of 50 µm high silicon structures, using trenches with an aspect ratio up to 16:1, an optimization of the existing deposition process, release etch and the highly parallel isotropic silicon etch were necessary. The results can be seen in Fig. 2, which is a SEM-picture of a part of an inclination sensor with a structure height of about 55µm.

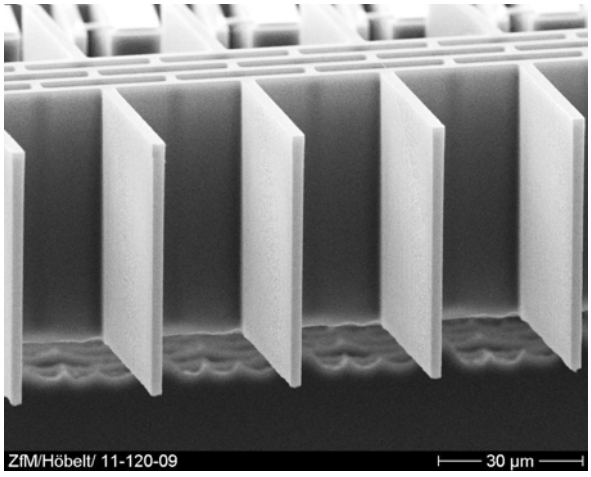

Fig. 2: SEM-picture: cross section of a silicon structure

3 Devices fabricated

Exemplarily, a sensor and a sensor-actuator system fabricated by the AIM technology are presented:

3.1 Large area sensor-actuator

In order to get an impression of the capability of the AIM principle, an electrostatically driven system for AFM-applications has been designed and fabricated. It includes a one-axis actuator enabling a large positioning range, a separate actuator for generating oscillation and a capacitive sensor (Fig. 3). It is comparable to former developments based on the SCREAM technology.

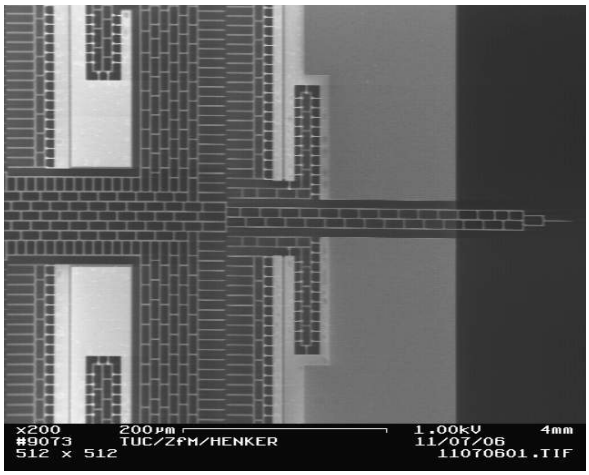

Fig. 3: SEM-picture of a large area sensor-actuator

As expected, when using the AIM technology there was no out-of-plane deformation detected like before. The system has been tested for actuation voltages up to 40 V. The long-term behaviour of the system has been controlled by measuring the mechanical resonance too. No significant shift of the resonance frequency is detected indicating that there is no creep fatigue.

3.2 *Low-g* inertial sensor

A *low-g* inertial sensor has been chosen as a second device for AIM technology evaluation because it is a very sensitive and fragile system during fabrication as well as application. Due to the low spring constant "sticking" during fabrication as well as in operation is a serious issue (Fig.4).

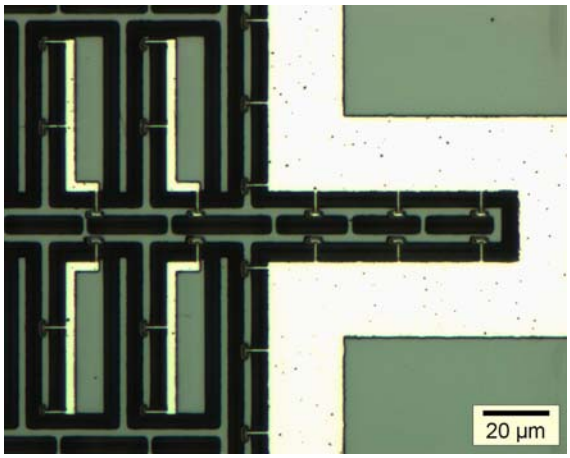

Fig. 4: Top view (detail) on fixed electrode and seismic mass of a low-g sensor fabricated by AIM technology

Throughout dry processing and respecting the existing design rules is a guarantee to avoid sticking. Meanwhile a proven technology is available offering a high yield and device applications for inclination measurements as shown in Fig. 5.

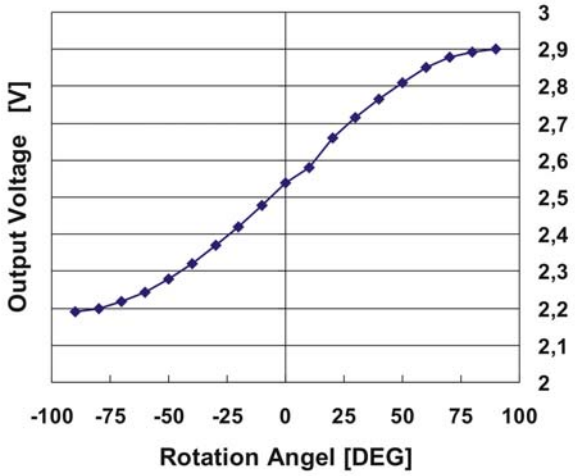

Fig. 5: Output vs. rotation of low-g sensor (GEMAC: CV2 ASIC and measurements)

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Different SiH_4 treatments of CVD TiN barrier layers for Cu Metallization

Ecke, Ramona; Bonitz, Jens; Schulz, Stefan E.
TU Chemnitz, Center for Microtechnologies

1 Introduction

The ITRS 2003 predicts for interconnects a reduced diffusion barrier thickness of a few nanometers in the next years. But the film thickness reduction involves an increased defect density. Particularly with regard to crystalline barriers like TiN the diffusion path along the grain boundaries is drastically shortened.
The TiN barrier performance can be enhanced by silane treatments. On the one hand the silane treatment could lead to Si-N formation, so that the TiN grains are embedded in amorphous SiN. On the other hand the Si introduction in the barrier results in higher electrical resistivity.

2 Experimental

The experiments were carried out in a lamp-heated tungsten CVD chamber of an applied Materials 5000™ cluster tool. The TiN layers were produced by a multistep process consisting of alternating MOCVD deposition steps and H_2/N_2 plasma treatment steps. The pyrolysis of tetrakis(dimethylamino)titanium (TDMAT) at substrate temperatures of 350°C is used for the deposition step. The density, microstructure, composition and consequently the electrical resistivity and barrier performance are strongly affected by the plasma treatment parameters [2]. This TiN contains grains reaching nearly from the bottom to the top of the entire film thickness which means there is no interruption of grain growth by the multiple deposition process.
Marcadal et al. [3] investigated silane soaks after each full cycle and for not plasma treated TiN films to exemplify the insufficient densification at the sidewalls of vias and trenches. In the case of plasma treated Ti(Si)N films the grains are smaller then for pure TiN and are confined to a single cycle layer. But the Si amount is smaller (4 %) than in the not plasma treated TiN (7 %).
We investigated silane treatments integrated as soak but also as plasma at different times in the TiN deposition cycle:

TiSiN 1 10 s SiH_4 plasma between pyrolysis and H_2/N_2 plasma
TiSiN 2 10 s SiH_4 soak between pyrolysis and H_2/N_2 plasma
TiSiN 3 30 s SiH_4 plasma instead of H_2/N_2 plasma
TiSiN 4 10 s plasma after a full cycle

The integration in the whole process was done for a 3 cycle process to obtain thin films ≤ 10 nm and only the middle cycle was treated with SiH_4.

3 Results

For all SiH_4 treatments the deposited film thickness and the electrical resistivity were partly drastically increased compared to untreated TiN. Only TiSiN 2 with the SiH_4 soak results in moderate thickness and electrical resistivity.

Table 1: Electrical resistivity of the SiH_4 treated TiN compared to TiN in the same thickness range

TiSiN process	ρ_{TiSiN} [μΩcm]	ρ_{TiN} [μΩcm]	d [nm]
TiSiN 1	689	175	16,8
TiSiN 2	334	260	8,5
TiSiN 3	1605	130	26,2
TiSiN 4	542	225	14

In case of the SiH_4 plasma treatments the clearly higher thickness is caused by the deposition of a Si interlayer. The thickness of these Si layers depends on the SiH_4 plasma treatment time. The replacement of the H_2/N_2 plasma by SiH_4 plasma leads to 13 nm Si deposition and thus to highest thickness of the whole layer. The SiH_4 plasma onto the not densified TiN layer (TiSiN 1 and TiSiN 3) yielded nearly no densification of these cycle layers. These layers remain amorphous in comparison with the first cycle layer. Also the middle cycle layer of TiSiN 2, SiH_4 soak onto the not densified layer with followed H_2/N_2 plasma, is thicker and appears more amorphous than the other cycle layers. Because of the H_2/N_2 plasma after the SiH_4 soak the formation of SiN bonds is more likely as the TOF-SIMS results confirm.

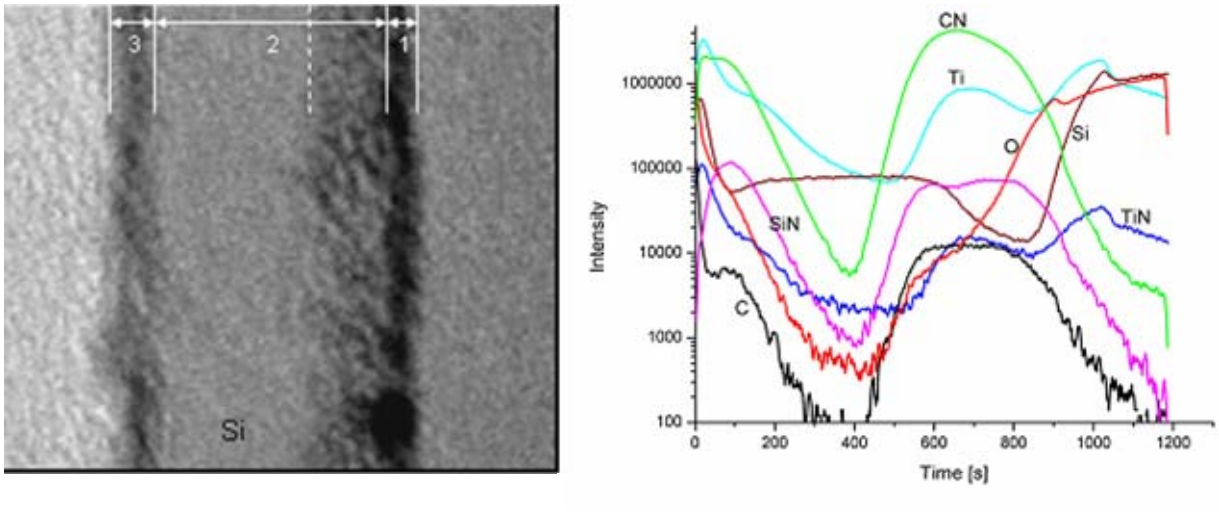

Fig. 1: TiSiN 3 (SiH_4 plasma insteat of H_2/N_2 plasma) TEM image and TOF-SIMS graph

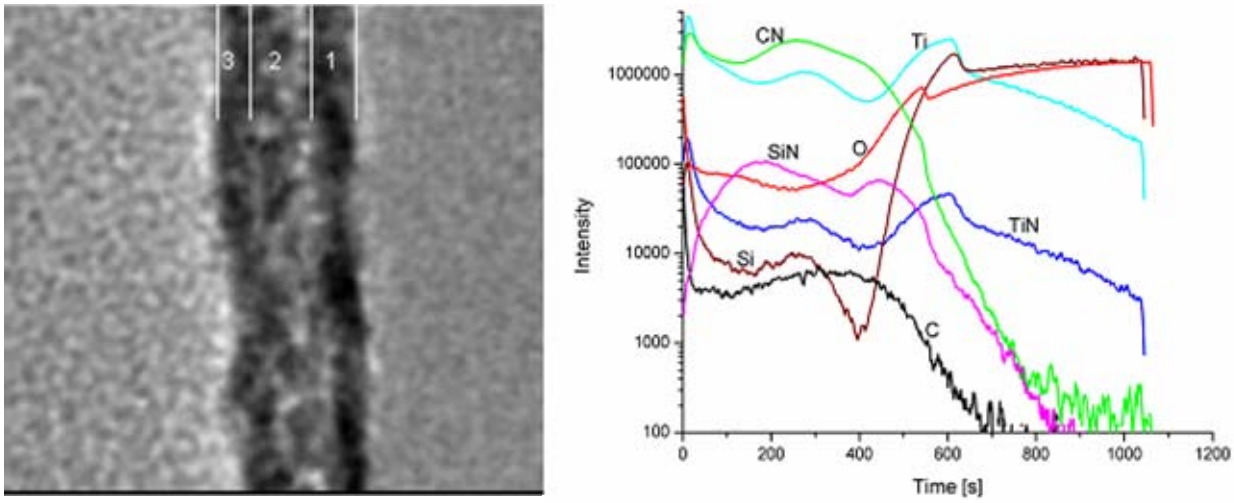

Fig. 2: TiSiN 2 (SiH_4 soak between pyrolysis and H_2/N_2 plasma) TEM image and TOF-SIMS graph

By the same evidence the layers from the 3rd cycle in all SiH_4 treatment variants seem less crystalline than the layers from the first cycle. Probably, here the Si from the foregoing cycle is incorporated during the pyrolysis of TDMAT in the layer and inhibits a continuous crystallisation.

Apart from the Si deposition of the SiH_4 plasma treatments, these treatment variants are not qualified for the improvement of barrier performance. The efficiency of the plasma at the sidewall is reduced because of the direction dependent impact of plasma.

A thermal silane treatment is more suitable to stabilize the TiN barrier. The electrical resistivity is only slightly increased and the grain growth is inhibited by the SiN formation.

Further investigations will be performed to examine the thermal stability and barrier efficiency of the developed Ti(Si)N films.

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Deposition and characterisation of ultra low k dielectric films for 45 nm node Cu interconnect systems of CMOS logic ICs

Frühauf, S.[1] ; Schulz, S.E[1].; Rennau, M[1].; Homilius, J[1].; Puschmann, R[1].; Himcinschi, C[2].; Friedrich, M[2].; Schneider, D. [3]

[1]TU Chemnitz, Center for Microtechnologies, Professorship Microtechnologies
[2]TU Chemnitz, Professorship Physics of Semiconductors
[3] FhG-IWS Dresden, Department Technology of Thin Films

1 Introduction

Methylsilsesquioxane (MSQ) is a promising candidate for ULK dielectric layers since it has a significantly lower density than silicon dioxide. Due to the methyl groups bonded to the Si-O-network of the MSQ it is much more hydrophobic and requires no additional hydrophobisation treatment like silica aerogel. At Center for Microtechnologies investigation of the MSQ-based and porogen containing spin on material LK2200™ provided by Rohm&Haas has been performed over the last year. The material is dedicated for dielectric layers in advanced 45nm Cu interconnect systems of CMOS logic ICs. The porogen consists in acrylic nanoparticles introduced in order to control the porosity of the layers. After porogen removal by annealing mesoporous films with k-value of about 2.2 were obtained. Integration, especially patterning and CMP can be also carried out on porogen containing films. This “post-integration-burnout” or “post-CMP-burnout” approach is known as “SOLID-FIRST-PROCESS”. In that case films have only intrinsic porosity of the MSQ skeleton and withstand much better chemical attack as well as mechanical load.
The deposition process for LK2200™ was adapted to Suss Microtech spin on track provided for deposition of low k materials. The obtained dielectric films were characterized in order to determine their starting properties before integration and to study their modification during integration.

2 Electrical properties

A simple stacked parallel plate capacitor approach was used to quantify dielectric film properties by capacitance measurements with a mercury probe. Dielectric constants were measured at a frequency of 100 kHz. Leakage current density was determined at an electrical field of 1 MV/cm. For determination of field break down voltage 17 points were generally tested. The cumulative frequency is shown in Fig. 1. Mean values are given in Tab. ***1***.

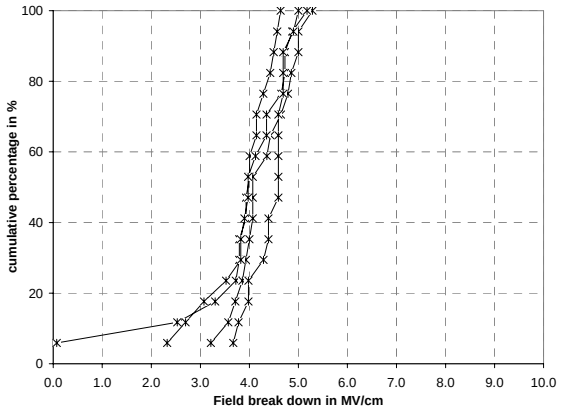

Fig. 1: Cumulative frequency for FBD of LK2200

Tab. 1: Electrical features of LK2200™

	mean k-value	**mean $I_{leakage}$ in A/cm²**	**mean FBD in MV/cm**
LK2200 (ver6)	2.28±0.05 (3σ=2.1%)	$1.8*10^{-10}$	4.2

3 Porosity and Mechanical properties

Youngs modulus is one of the most critical features of the material. All relevant mechanical properties like hardness, strength and crack

resistance are related to the elastic constant. On the other hand Youngs modulus depends strongly on porosity. Pore size distribution and porosity was determined by ellipsometric porosimetry in co-operation with SOPRA France (see Fig. 2).

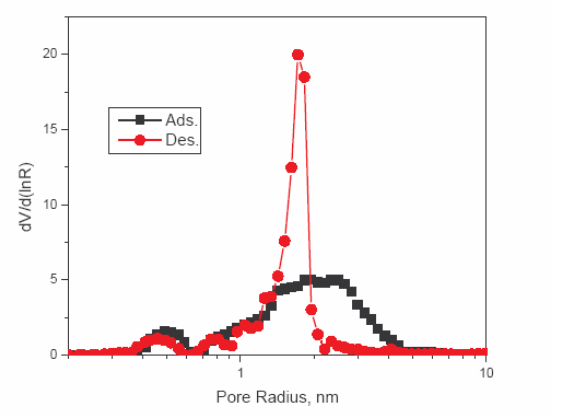

Fig. 2 Pore size distribution for LK2200™ obtained from ellipsometric porosimetry (SOPRA)

An estimation of the porosity π can deduced from effective refractive index of the dielectric film n_r using LORENTZ-LORENTZ-Effective Medium Approximation, if the refractive index of the skeleton n_s is known:

$$\pi = 1 - \left[\frac{n_r^2 - 1}{n_r^2 + 2}\right] / \left[\frac{n_s^2 - 1}{n_s^2 + 2}\right]$$

Both values for porosity, from ellipsometric porosimetry (EP) and from refractive index (SE), are compared in Tab. 2.

Tab. 2 Porosity and mean pore radius of LK2200™

	porosity (n_{msq}~1.45)		**mean pore radius**
	EP	**SE**	
LK2200	31 %	30 %	2.1 nm

Measurement of the elastic constant needs careful investigation of the limits of the selected method. Nanoindentation as an often applied method causes generally inelastic deformation of the material by indenter penetration. Additionally, substrate influence is significant for thin layers and for penetration depths of more than 10% of film thickness. At TU Chemnitz an advanced measurement procedure called “elastic measurement” was developed using a spherical indenter and very low indenter loads. It is assumed, that with this method a nearly elastic deformation state of the material is possible to realize without damage of the film. The obtained values correlate well with the elastic constants determined by laser-acoustic measurement. Dispersion of surface acoustic waves causes only very small deformation. Therefore the condition for pure elastic deformation state is achieved. The results for the Youngs moduli are summarized in Tab. 3.

Tab. 3: Youngs modulus of LK2200™

	Youngs Modulus	
	Nanoindentation	LSAW
LK2200	2.9 GPa ± 0.91 (spherical indenter) 4.0 GPa ± 0.43 (Berkovich indenter)	3.2 GPa ± 0.08

In order to evaluate internal stress and adhesion strength the dielectric film was deposited on several sublayers (SiO, SiN, SiC, SiCN) and were capped with several hardmask materials (HM2800, SiO, SiN, SiC, SiCN). All dielectric film stacks passed the adhesion tape test without failure. The internal stress of the dielectric film was found to be below 100MPa.

4 Outlooks

Since the LK2200™ films exhibit excellent electrical and mechanical properties these dielectric films has been dedicated for integration in Single DAMASCENE architecture for Cu/low k interconnect systems for the next research phase.

Acknowledgement

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Polycyanurates – low-k materials approach for IC metallization

Schulze, K.[1]; Schulz, S. E.[1]; Schuldt, U.[2]; Kahle, O.[2]; Dreyer, C.[2]; Uhlig, C.[3]; Gessner, T.[1]; Bauer, M.[2]
[1] Chemnitz University of Technology, Center of Microtechnologies, Germany
[2] Brandenburg University of Technology Cottbus, Chair of Polymeric Materials, Teltow, Germany
[3] Fraunhofer Institute for Reliability and Microintegration IZM, Branch Lab Polymeric Materials and Composites in Teltow, Germany

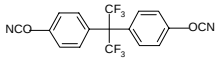
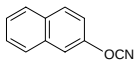
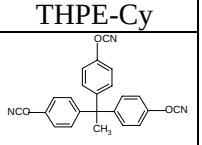
1 Introduction

Development of new low-k materials can be realized by two main attempts. One way is to decrease the dipole strength by using materials with non-polar bonds. The other approach is to decrease the dipole density, which means the reduction of the density of the material itself by introducing porosity or increasing of the free volume.

2 Experimental

For the examinations described here, polycyanurates are the basic materials. They are good candidates for low-k materials of reduced density, since annealed difunctional cyanate ester monomers yield by polycyclotrimerization a polycyanurate network of high symmetry consisting of interconnected triazine rings. The density of the polycyanurates was reduced by copolymerization of difunctional cyanate (ester) monomers with aromatic bulky trifunctional or monofunctional cyanate ester monomers. For the according structural formulas see table 1.

Tab 1:Used monomers

monomer	F10	mCF3Cy
chemical formula		
monomer	2Naphtcy	THPE-Cy
chemical formula		

Copolymerization reduces density without generation of a porous network. That offers the advantage to prevent partially from generally known integration issues of porous materials, like moisture absorption or precursor penetration during other process steps.
Polymers of different amounts of the additional introduced monomer by copolymerization were mechanically (E-Modulus, density, hardness) and electrically (k-value, field breakdown strength, leakage current) characterized. Some electrical measurement results are shown in table 2. For instance for F10, the k-value could be reduced by copolymerization from 2.91 to 2.54.

3 Results

At all the investigated films had very promising electrical properties, especially leakage current was very low and field breakdown strength fulfilled in general the required value of more than 3 MV/cm. By further examinations including curing, thermal stability and influence on k-value were tested.

Tab. 2: Electrical properties of copolymerized and non-copolymerized polycyanurates

Film composition	k	Leakage current J_{leak} [A/cm²]	E_{BD} [MV/cm]
100mol% F10	2.91	$< 5.0 \cdot 10^{-13}$	-
50mol% F10 + 50mol% mCF3Cy	2.88	$< 1.9 \cdot 10^{-12}$	7.1
33mol% F10 + 67mol% mCF3Cy	2.54	$< 5.4 \cdot 10^{-11}$	3.2

Patterning experiments on these polymers were done for a basic evaluation of the potential for integration in copper damascene technology. Representative for a non-copolymerized and a copolymerized material *100mol% F10* and *50mol% F10 + 50mol% mCF3Cy* were selected for these examinations. A single hard mask was used. For a better evaluation of the patterning results and possible defects a partial hard mask

(see figure 1) etching was applied. That allows a strict separation of all single process steps to be done and their influence in respect to a modification or damage of the low-k films.

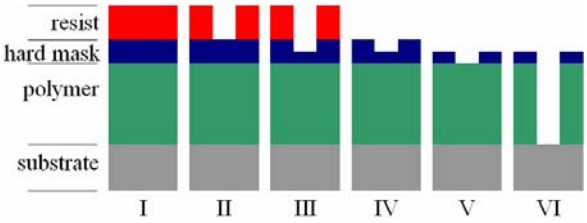


Fig. 1: Application of partial opened hard mask for patterning

After photolithographic patterning of the resist a partial anisotropic plasma etching of the PECVD SiO_2 hard mask followed. Main aspect thereby was, to avoid any breakthrough of the hard mask. This is necessary to avoid any damage or istropic etch of the polymer film by the subsequently applied O_2 plasma resist stripping. Via an additional process step, the hard mask was etched until breakthrough to the low-k material. For patterning of the polymer a new O_2 dry etching recipe was developed. In figure 2 and figure 3 SEM images of damage-free patterning results are shown.
During preparation no significant difficulties or defect mechanisms like delamination, crack or blister generation, known from other low-k materials, did occur. The quality of the generated profiles is good and comparable for both materials.

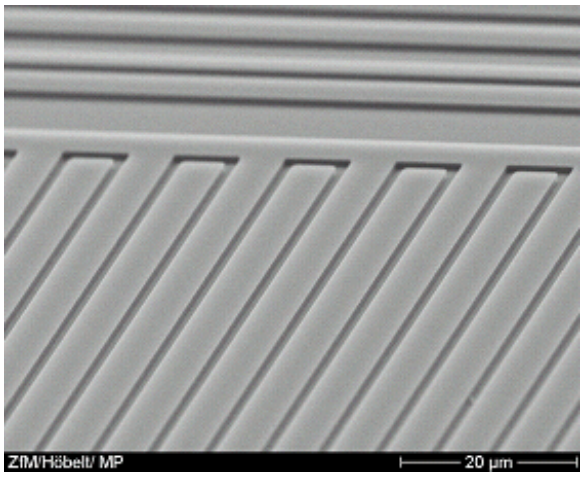


Fig. 2: SEM of patterned polycyanurate and PECVD SiO_2 hard mask on top

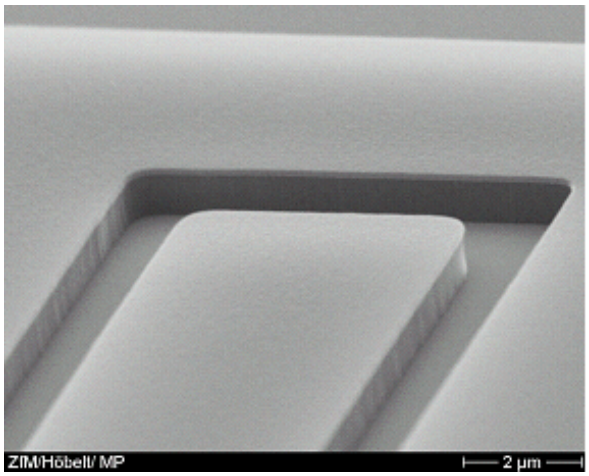


Fig. 3: SEM of patterned polycyanurate sidewalls (PECVD SiO2 hard mask on top)

Future work will be concentrated on integration of these materials in copper damascene technology, by evaluating CMP compatibility or compatibility to barrier materials. Especially mechanical properties (see table 3) are very promising for a successful Cu and barrier CMP using these low-k materials.

Tab. 3: Mechanical properties of copolymerized and non-copolymerized polycyanurates

Film composition	E-modulus [GPa]	Hardness [GPa]
50mol% F10 + 50mol% mCF3Cy	3.5	0.24
33mol% F10 + 67mol% mCF3Cy	4.0	0.21
B10	4.7	0.26
86mol% B10 + 14mol% THPE-Cy	4.1	0.27
50mol% B10 + 50mol% THPE-Cy	3.8	0.30

Acknowledgement

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Ultra low-k dielectric etching and stripping processes

Blaschta, Frieder; Schulz, Stefan E.; Rennau, Michael
Chemnitz University of Technology, Faculty for Electrical Engineering and Information Technology,
Center for Microtechnologies

1 Introduction

Although the debate still rages about the materials used, we will report essentially about the patterning and stripping of SiO_2 aerogel and MSQ based ultra low-k dielectrics. Common to both is that there is porosity in the dielectrics. This means, that all processes must be carefully adapted to this fact.

2 Experimental

In general, the patterning processes of dense SiO_2 are transferable to low-k. However, the layer stack, mask material and strategy have to be modified. Always one must consider the large inner surface of the dielectrics because of the porosity. Moreover, low-k material demands an additional cap layer, which simplifies patterning. In connection with this, the concept of single and dual hard masks was introduced to etch the low-k materials and to strip the necessary photoresist afterwards.

Fig. 1 shows the scheme of a single and dual mask stack.

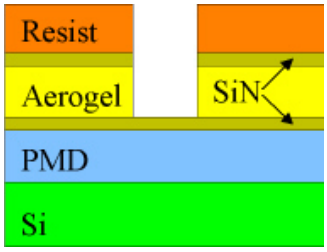

Fig. 1a: Single hard mask

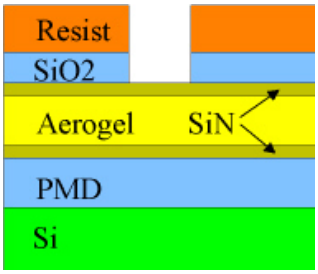

Fig. 1b: Dual hard mask

In general, after 500nm PECVD SiO_2 / 50 nm PECVD SiN deposition on a Si (100) substrate, an about 500nm thick porous layer of low-k material was deposited. Normally, a cap layer of SiN (Hardmask HM1, 50 - 400nm thick) was deposited on it. In case of dual hard mask additionally a PECVD SiO_2 layer (HM2) of about 500nm thickness was used.

The patterns of vias and lines were formed by conventional i-line photolithography and e-beam lithography in some cases.

The reactive ion etch (RIE) with inductively coupled plasma source (ICP) has been carried out in an equipment of Oxford Instruments.

First trials with a conventional gas mixture of $CHF_3/CF_4/O_2$ showed adhesion failures at the interface between SiN and aerogel (Fig. 2).

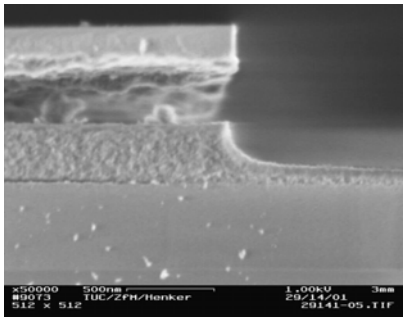

Fig. 2: Adhesion failure at single hard mask caused by oxygen containing etch processes.

By eliminating oxygen in the etch processes the adhesion could be improved and at the same time the damages of low-k materials were reduced. In this way we were able to etch sensitive low-k materials, like aerogel [1].

Fig. 3 demonstrates the successful patterning using a CF_4/Ar mixture.

The advantage of a dual hard mask was used to remove the photoresist without impacts on porous low-k and hardmask / aerogel interface with an intermediate etch stop after etching the hard mask HM2.

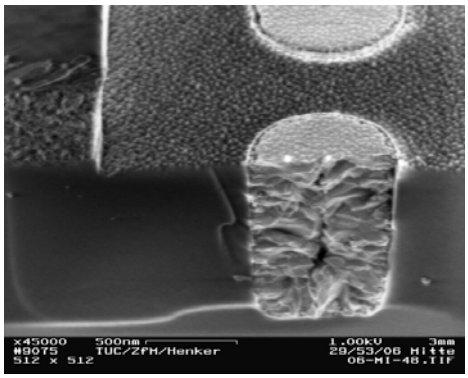

Fig. 3: Patterning with dual hard mask

In the following, a hydrogen based resist removal has to be performed in order to minimize the impact on low-k materials. A suitable H_2-plasma strip was developed at an AMAT ASP chamber, using a downstream microwave discharge. Remaining impact of hydrogen ashing process on low-k materials, like aerogel, porous MSQ and non-porous Black Diamond™ was investigated. In order to simulate the worst case of impact, plasma treatments were done at blanket wafers with the above mentioned materials. The relative change of thickness and the k-values were investigated.
Fig. 4 shows the relative change of thickness in dependence of time of plasma treatment.

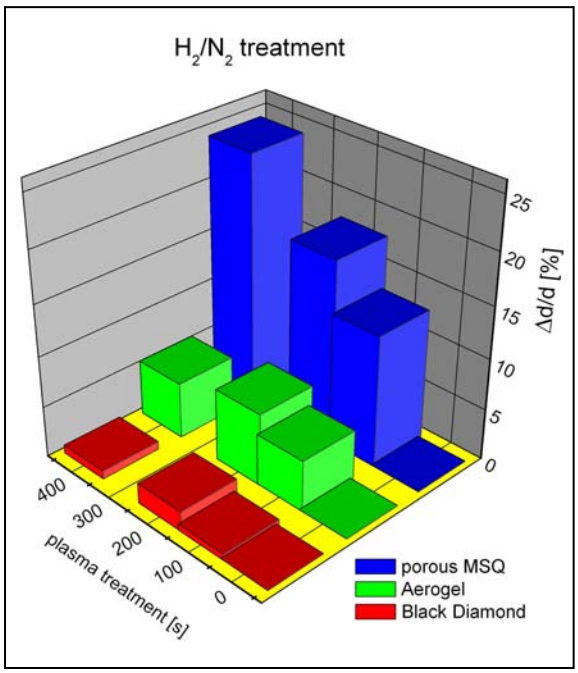

Fig. 4: Thickness change after plasma treatment of low-k materials

It is obvious that porous material suffer the most impact of stripping. That means the ashing process should be reduced to minimum with respect to damages of low-k materials. A similar situation was found by measuring the k-values. Fig. 5 confirms the impact of ashing on porous materials, again.
The nonporous material is nearly unchanged.

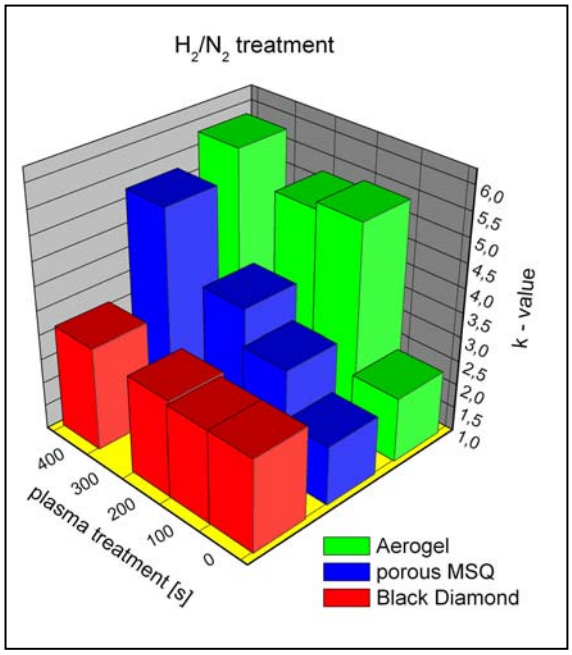

Fig. 5: k-values of plasma treated dielectrics

3 Summary

The concept of single and dual hard mask was studied with respect to etching and stripping. Both procedures have pros and cons.
It was found common to both, that oxygen must be excluded in all cases.
The stripping by means of hydrogen plasma is most promising, but further optimization is needed.

4 References

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Acknowledgement

This work was performed in the framework of the IST program of the EC in the projects ULISSE (IST2000 30043) and NANOCMOS integrated project (IST-507587; www.nanocmos-eu.com).

Interface between porous ultra low-k materials for 45 nm node and diffusion barrier - pore sealing approaches

Schulz, Stefan E.[1]; Bonitz, Jens[1]; Engelmann, Hans-Jürgen[2]; Gessner, Thomas[1]
[1] Chemnitz University of Technology, Center for Microtechnologies
[2] AMD Saxony LLC & Co KG, MaLab, Dresden

1 Introduction

One of the main challenges for integrating porous low-k dielectrics into Copper damascene interconnect schemes is the interface between the conducting diffusion barrier and the etched porous material at the trench and via sidewalls. It has been shown, that different issues exist for barrier deposition onto the porous material:

- Precursor penetration into open-pore dielectrics during either barrier CVD or ALD,
- Resulting barrier deposition in the surface-near region or even in the whole porous dielectric,
- Formation of a porous or less dense barrier at porous surfaces (PVD, CVD) causing decreased barrier efficiency.

To overcome these problems pore sealing has to be performed at the trench and via sidewalls. Different approaches exist to achieve smooth and/or sealed sidewalls of porous dielectric materials after etching:

- Deposition of a CVD dielectric liner of minimum thickness and subsequent spacer formation by etching [1].
- Deposition of a very thin spin-on dielectric sealing layer.
- Post-etch burnout (PEBO) of porogen in the dielectric: The porogen contained in the dielectric is usually removed after deposition by annealing and leads to the formation of the porous structure. Special porogens (e.g. in pSiLK) are modified during dielectric etch at the sidewall of the patterns, where they are exposed to the etching chemistry. A porogen removal (burn out) after etching leads to decomposition of the porogen only at not exposed locations leaving the porogen at the sidewall in place. This results in a smoother and sealed non-porous sidewall.
- Solid first™ or post-CMP burnout: The porogen contained in the dielectric is removed after CMP. For this case the dielectric is dense during integration which is important for CMP and exhibits a dense and non-porous sidewall after etching.
- Sealing of the sidewalls during etching by formation of sidewall passivation layers and/or plasma impact.
- Sealing of the sidewalls by plasma treatments after patterning.

In the examinations described in the following we applied pore sealing by using a CVD dielectric liner for porous spin on dielectrics with different pore size.

2 Experimental

A SiO_2 aerogel with a pore size of ~ 7 nm and a porous MSQ with ~ 3 nm pore size was deposited by spin on with a PECVD SiN cap layer to prevent interactions between photoresist and the porous material. The low-k dielectrics were patterned using reactive ion etching in an ICP discharge with CF_4 and Ar. After etching the photoresist was stripped by using an H_2/N_2-plasma. PECVD SiO_2 was used as liner material because it has the lowest k compared to SiC and SiN. The TiN barrier was deposited from TDMAT followed by a N_2/H_2 plasma treatment using one to 8 cycles of TiN deposition and plasma treatment. The process is described particularly in [2, 3]. Fig. 1 shows the cross-sections of the investigated samples.

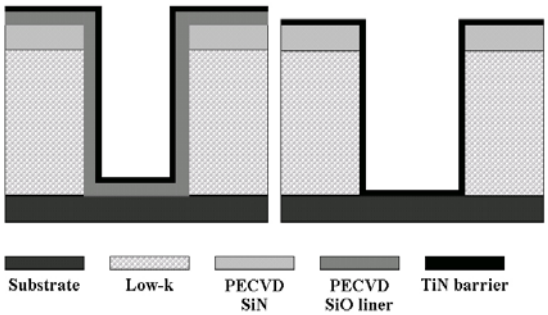

Fig. 1: Investigated porous low-k samples with (left) and without (right) CVD liner for pore sealing

3 Investigation of the TiN/porous dielectric interface

TEM and EDX line scan were done for samples of 10 nm TiN with and without 20 nm CVD liner, to determine the depth of penetration of TiN into aerogel (7 nm pore size) and MSQ (3 nm pore size) at the sidewall of the structures.

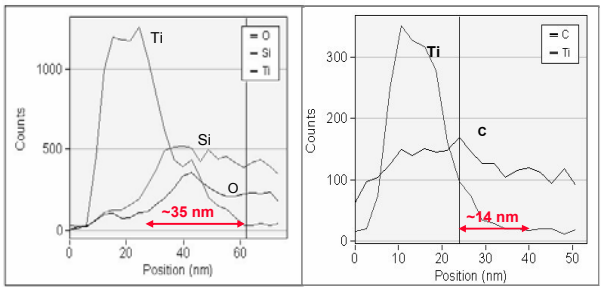

Fig. 2: EDX line scan of a TiN/Aerogel interface:at the surface (left) and at the trench sidewall(right)

Figure 3 shows EDX line scans of TiN/aerogel interface on top of the non-patterned dielectric and at the sidewall of an etched trench pattern (without CVD liner). At non-patterned samples Ti was detected in the dielectric up to a depth of 35 nm [4]. The Ti signal in the aerogel decreases down to the detection limit at a depth of ~ 14 nm at the Ti/aerogel interface at the trench sidewall. This may be due to a partial pore sealing by aerogel etching or photoresist stripping. Furthermore the highest carbon signal was measured at the interface (Fig. 3, right) indicating a possible formation of a sidewall passivation layer during ULK etching using a photoresist mask as reported in [5]. A CVD liner showed no additional improvement in preventing TiN prenetration.

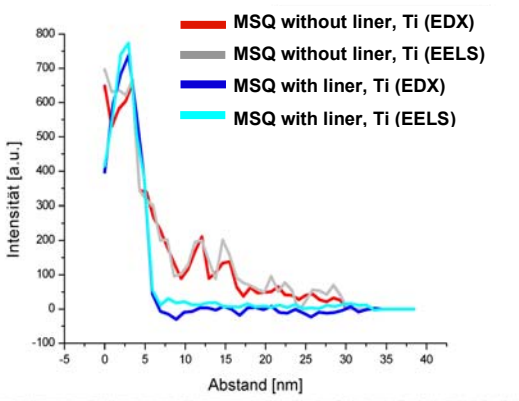

Fig. 4: EDX and EELS line scan of a TiN/porous MSQ interface with and without PECVD SiO_2 liner

EDX/EELS line scans of samples of TiN on porous MSQ show the positive impact of the CVD liner (Fig. 4). Without CVD liner the Ti signal in the MSQ decreases down to the detection limit at a depth of ~ 14 nm. This makes no difference to the respective aerogel sample and indicates no impact of the dielectric pore size on TiN precursor indiffusion. For the sample with CVD liner nearly no TiN penetration was detected. The Ti signal decreases abruptly just after the TiN/CVD liner interface. The reason is an improved pore sealing by the CVD liner due to the smaller dielectric pore size of the MSQ leading to a lower sidewall roughness and therefore improved barrier film growth.

3 Summary

The impact of different ULK material pore size (3 and 7 nm) on TiN diffusion barrier integrity was investigated. In addition, a SiO_2 CVD liner was used for pore sealing. It was detected that a smaller pore size facilitates better CVD liner and TiN barrier growth which results in a better barrier integrity. For SiO_2 aerogel with 7 nm pore size the CVD liner has no effect for the samples of 10 nm TiN with and without CVD liner. For the ULK material with 3 nm pore size an obvious improvement was found using the SiO_2 CVD liner. Furthermore a reduced TiN penetration into the aerogel dielectric compared to non-patterned samples was detected. This is believed to be caused by a partial pore sealing during ULK etching using a photoresist. Further investigations are in progress to prove this assumption.

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Acknowledgement

The work was performed in the framework of European NANOCMOS integrated project (www.nanocmos-eu.com). The support by the European Commission under EU contract number IST-507587 is acknowledged.

CMP process development for Cu/low-k based interconnect systems

Gottfried, Knut [1]; Schubert, Ina [2]; Günnel, Heiko [2]; Schmidt, Ariane [2]

[1] FhG-IZM Chemnitz , Department Micro Devices & Equipment
[2]TU Chemnitz, Center for Microtechnologies, Professorship Microtechnologies

1 Introduction

CMP technologies are widely established for the realization of interconnect systems in advanced microelectronic devices. Nevertheless, ongoing research and development is necessary in order to meet the requirements of future device generations. The new (porous) low k materials need CMP processes with a very low down force due to their weak mechanical strength. In addition, porous low k materials require a cap layer whose selectivity within the polishing processes must be ensured. The continuous down scaling requires extreme low values for dishing and erosion. Moreover, slurries with a lower abrasive size or abrasive free slurries are needed for polishing of small features. Within the last year first investigations concerning the polishing of copper-barrier-stacks on different porous low-k material stacks have been performed at Center for Microtechnologies.

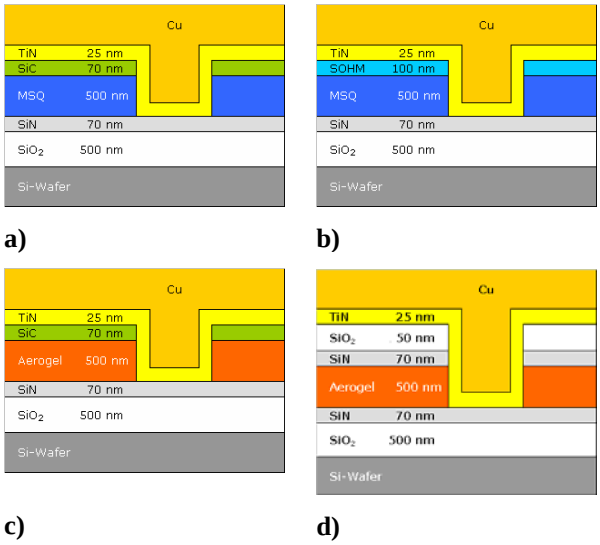

Fig. 1: Prepared layer stacks for CMP investigations
a) Porous MSQ with SiC cap layer
b) Porous MSQ with spin-on hard mask (SOHM)
c) Aerogel with SiC cap laye
d) Aerogel with SiO_2/SiN cap layer

2 Experimental

As low-k dielectrics porous silicon oxide (aerogel) as well as porous methylsilsesquioxane (MSQ) have been investigated. The used cap layers were SiC, SiO_2/SiN, and a MSQ-based spin on hard mask (SOHM). Four different stacks have been prepared as shown in figure 1.
Polish rate and selectivity were determined using blanket wafers with the appropriate films on top. The critical factors for the polishing process (dishing, erosion, defects, homogeneity) were examined on the patterned wafers by optical microscopy, SEM (plain view and cross section), and topography measurements after polishing. The polishing experiments have been carried out using two different sets of chemicals provided by two suppliers. Set #1 (supplier A) consists of one copper slurry (suitable for bulk removal and Cu-clearing) and one barrier slurry (designed for TaN/Ta, applicable for Ti/TiN). Set #2 (supplier B) consists of one Cu-bulk slurry, one Cu-clearing slurry, one barrier slurry (TaN/Ta, Ti/TiN), and a special pad cleaning solution.

3 Polish rates and selectivity

Chemicals set #1

The polish rate of the Cu slurry was determined with 200…350 nm/min (depending on the pattern factor) at 2 psi down force and 100 ml/min slurry flow. The selectivity of the Cu slurry regarding barrier and cap layer materials is summarized in table 1 (left part). For TaN/Ta barriers the selectivity is high as desired. In case of Ti/TiN however, the Cu slurry shows nearly no selectivity. Moreover, for the SOHM a serious mechanical impact was found (scratches). The barrier slurry was used at 1 psi down force and 200 ml/min slurry flow. The obtained polish rates (see table 1 right part) show a relatively low selectivity to Cu as well as to SiN and SOHM.

Tab. 1: Selectivity of Cu slurry and polish rates of barrier slurry from supplier A

Cu slurry Selectivity		***Barrier slurry*** Polish rate [nm/min]	
Cu : TaN/Ta	> 100	TaN	20 … 50
Cu : Ti/TiN	2	TiN	20 … 50
Cu : SiC	> 250	Cu	5 … 20
Cu : SiN	> 100	SiC	0.8
Cu : SOHM	10	SiN	30
		SOHM	30 … 40

Chemicals set #2

The polish rates for bulk and clearing slurry were determined with 900…1000 nm/min and 600… 650 nm/min, respectively. The polish parameters for both slurries were 2 psi down force and 200 ml/min slurry flow. Table 2 shows the obtained selectivity results.

Tab. 2: Selectivity results for Cu bulk and clearing slurry from supplier B

	bulk slurry	***clearing slurry***
Cu : Ti/TiN	> 14	> 10
Cu : SiC	> 55	> 600
Cu : SiN	> 110	> 60
Cu : SOHM	∞	∞

For both slurries the selectivity regarding Ti/TiN is low, but better than for the Cu slurry of supplier A. Regarding all dielectric cap layers both slurries exhibit an excellent selectivity. For the SOHM material once again scratches have been found. Table 3 summarizes the polish rates for the barrier slurry.

Tab. 3: Polish rates for the barrier slurry of supplier B (in nm/min)

TiN	150…200	SiC	3…4
Cu	40…50	SiN	6…8
SiO_2	7…8	SOHM	22…25

4 Polishing of Cu/TiN layer stacks on low k materials

The prepared layer stacks (fig. 1) were polished. Fig. 2 shows a typical result for the porous MSQ material after the polishing with chemicals set of supplier A. Due to the low selectivity of that Cu slurry regarding the TiN barrier a two step polishing has been applied. Platen 1 was used for Cu bulk removal and platen 2 for Cu clearing and barrier removal. The porous material has been found unchanged after polishing. Neither mechanical damages nor film delamination could be observed. Dishing values have been found in the range of 30…50 nm, measured on 10 µm wide lines with 4 µm spaces. The typical erosion was below 20 nm. No differences were found between the SOHM and SiC cap layer.

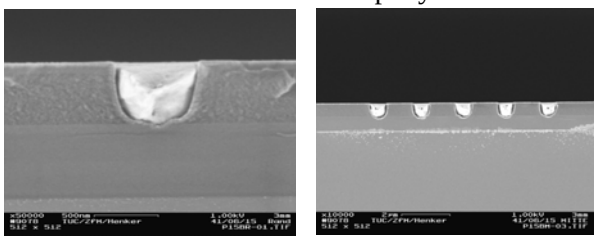

Fig. 2: SEM cross section after polishing a Cu/TiN layer stack on porous MSQ with SOHM cap layer (left picture) and with SiC cap layer (right picture)

Different results were obtained for the aerogel low k material. Polishing of that material results in a nearly complete loss of the dielectric stack in areas with a low pattern density. In areas with a high pattern density the low k stack seems to be unchanged as shown in figure 3. This behaviour was found independent from the consumables as well as from the used cap layer. This material definitively needs dummy Cu patterns or even lower down force to be polished defect-free.

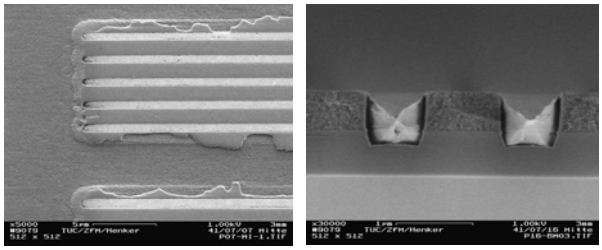

Fig. 3: SEM cross section after polishing a Cu/TiN layer stack on aerogel: delamination in areas with low pattern density (left picture), unchanged material between narrow structures (right picture)

4 Summary and outlook

The performed investigations were very first approaches to the polishing of low-k based interconnect systems. Promising results could be obtained with the porous MSQ material. For that material the next steps will be to figure out the critical down force and a further minimization of dishing and erosion.

Acknowledgement

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Modeling of Oxide CMP at Chip Scale

H. Wolf [1], R. Streiter [1], R. Rzehak [2], F. Meyer [2], G. Springer [2], T. Gessner [1]
[1] FhG-IZM Chemnitz, Dept. MDE
[2] Infineon Technologies, Dresden

1 Introduction

Chemical Mechanical Planarization (CMP) of oxide layers is an important process step during the formation of the Shallow Trench Isolation (STI) of present and future CMOS ICs. As for other processes, optimization by simulation is desired also for CMP, but because of the complex mutual interaction of many different concerns, physically based and experimentally verified general solutions are not sufficiently available yet.

CMP modeling takes place at various length scales. At wafer scale, FEM and BEM codes are often applied to optimize the pressure distribution across the wafer. The within-wafer non-uniformity of removal rates is reduced for very homogeneous pressure distributions that can be achieved by equipment optimization (e.g. wafer carrier, retaining ring etc.). For further improvements, the hydrodynamics of the pad-wafer contact have to be taken into account, too.

One main objective of CMP modeling at chip scale is to find out how the time dependence of material removal is affected by layout properties such as pattern density and dimensions of lines and spaces. Having determined the values of model parameters by evaluation of test patterns, predictions for arbitrary layouts should be possible with regard to the homogeneity of oxide dishing and nitride erosion across the chip. Thus, empirical CMP simulation at chip scale is applied not only for the determination of optimum process conditions, but also for layout optimization including the insertion of dummy structures (see e.g. [1]).

The evolution of feature topography during polishing is evaluated by solving the equations of linear elasticity to describe the interaction between polishing pad and wafer. Additionally, the pattern dependence of some parameters of the chip-scale models can be determined at feature scale. Moreover, elastohydrodynamic considerations at the length scales of pad asperities and slurry abrasive particles are necessary to explain how removal rates depend on process variables such as pressure and velocity.

This paper describes the representation of very extensive experimental data (about 8000 data points) at chip scale using an density-step height model, necessary extensions of the model, and the dependence of some of its parameters on process conditions.

2 Experimental

Mask set: Test structures have been prepared at Infineon Technologies using a CMP characterization mask set developed at the Massachusetts Institute of Technology [2]. A schematic representation is shown in Fig. 1. Within the density array (lower part), the layout density varies from 4 % to 72 % at a fixed pitch of 250 µm. The pitch array (upper part) consists of arrangements of equidistant lines and spaces. The pitch varies from 20 µm to 1000 µm at nearly uniform pattern density of about 50 %. The minimum feature size in both arrays is 10 µm.

Preparation of test wafers: 4 nm pad oxide and 110 nm silicon nitride were deposited on 200 mm silicon wafers followed by the patterning of 390 nm deep spaces. Afterwards, an 860 nm thick oxide layer has been deposited.

Planarization: The test wafers were polished using a Westech tool and the process conditions as follows:

Pad:	IC1000 + SUBA IV (stacked)
Slurry:	Klebosol 30 N 50
Pressure:	3, 4.5, and 6 psi
Back pressure:	1 psi
Table speed:	35, 58, and 80 rpm
Carrier speed:	110, 95, and 80 rpm
Center distance:	13.8 cm

The heights of the up and down areas have been measured on the center chip at all positions assigned to the given density and pitch values for equally incremented polishing times until complete nitride removal.

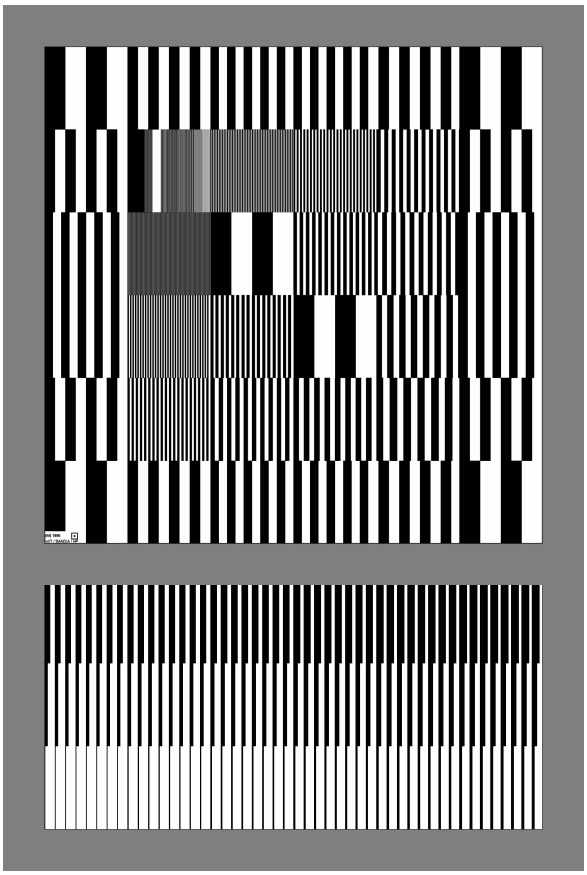

Fig. 1: Schematic representation of the test mask used. Up areas are white and down areas are black.

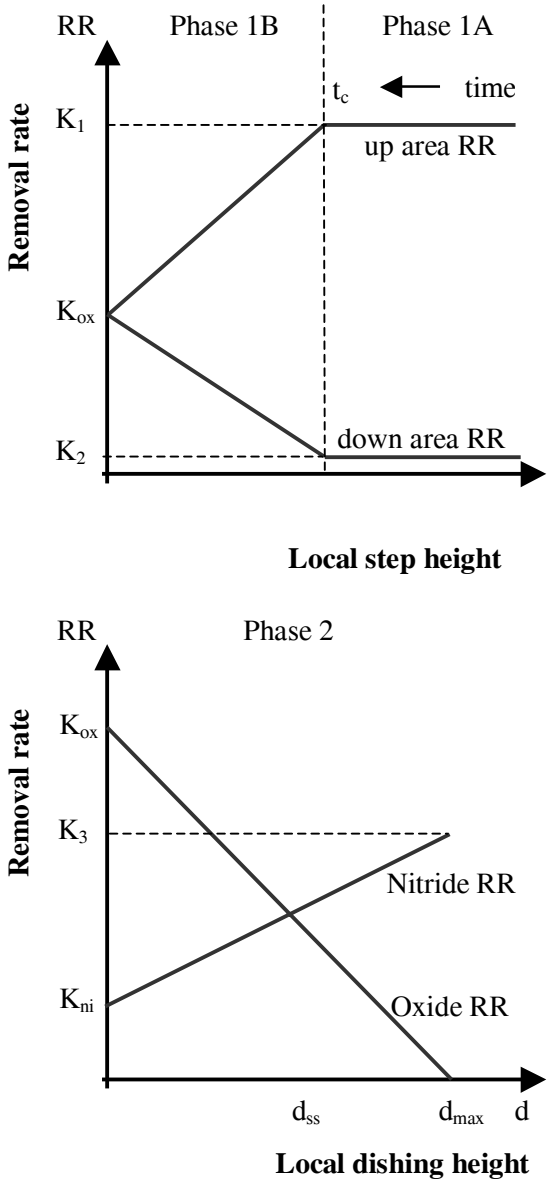

Fig. 2: Removal rate diagrams for oxide CMP [2]. Phase 1A indicates polish before the pad contacts the down area at the contact height h_c. Phase 1B indicates polish after down area has been initially contacted until nitride touch down followed by phase 2 indicating the simultaneous polish of oxide and nitride.

3 Modeling

3.1 MIT model

The density-step height model used for oxide CMP modeling at chip scale (hereafter referred to as the MIT model) is described in detail in [1] or in many other references listed at [2]. According to this model the oxide removal rates RR_u and RR_d of the up and down areas before nitride touch down depend inversely on effective density ρ and linearly on step height h as depicted in Fig 2 (phase 1A and phase1B). Similar dependences on density and dishing height d have been established for the removal rates RR_{ox} and RR_{ni} during the simultaneous polish of oxide and nitride. The rate equations are summarized in Eqs. (1) - (3).

K_{ox} and K_{ni} are the blanket removal rates of oxide and nitride, respectively. Within the frame of the standard MIT model, rate constants K_i and the contact height h_c are determined as

$$\text{Phase 1A:} \quad RR_u = K_1 \qquad RR_d = K_2 \qquad \text{for} \quad h \geq h_c \tag{1}$$

$$\text{Phase 1B:} \quad RR_u = K_1 + (K_1 - K_{ox})\frac{h}{h_c} \qquad RR_d = K_1 - (K_{ox} - K_2)\frac{h}{h_c} \qquad \text{for} \quad 0 \leq h \leq h_c \tag{2}$$

$$\text{Phase 2:} \quad RR_{ox} = K_{ox}\left(1 - \frac{d}{d_{max}}\right) \qquad RR_{ni} = K_{ni} + (K_3 - K_{ni})\frac{d}{d_{max}} \tag{3}$$

$$K_1 = \frac{K_{ox}}{\rho} \qquad K_2 = 0 \qquad K_3 = \frac{K_{ni}}{\rho_{ni}} \qquad h_c = \frac{a}{\rho} \qquad (4)$$

The effective density ρ at a spatial location on the die is defined as the weighted ratio of raised to total area within a weighting region. The raised area is determined from layout after adjusting for deposition with a bias which accounts for the increase/decrease in feature size due to deposition. A 2d Gaussian weighting filter characterized by a filter length FL was used to determine the effective density by weighting the influence of nearby cell densities for each cell. FL depends on consumables and process conditions and has to be determined together with K_{ox}, a, K_{ni}, and d_{max} from experimental data by least square fitting.

3.2 Model extensions

The representation of the experimental data can be improved further, if additional effects like edge rounding, non-vanishing initial down rates, and pressure dependent contact heights and dishing are taken into account. In doing so, the number of model parameters is increased. Moreover, the formulation of the model affects the value of the filter length. Thus, filter lengths from different models cannot be compared.

Contact height: Because h_c should depend on pressure P, a linear relation

$$h_c = \frac{a_1}{\rho} P \qquad (5)$$

has been assumed in this study as follows from Hookes Law.

Edge rounding: Freestanding narrow lines are removed faster than predicted by the standard MIT model. This is called edge rounding or corner rounding and may be due to an enhanced lateral erosion. The enhanced removal is observed only in the density array. In the pitch array the narrow lines are sufficiently screened and the enhancement is suppressed. Edge rounding is empirically modeled here as an enhancement factor to the rate K_1 and depends on line width L (up) and space S (down).

$$K_1 = \Psi \frac{K_{ox}}{\rho} \qquad \Psi(L, S) = 1 + [\Psi(L, \infty) - 1]\, f(S) \qquad f(S) = 1 - \exp\left(-\frac{S}{S_{c1}}\right) \qquad (6)$$

$$\Psi(L, \infty) = \begin{cases} L_c / L & \text{for } L \le L_c \\ 1 & L \ge L_c \end{cases}$$

Parameters L_c and S_{c1} have to be determined by evaluation of experimental data.

Non-vanishing down rate: It has been observed from experimental data that the down rate between wide-spaced lines is not zero in phase 1A as predicted by the standard MIT model. For narrow trenches the removal of the down rate is suppressed by screening. The same influence should act on the contact height, too, so that the same screening function g(S) is used for both. Moreover, the down rate is also decreased at higher densities what might be related to the increased lateral strain of the polishing pad. The decrease of the down rate results in higher pressure and an increased removal rate in the up area. For empirical modeling, exponential functions have been preferred to keep the number of parameters limited. Parameters b and S_{c2} have to be determined from experimental data.

$$K_2 = K_{ox} \exp\left(-\frac{\rho}{b}\right) g(S) \qquad h_c = \frac{a_1 P}{\rho} g(S)$$

$$g(S) = 1 - \exp\left(-\frac{S}{S_{c2}}\right) \qquad \leftarrow (7)\uparrow \quad (8)\downarrow$$

$$K_1 = \Psi\left[\frac{K_{ox}}{\rho} + K_{ox} \exp\left(-\frac{\rho}{b}\right) \frac{S}{L} (1 - g(S))\right]$$

Dishing: As for the contact height, the maximum dishing d_{max} is also expected to increase with pressure and for large nitride line space

$$d_{max} = d_1 P \qquad (9)$$

Parameter d_1 depends on selectivity, local pattern dimensions, and (visco-) elastic pad properties and can be calculated using an analytical dishing model (e.g. Eq. (14) of Ref. [3]). Unfortunately, our experimental data did not allow to resolve dependences other than on pressure.

4 Results and discussion

4.1 Blanket removal rates

For each combination of pressure and table speed the values of the model parameters have been determined by least square fitting of the corresponding up and down heights measured for every time step until complete nitride removal. For the blanket rates K_{ox} and K_{ni}, a linear dependences on pressure P and a sublinear dependence on relative velocity V could be identified as shown in Fig 3.

$$\frac{K_{ox}}{nm/s} = 0.7 \left(\frac{P}{psi}\right)\left(\frac{V}{m/s}\right)^{0.6}$$

$$K_{ni} = \frac{K_{ox}}{2.5} \qquad (10)$$

Selectivity remains constant at a value of about 2.5 for all process conditions investigated. No offset at P V = 0 has been observed.

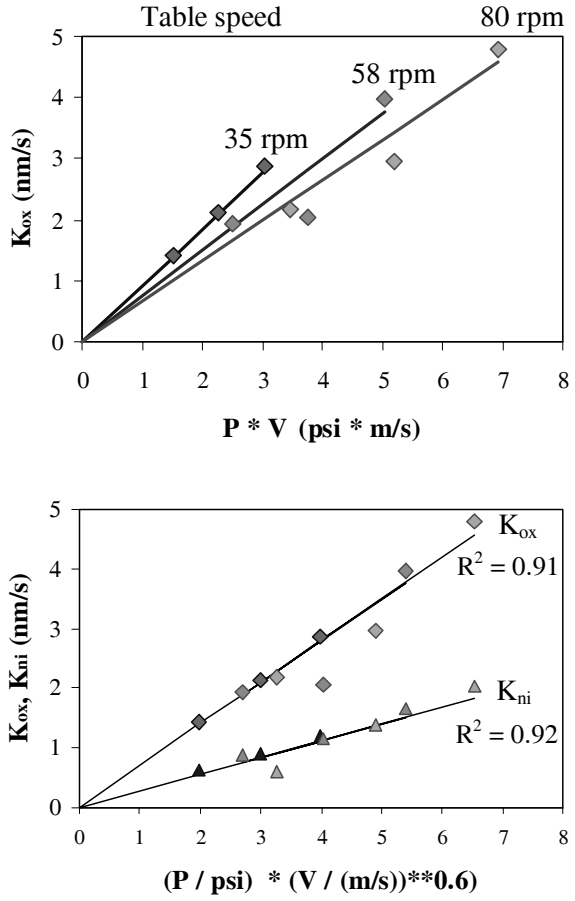

Fig. 3: Dependence of the blanket removal rates of oxide and nitride on pressure and relative velocity. The data points indicate the results of the individual fit for every set of process conditions. The lines show the simulation result based on Eq. (10).

The pressure exponent of unity is in accordance with Preston's findings for glass polishing [4], close to the value of 5/6 derived by Tseng and Wang [5], in agreement with the predictions of the comprehensive model developed by Qin et al. [6], but in contradiction to other models predicting values down to 0.5 [7]. Note that the derivation of the MIT model implies a linear dependence of blanket rates on pressure [2].

The value of the velocity exponent of 0.6 is between the limits of 1 for momentum transfer by direct solid contact between pad, abrasive particles, and wafer (boundary lubrication) and of 0.5 for hydrodynamic momentum transfer (hydrodynamic lubrication). A similar value of 0.65 was derived from experimental data by Hocheng et al. [8]. Eq. (10) can be transformed into a Prestonian representation

$$K_{bl} = K_p(V)\ P\ V \qquad K_p(V) \sim V^{-0.4} \qquad (11)$$

where K_{bl} stands for both blanket rates K_{ox} and K_{ni}. The Preston coefficient K_p is closely related to the coefficient of friction [9]. If the dependence of K_p on V/P is analyzed in terms of the Stribeck curve [10], the negative slope in Fig. 4 indicates that pad, abrasive particles, and wafer are in semi-direct contact characterized by elasto-hydrodynamic (mixed) lubrication. The decrease of K_p with increasing V/P is an expression of the growing influence of hydrodynamic effects in context with an increasing slurry film thickness [11].

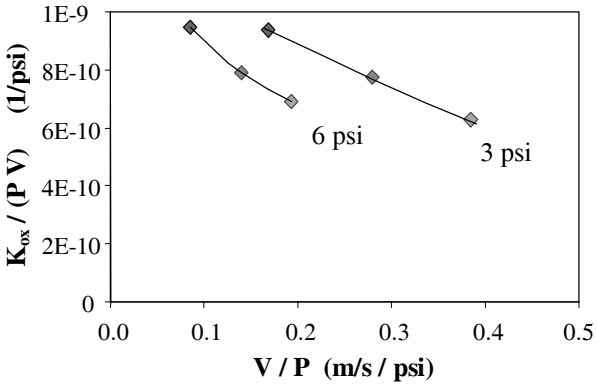

Fig. 4: Dependence of the Preston coefficient on V/P.

4.2 Filter length

The dependence of filter length FL, which characterizes the planarization behavior, on pressure and relative velocity is shown in Fig. 5. From the experimental data evaluated separately

for every set of process conditions, an upper limit of FL, a linear decrease with increasing pressure, and a sublinear increase with increasing velocity according to

$$\frac{FL}{\mu m} = 2250 - 115 \left(\frac{P}{psi}\right)\left(\frac{V}{m/s}\right)^{-0.4} \qquad (12)$$

were found. Combining Eqs. (10) and (12), a relation between FL, K_{ox}, and V is obtained

$$\frac{FL}{\mu m} = 2250 - 1.64E11\frac{K_{ox}}{V} \qquad (13)$$

which may be more general than the fitted results expressed by (10) and (12). The ratio of K_{ox} and V is equal to the material removed per sliding distance which decreases as velocity and slurry film thickness increase [11].

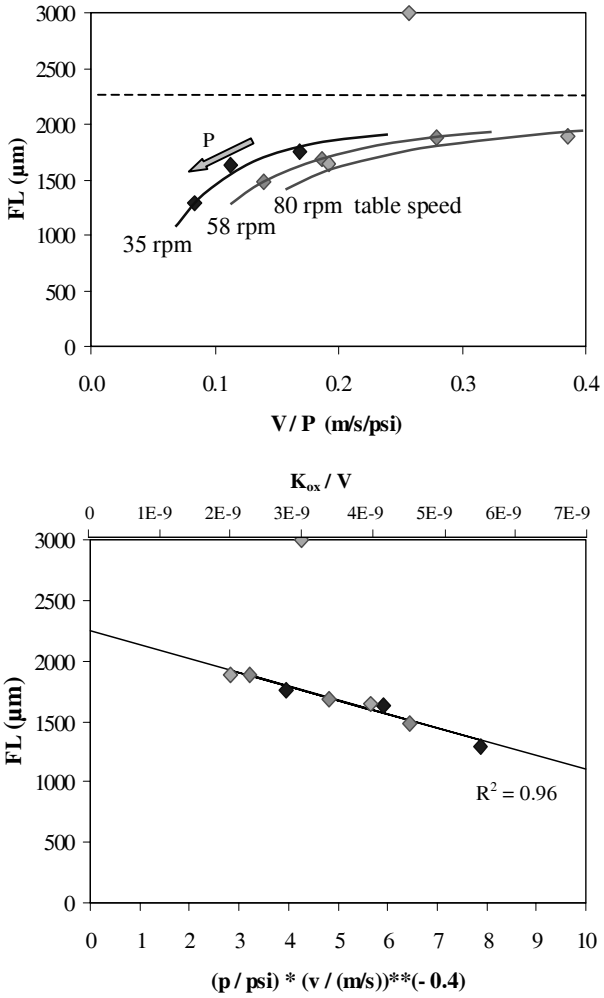

Fig. 5: *Dependence of the filter length on pressure and linear velocity. The data points indicate the results of the individual fit for every set of process conditions. The curves show the simulation result based on Eq. (12).*

The slurry film thickness h can be estimated from the case of full hydrodynamic lubrication, as

$$h \sim \sqrt{\frac{\mu V}{A P}} \qquad (14)$$

[8,12], where µ is the dynamic viscosity of the slurry and A is the area of the wafer. A similar dependence on V/P can be seen in the upper frame of Fig. 5. At low values of V/P there is direct solid contact all over the wafer surface resulting in nearly homogeneous removal and bad planarization behavior. If the average slurry thickness increases with increasing V/P, there is still direct solid contact with strong mechanical erosion at exposed surface positions, but already hydroplane sliding at positions with greater pad to wafer separation. Thus, planarization is improved. If the slurry film thickness is increased further, the number of positions with direct solid contact decreases and planarization cannot be improved further. Changing contact mode and limited stiffness of the pad cause FL to level off at increased values of V/P.

4.3 Parameter extraction

Because the parameter extraction for every individual set of process conditions resulted also in values having both less significance than K_{ox}, K_{ni}, and FL and no clear correlation to P and V, a common fit of the whole data set has been performed based on Eqs. (10) and (12) and constant values for the remaining parameters of the extended model. The results are collected in Table 1. Using this parameter set, the rms error is 20 nm.

Parameter	Unit	Value
K_{ox}	nm/s	$0.7\ (P/psi)\left(\frac{V}{m/s}\right)^{0.6}$
L_c	µm	83
S_{c1}	µm	1160
b		0.52
S_{c2}	µm	65
d_1	nm/psi	51
FL	µm	$2470 - 148\left(\frac{P}{psi}\right)\left(\frac{V}{m/s}\right)^{-0.4}$
a_1	nm/psi	14
K_{ni}	nm/s	$K_{ox}/2.5$

Table 1: Parameter set for the extended model.

4.4 Total indicated range

The total indicated range (TIR) is a quantitative measure for the planarization achieved by the polishing process. The TIR is defined as the maximum possible vertical topography difference within a given area (chip or part of a chip). Using the standard MIT model, the TIR can be calculated [13]. For sufficiently long polish times when all step heights have become small against the contact height, the TIR depends only on the initial step height h(0) and on the variation of the effective density $\Delta\rho = \rho_{max} - \rho_{min}$ according to

$$\mathrm{TIR}(t) = h(0)\,\Delta\rho \quad \text{for} \quad t >> h(0)\frac{\rho_{max}}{K_{ox}} \qquad (15)$$

For shorter polish times the TIR is above this long-time limit. But even for long polish times, Eq. (15) is only a crude approximation because local pattern effects are ignored.

If the extended model is used, the issue is more complicated. Both edge rounding and non-vanishing down rates promote the early erosion of down areas at low density and, therefore, tend to increase the TIR in the density array. Figs. 6 and 7 show that, although polish times are sufficient, the experimental TIR is more or less

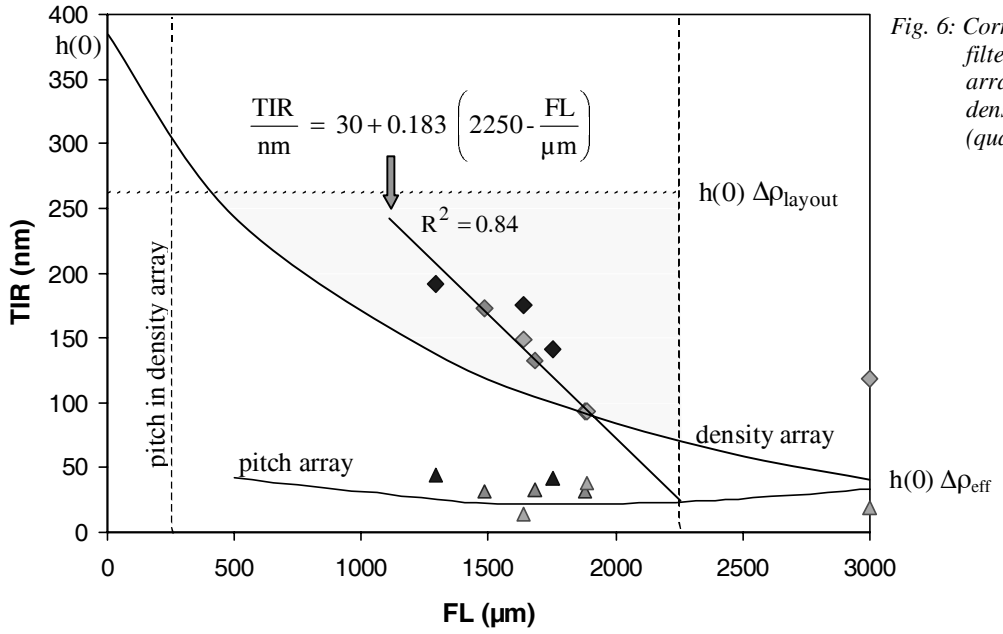

Fig. 6: Correlation of TIR and filter length for the pitch array (triangles) and the density array (quadrangles).

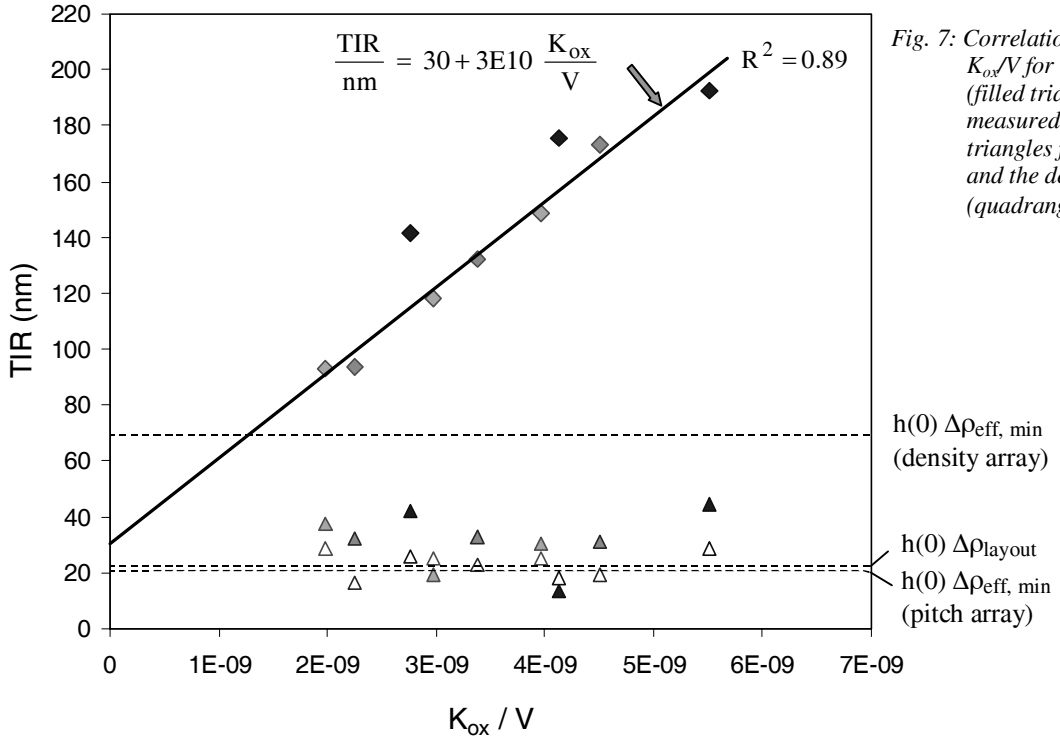

Fig. 7: Correlation of TIR and K_{ox}/V for the pitch array (filled triangles for measured TIR, open triangles for simulation) and the density array (quadrangles).

above the predictions of Eq.(15).

Because effective densities strongly depend on filter length, a correlation between TIR and FL is expected. Evaluation of measured heights *only for the density array* leads to

$$\frac{\mathrm{TIR}}{\mathrm{nm}} = 30 + 0.183 \left(2250 - \frac{\mathrm{FL}}{\mu\mathrm{m}} \right)$$

$$= 30 + 3\mathrm{E}10 \frac{K_{ox}}{V} \qquad (16)$$

where the second relation follows from (13).

The TIR of the density array for any individual process is found in Fig. 6 within a range determined by the maximum filter length, the initial step height, and the variations of layout density and effective density. For the process with 3 psi down pressure and 80 rpm table speed, the TIR is practically at its lower limit and cannot be reduced further with the given set of consumables. Also in the extended model, a greater value of FL corresponds to a lower TIR indicating improved planarization.

Fig. 7 shows the dependence of the TIR on the ratio of K_{ox} and V which is equal to the material removed per sliding distance. The TIR of the density array increases for more aggressive removal (e.g. higher P) and planarization gets worse. No such dependence has been found within the pitch array. The TIR varies here by some tens of nm. This is not only caused by statistical scattering of the measurements, because measured and simulated data follow the same trend.

5 Conclusions

- The MIT Model is suitable to simulate topography evolution at chip scale. Density and pitch dependent extensions such as edge rounding and non-zero down rates can reduce rms errors further.
- Oxide removal rates show a linear dependence on down force and a sub-linear dependence on relative velocity. The non-Prestonian behavior is due to changed pad-wafer contact caused by velocity dependent slurry film thickness.
- Filter length depends on details of the model and on process conditions. An upper limit and a linear dependence on material removal per sliding distance (K_{ox}/V) were found for the processes investigated.
- Within the density array the TIR depends linearly on K_{ox}/V. The TIR of the pitch array is nearly constant.

Acknowledgement

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Extraction of k_{eff} of multilayer intermetal dielectric stacks by FEM simulation

Schulze, Knut; Schulz, Stefan; Gessner, Thomas
Chemnitz University of Technology, Center for Microtechnologies, Chemnitz

1 Introduction

The continuous reduction of geometrical dimensions in microelectronics is the reason for a super proportional increasing of unwanted electrical effects, working against a further acceleration of IC clocking. Dominant forces are parasitic capacitances between, and the resistivity along, the metal lines in backend interconnect systems (characterized by the R·C time delay). Substitution of aluminium by copper reduces R, because of the higher conductivity offered by copper. The reduction of C is basically possible by reducing the k-value of the inter- metal- and inter-layer dielectrics.

$$C = k_0 \cdot k_{eff} \cdot \frac{A}{d} \qquad (1)$$

Newly developed films with a lower k-value (low-k materials), than the conventionally used SiO_2 for dielectrics (k=4.2), have been introduced more or less successfully in copper-damascene technology in the last few years.
These films have generally reduced density and polarizability and are often porous which implicates deteriorated mechanical, thermal and chemical properties. For damage-free treatment during process steps like patterning or resist stripping, or to improve adhesion, additional films are necessary. In the end, these functional layers influence the effective k-value between the metal interconnects. Characterization of low-k material requires indication of the true working k-value (k_{eff}) of the functional stack consisting of low-k and additional layers.

2 FEM simulation of k_{eff}

Figure 1 shows a schematic cross section of a damascene architecture. The low-k material is vertically and horizontally enclosed by several other dielectric materials needed for poresealing and patterning processes. The effective k-value of the low-k material, SiO_2 spacer, hard mask and stop layer should be estimated at all. The k-value of every single layer is known.

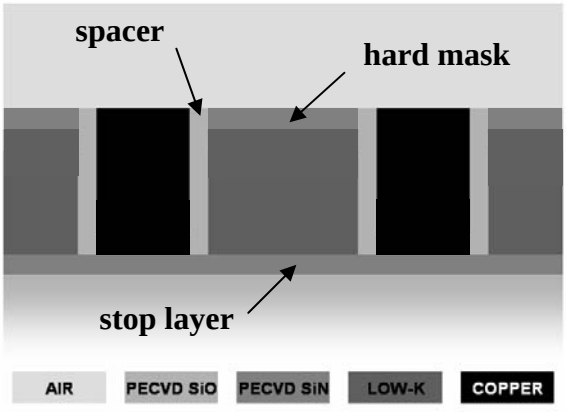


Fig. 1: Schematic cross section of a damascene architecture with application of a spacer material

Via application of a static FEM analysis, the resulting capacitance C_{all} between the two copper lines within this system was calculated. A sample of the formed field with its equipotential lines is shown in figure 2.

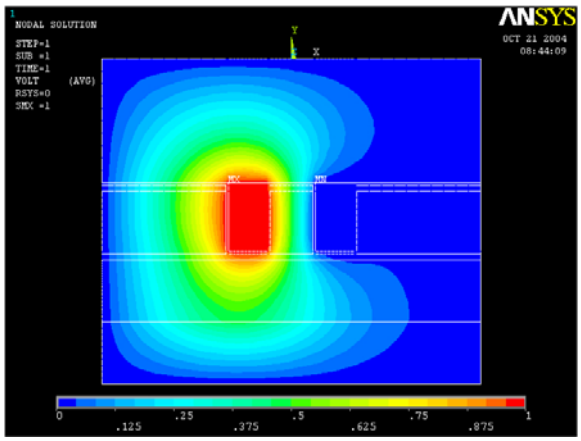


Fig. 2: Equipotential lines simulated via FEM analysis

In the the next step, the simulation model was simplified. All functional layers concerning to the low-k material were merged and furnished

with the same k-value k_{mat}. By the usage of a binary search algorithm the k_{mat} was determined, which results in the same C_{all} for the modelled simlified architecture. In figure 3, the according k_{eff} is the k-value of the intersection point of both graphs.

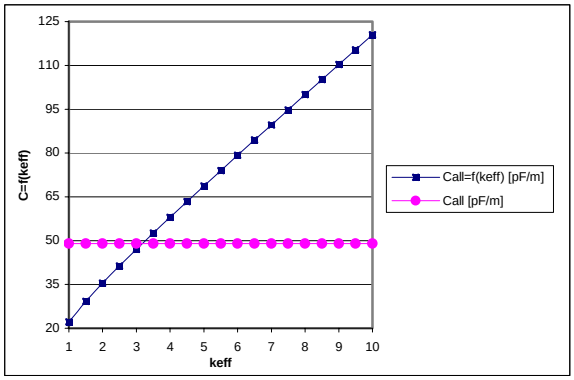


Fig. 3: Simulated C_{all} (multilayer and merged dielectric stack)

The chosen procedure of simulation allows observation of the behaviour of the system without paying attention to the leakage field. We can truly estimate the influence of the electrical properties of additional layers, of the geometrical dimensions and of the architecture itself. In figure 4 the interconnect distance and interconnect width were changed.

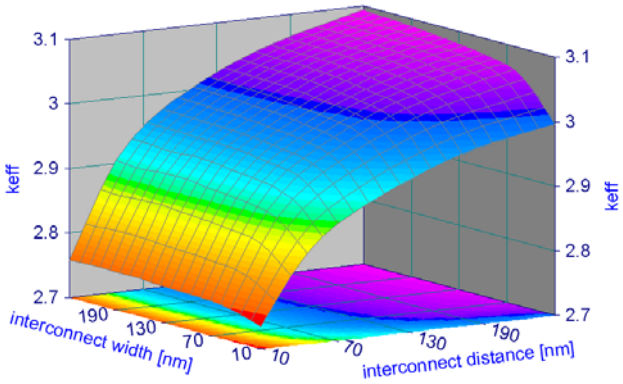


Fig. 4: Example for the effect of variation of geometrical dimensions on k_{eff}

Additionally to the described simulation approach, these FEM analyses were used to verify electrical measurements on prepared samples. The real geometrical dimensions are necessary as an input for the interconnect system to be modelled. FIB preparation combined with SEM is a suitable technique to determine the geometrical parameters at cross sections. An example of such a preparation is shown in figure 5.

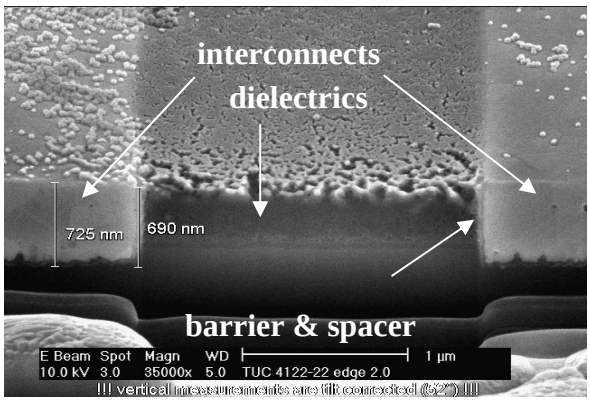


Fig. 5:FIB preparation of a copper damascene architecture

The porous spin on SiO_2 Aerogel, developed at the Centre for Microtechnologies, was used as dielectric, CVD TiN as barrier, Copper as interconnect and PECVD SiO_2 as spacer material.

Development of a high resolution acceleration sensor

R. Schmiedel[1], D. Billep[1], S. Kurth[3], H. Wolfram[1], K. Hiller[1], T. Gessner[1], W. Dötzel[1], W. Günther[2], T. Aurich[2], C. Dittrich[2]

[1] Chemnitz Univ. of Technology, Center of Microtechnologies, Chemnitz

[2] GEMAC mbH, Chemnitz,

[3] Fraunhofer Institute Reliability and Microintegration, Department Micro Devices and Equipment, Chemnitz,

1 Introduction

Presently a new bulk micromachined multi-use acceleration sensor is under development. The sensor should provide a measurement range of ± 8 g, a resolution of 500 µg at 200 Hz bandwidth, and a bias stability better than 100 mg. A differential capacitor design (Fig. 1) based on bulk micro machined and wafer bonded elements is chosen for the sensor, because this approach supplies a large inertial mass in combination with small capacitor gaps. So the sensor can reach a high sensitivity. The differential capacitor arrangement can be used both for detection of small deflections of the movable mass and for force compensation using electrostatic forces. The closed-loop operation principle (Fig. 2) enables a high resolution.

2 The sensitive element

In contrast to a former development of acceleration sensors a new type of spring-mass-system has been designed, simulated and patterned (Fig. 3 and 4). The seismic mass is suspended in the wafer frame by two vertical torsional beams, which have a nearly rectangular cross-section. This shape of the springs can be realised using (100)-Si and wet etching in KOH with a symmetrical etch process from both sides, if the edges of the mask are aligned with an angle of 45° to the [110] direction (wafer flat). With this process, the dimensions of the spring, resp. the spring width, can be easily controlled using a microscope. In order to reduce damping, fluidic channels have been integrated into the surface of the seismic mass (Fig. 4).

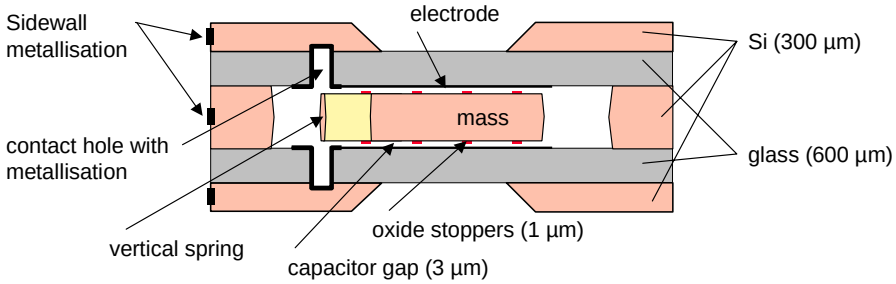


Fig. 1: Cross-section of the acceleration sensor

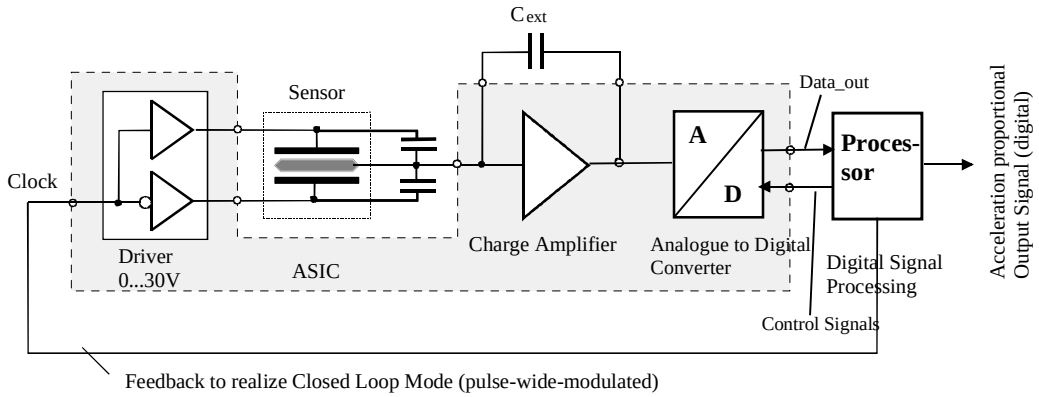


Fig. 2: Feedback control scheme of the acceleration sensor

The dimensions of the spring in Fig. 3 are 660 µm in length, 300 µm in height and 16 µm in width, resulting in a torsional resonant frequency (1st order mode) of about 400 Hz. Fig. 3 shows a FEM simulation of this primary vibration mode, which is used for the acceleration force measurement. The 2nd and 3rd modes, which occur at about 2 kHz and 2.7 kHz, are in-plane-modes, which do not contribute to the detection signal. Higher order vertical modes, which can cause detection signal errors, have frequencies of more than 18 kHz. The fabrication technology of the middle wafers uses 4 masks on each side, creating the capacitor gap, the oxide stoppers, the fluidic channels, the springs and mass.

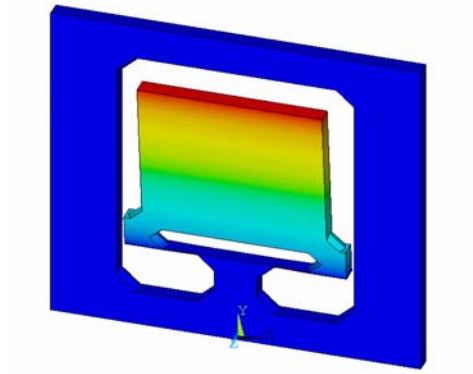


Fig. 3: FEM simulation of the 1st order mode

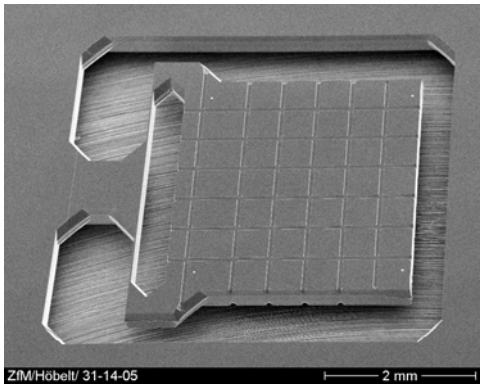


Fig. 4: SEM picture of the spring-mass-system

3 Packaging

The cover wafers must provide the fixed electrodes, hermetic electrical feed through and wire bonding areas. In order to achieve low parallel capacitances of the wafer frame, glass (Hoya SD2) has been chosen for the substrate material. The electrical connections to the outer side are realised using ultrasonic drilled holes, which are covered by Si islands, and therefore are hermetically sealed. Al is sputtered in these holes via a hard mask, this way connecting the fixed electrode areas (Al) with the Si islands. The mounting of the sensors is done by two subsequent Anodic bonding processes with temperatures of 400°C and voltages of 300 ... 350 V. The second bonding step can be carried out in a vacuum chamber in order to reduce damping. Afterwards the compound is diced into pieces, and the sidewall metallization is realised. Fig. 5 shows complete sensors. Sensor and electronics are packaged together in a waterproof box, which is shown in Fig. 6.

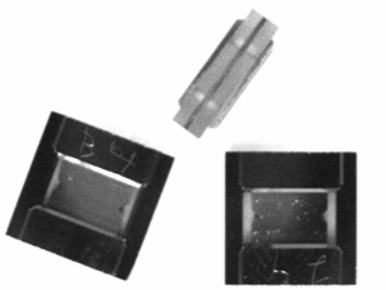


Fig. 5: Acceleration sensor chips (7 x 7 x 2.1) mm³

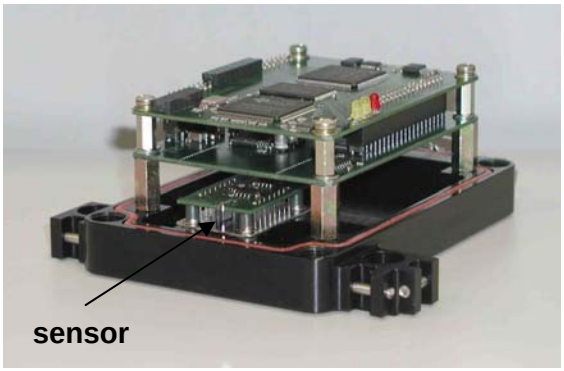


Fig. 6: Ground plate with mounted inner box and electronics

4 Results

Several sample tests of sensors prototypes together with electronics have been carried out. Four-point-tumble tests as well as tests on the rotation table have shown that both measurement range and resolution meet the specification. Typical measured values of bias are 10…40 mg. The bandwidth was measured to be 210…220 Hz. All sensors passed shock tests with loads higher than 80g over 5ms, vibration tests with 0.04 g²/Hz, and full temperature tests from -40°C to 70°C. Based on these promising results, a second phase for development of prototype II is planned.

This acceleration sensor will be applied e.g. in a cooperation project with FARA New-Tech Development Co. in Xián (China).

The Bonding and Deep RIE (BDRIE) technology approach for high aspect ratio sensors and actuators

K. Hiller[1], M. Küchler[2], M. Dienel[1], T. Gessner[1,2]
[1] Chemnitz University of Technology, Center of Microtechnologies, Chemnitz
[2] Fraunhofer Institute Reliability and Microintegration, Department Micro Devices and Equipment, Chemnitz

1 Introduction

For several years, high aspect ratio technologies based on deep dry etching have been used and commercialised e.g. for fabrication of inertial sensors. The typical height of structures varies between 12 µm (epipoly-surface technology) and up to 50 µm for SOI, SCREAM and other related technologies. These technologies use isotropic underetch steps in order to release the movable structure, therefore a lot of design restrictions concerning the size and arrangement of gaps and beams exist, movable structures must have the typical holes for underetching, and the size of the vertical gap is restricted to some microns. Alternative approaches use dry etching steps in combination with bonding processes. The basic idea of BDRIE, characterised by bonding of two wafers with pre-patterned vertical gaps and subsequent RIE trench etching of the active layer, has already been described before (e.g. [1]). We have investigated two special approaches with some variations of this Bonding and Deep RIE technology, which are described and discussed below.

2 BDRIE APPROACHES

Both glass and silicon can be used for the basic wafer. Fig. 1 shows the scheme of the anodically bonded silicon-glass compound (BDRIE A). The silicon layer contains the movable structure as well as drive and detection electrodes for lateral movement. Wire bonding pads on top define the electrical contact areas. A flat groove for vertical movement and detection has been etched from the backside of the silicon wafer prior to bonding. The glass wafer contains detection electrodes for vertical movement. The access to these underlying electrodes can be provided either by contact holes or by pressure contacts to the silicon islands. These areas are electrically insulated by air gaps in lateral direction and the glass substrate in vertical direction. Hence, depending on the gap size, the parasitic capacitance is very low. With this approach it is possible to create HARM structures which can be actuated and sensed both in lateral and vertical direction.

For the directly bonded silicon-silicon compound (Fig. 2), the groove is preferably etched into the silicon basic wafer. Thick thermal oxide layers are used for vertical insulation and air gaps for lateral insulation. Although the integration of vertical detection electrodes would be possible with a high effort, we have not tested this option, therefore this approach is suitable for structures with lateral drive and detection capacitors.

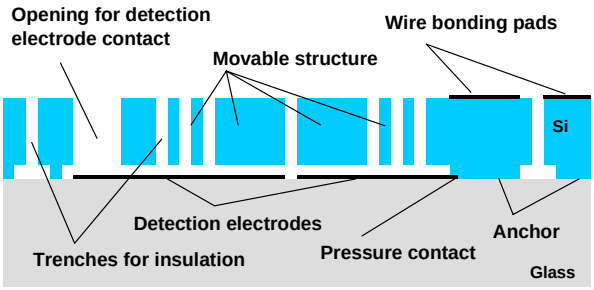


Fig. 1: BDRIE A: Silicon-glass

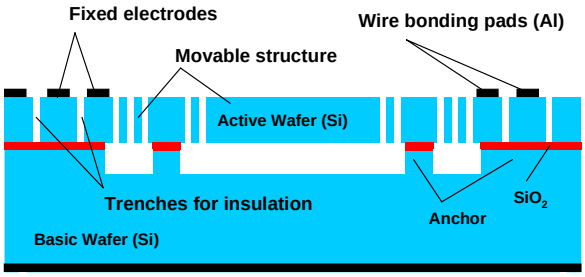


Fig. 2: BDRIE B: Silicon-Silicon

2.1 Wafer bonding

The wafer bonding processes for basic and active wafers have been carried out using a commercial wafer bonding equipment (SB6, Karl Suss). In case of anodic bonding, we used Pyrex glass for

the basic wafer. A patterned aluminium bond electrode on the backside of the glass, forming a grid structure aligned to the chip frames enables a reduction of bond voltage down to about 300 V. Bond temperatures were in the range of 360 ... 400°C. For direct bonding we normally utilise a hydrophilic regime: RCA cleaning, pre-bonding at room temperature with a bond tool pressure of 3 bar, and subsequent high temperature annealing (1000°C, 5 hours). With both processes we have successfully bonded minimum (anchor type) areas of (100 x 100) µm² and chip frames of 150 µm. During the bond process the pre-etched cavities are sealed. Several investigations [2] have shown that it is advantageous to seal the cavities in vacuum at a pressure of about 1 mbar.

2.2 Active layer thickness

The active layer thickness is suitable in the range from 30 µm to 300 µm with an optimum value depending on the specific application. Due to the specific of the BDRIE process, some limiting conditions must be taken into account, too. Before trench etching, the active layer forms a membrane over the recess, which undergoes a deflection depending on the thickness, the gap area and the pressure inside the cavity (see Fig. 3) [2]. This deflection should be as small as possible [nm range], especially in case of high temperature annealing, when silicon can undergo a plastic deformation, which is irreversible. Therefore during high temperature annealing a thick wafer is required.

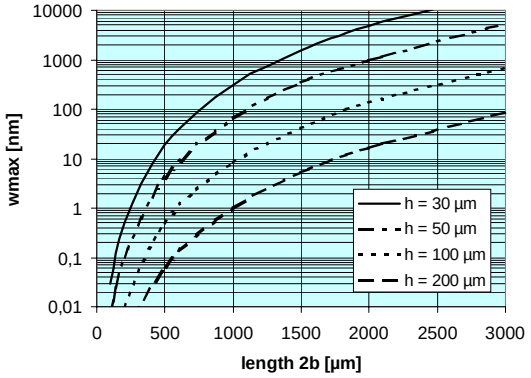


Fig. 3: Maximum deflection in the middle of a square with side length 2b (pressure difference of 1 bar)

Thinning of the active layer can be achieved

a) by grinding and polishing,
b) by etching and polishing
c) by bonding of an SOI wafer and etching the handle wafer.

Both methods b) and c) have been tested successfully. During thinning, the maximum deflection is increased, but should not exceed 1 µm in order to enable the stepper lithography for the trench mask. In case the recess is too large, special support posts (anchor type) can be introduced (see Fig. 2).

2.3. Trench etching into cavity

The trench etching process should provide a highly anisotropic etch behaviour and a good homogenity, a sufficient selectivity to mask and moderate etch times. Nowadays the time multiplexed deep etch (TMDE) technique is widely applied, which is based on a repetitive sequence of deposition and etching steps. During deposition C_4F_8 is used to form sidewall passivation, whereas SF_6 is used to perform etching. This work was performed using a Surface Technology Systems multiplex ICP. The high density ICP plasma source is powered by an rf generator supplying 1 kW at 13.56 MHz. Bias is generated at substrate electrode by means of a pulsed rf generator operating at 380 kHz (LF processes, especially for wafers including isolating substrates). The trench profile of the LF precision process, which can be used for a layer thickness up to 100 µm, is shown in Fig. 4.

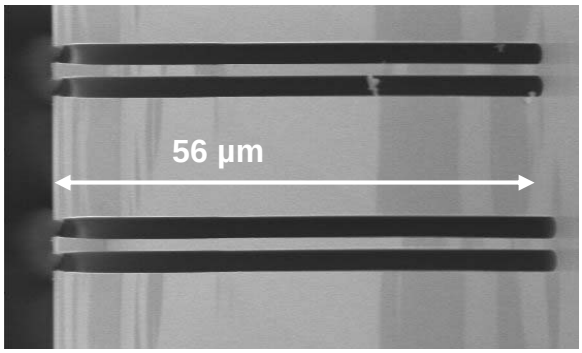
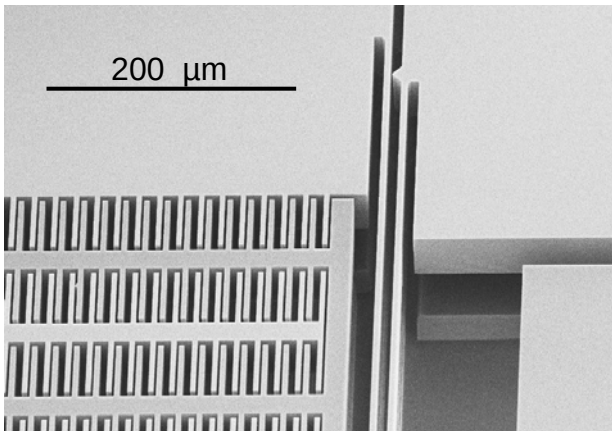
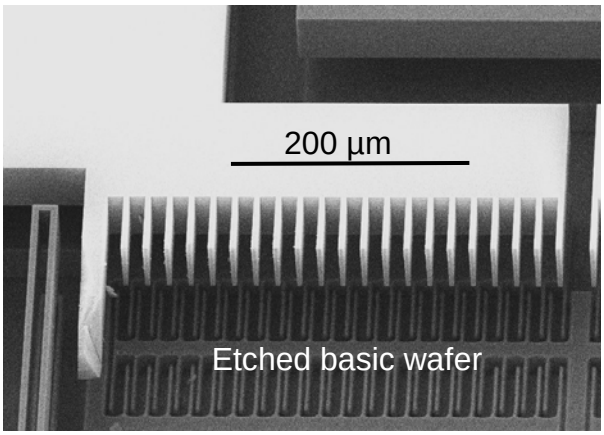


Fig.4: Trench profile of the precision LF process (*Sidewall angle 90.2 … 90.3°)*

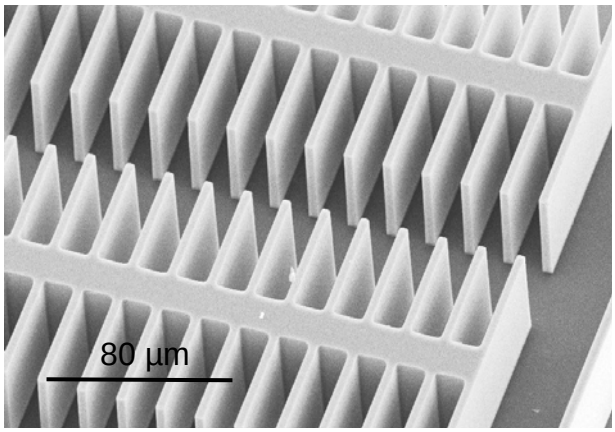
The trench etching process has to be continued until all trenches have reached the cavity, thus way the structure is released. Usually, due to the aspect ratio depending etching (ARDE), the wider trenches reach the cavity first. When the process goes on, the silicon substrate of the basic wafer is etched, too. In case of a glass substrate it is useful to introduce a conducting screen electrode underneath the trenches in order to avoid backscattering of the ions and backside etching [2]. Fig. 5 shows SEM pictures of typical structures fabricated with the Silicon-Silicon BDRIE approach.



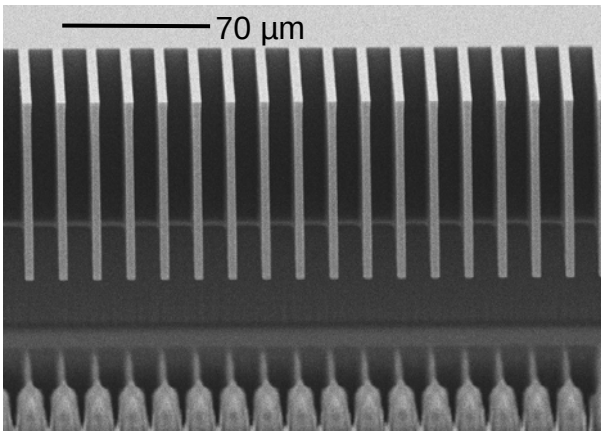
a) top view



b) view on bottom after removing of structure



c) view on backside of structure (50 µm thickness)



d) view on fixed part of a comb drive (75 µm thickness)

Fig. 5: SEM pictures of fabricated structures (acceleration sensor)

3 Applications

The BDRIE approach can be applied for all types of inertial sensors, e.g. acceleration sensors, gyroscopes, vibration sensors and resonators, but also for actuators like torsional micromirrors.

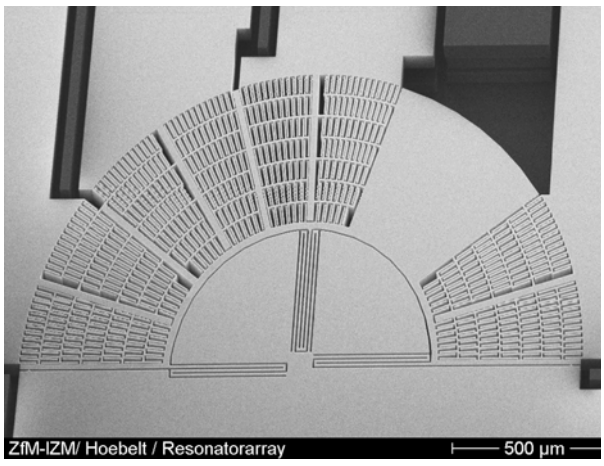


Fig 6: Acceleration sensor

For example of silicon-silicon compounds, Fig. 10 shows part of an asymmetric central fixed acceleration sensor [3]. In this example, the structure height is 50 µm, the smallest trench width is 2 µm and the maximum free standing membrane (area around the moving segment) is about (1.6 x 1.6) mm².

BDRIE structures can be packaged e.g. using a silicon cover wafer and either polymer bonding, direct bonding or glass frit bonding [2].

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[1] Capuz, C.; Ridley, J. (Honeywell International Inc.): *Thin Silicon micromachined structures*, international patent publication WO 02/051743 A3, 2001

[2] Hiller, K. et al.: Bonding and Deep RIE – a powerful combination for high aspect ratio sensors and actuators, submitted to SPIE 5715, San Jose (CA), Jan. 2005

[3] Billep, D.; Dienel, M.: *Acceleration sensor*, German patent DE 10 2004 046 411.1, 2004

Novel high precision micromachined gyroscope

K. Hiller[1], D. Billep[1], M. Küchler[2], T. Gessner[1,2], W. Dötzel[1], W. Geiger[3], U. Breng[3], P. Leinfelder[3], W. Gutmann[3] et al.

[1] Chemnitz University of Technology, Center of Microtechnologies, Chemnitz

[2] Fraunhofer Institute Reliability and Microintegration, Department Micro Devices and Equipment, Chemnitz

[3] LITEF GmbH, Freiburg

1 Introduction

Within the project "EKOFEM" a novel high precision silicon gyroscope fabricated by a special high aspect ratio technology is under development. The planar structure exhibits two in-plane vibration modes for drive and detection. Comb drive electrodes are used to force the resonator to vibrate with it's primary mode resonance frequency, and differential detection electrodes measure the vibration amplitude of the secondary mode caused by Coriolis forces. Due to the very high requirements to accuracy and resolution (bias stability 10°/h, angle random walk $< 0.3°/\sqrt{h}$), it is necessary to compensate fabrication tolerances as well as other influences (e.g. thermal drift). This is achieved by electronics; the control loops are implemented in a digital signal processor. The working principle and the basics of design and technology have been described in the 2003 report and in [1], [2].

2 Fabrication of prototypes with an optimised design

The gyroscope is fabricated by a new technology approach based on SOI-wafers with a buried cavity (see Fig. 1). The thickness of the active layer is 50 µm. Deep dry RIE etching (time multiplexed deep etch technique with STS equipment) via photoresist mask is used for the trench patterning process. Much effort has been spent on the optimisation of this trench etch process (rectangular and symmetric trench profile, reduced ARDE and notching). Presently a trench angle of 90.2...90.3° has already been achieved (Fig. 2), a further reduction is aspired. In order to avoid notching the Bias voltage is generated at substrate electrode by means of a pulsed rf generator operating at 380 kHz (LF process, especially for SOI processing).

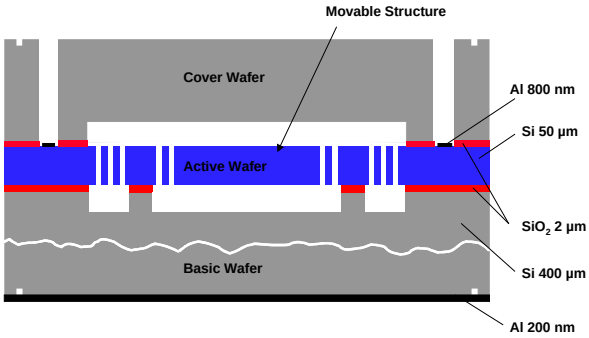


Fig. 1: Schematic cross section of the sensor

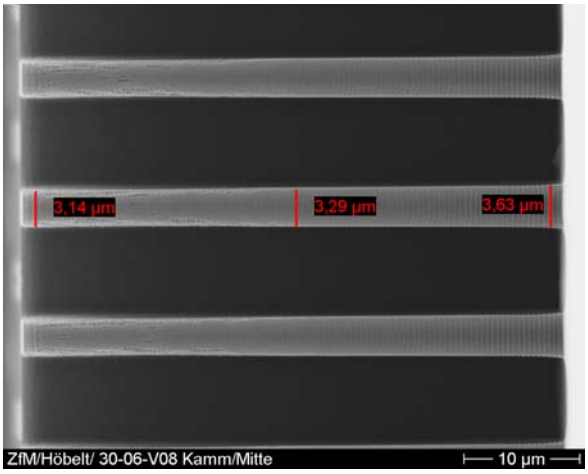


Fig. 2: View on the front end of a comb drive (SEM)

Targets of design optimisation have been

- reduction of frequency difference between excitation and detection mode
- ratio between mass and stability of the frames
- high linearity
- low bias.

Different designs including single and dual linear configuration have been developed and fabricated. Fig. 3 and 4 show details of the excitation comb drive as well as the detection capacitor.

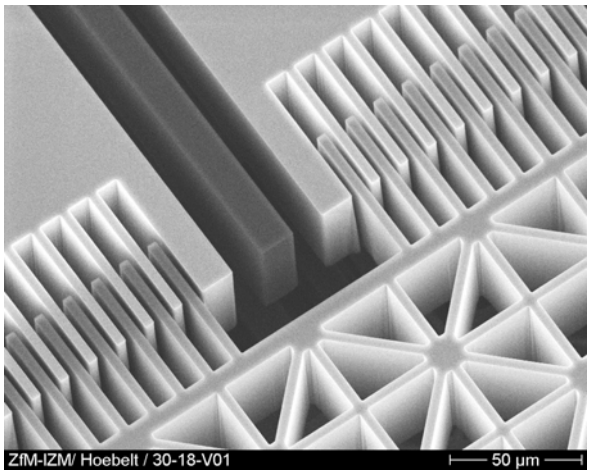


Fig. 3: Detail view (SEM) on the comb drive

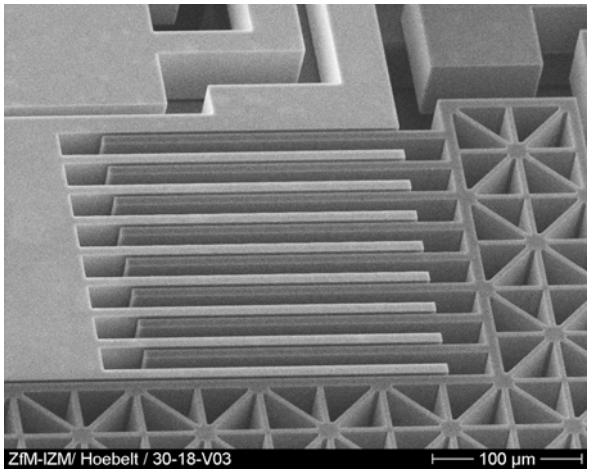


Fig.4: Detail view (SEM) on the detection system

The smallest trench width is 2.5 µm, the widest trenches are about 30 µm. The resonant frequencies of the resonators are about 9.2 kHz and 9.4 kHz.

3 Packaging

For hermetic encapsulation of the resonators, a Si cover wafer with thermal oxide is used (see Fig. 1). A special direct bonding regime has been developed and applied. Fig. 5 shows a cross section of such a sensor compound. With this bonding approach, hermetic sealing of the sensors with residual cavity pressure as low as 1 Pa has been achieved.

4 Measurements

Both uncapped and capped sensors have been tested at LITEF GmbH Freiburg (see Fig. 6). The resonators show very high quality factors (up to 120,000 at a pressure of 1 Pa for excitation mode). Over a time period of 15 months no change of the Q factor was observed [2]. Other promising measurement results of the capped sensors presented in [2] are the very low noise (< 0.09°/√h) and a bias stability over temperature of presently 27°/h, which is expected to be reduced to < 5°/h with the optimised design.

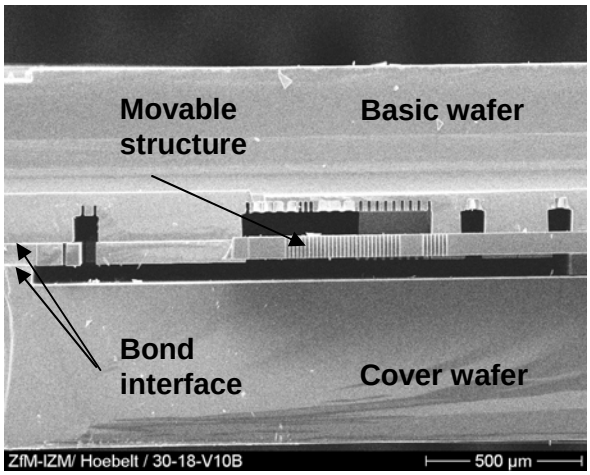


Fig.4: Cross section (SEM), chip face down

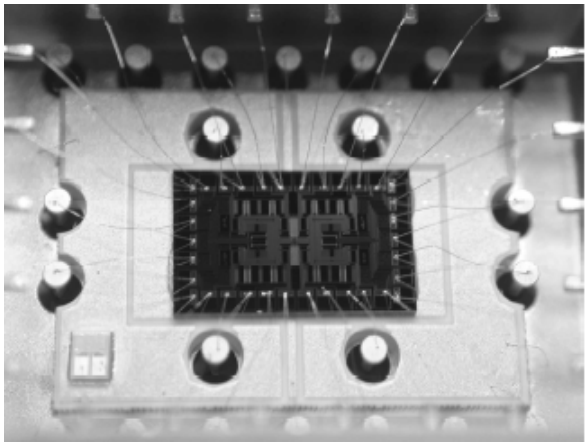


Fig 6: Photo of assembled chip (dual linear configuration)

The sensors can cover a measurement range of ± 200°/s (realised) up to ± 5000°/s, the scale factor non-linearity (maximum error) is 600 pm. With the fabricated prototypes II the target of the EKOFEM project can be fulfilled.

References

[1] Geiger, W. et al.: *The micromechanical Coriolis Rate Sensor µCORS II*, Symposium Gyro Technology, Stuttgart 2003

[2] Geiger, W. et al.: *Test results of the* m*icro-mechanical Coriolis Rate Sensor µCORS II*, Symposium Gyro Technology, Stuttgart 2004

Modeling and Simulation of MicroElectroMechanical Systems

Jan Mehner[1], Thomas Gessner[1], Detlef Billep[2], Wolfram Dötzel[2]
[1]Fraunhofer Institut for Reliability and Microintegration, Department Micro Devices and Equipment
[2]Chemnitz University of Technology, Department of Microsystems and Precision Engineering,
Reichenhainer Strasse 88, 09126 Chemnitz

1 Introduction

Modeling and simulation of MEMS is of vital importance to develop innovative products and to reduce time-to-market at lower total costs. Advanced design methodologies and a variety of software tools are utilized by the MEMS-Design group in order to analyze complex geometrical structures, to account for interactions among different physical domains and to capture the cooperative play of micro devices and connected electronic circuitry or signal processing units. Computer simulations provide a deep understanding of the device behavior and lead to systems with optimized performance parameters.
Activities of the MEMS-Design group are focused on software development for device and system simulations, on modeling and simulation of user-specific applications and practical Microsystems design for prototypes manufactured at our clean room facilities.
In particular, we make use of Finite Element Techniques for structural, thermal, electromagnetic and fluid analyses of moving silicon-parts for sensor and actuator applications. Individual effects and cross-talk among different physical domains are either covered by direct coupling algorithms or parameter extraction methods referred as Reduced Order Modeling.
Reduced Order Modeling of MEMS allows a tremendous reduction of model size which becomes important for time-domain simulations with several hundreds of steps needed for circuit and control system virtual prototyping. Since Reduced Order Models are based on analytical terms, they can easily transferred from one simulator to others and can be adjusted to experimental data. Automated generation of parametric Reduced Order Models is considered as the ultimate goal for the future.
Our work is based on a close cooperation of the Fraunhofer Institute for Reliability and Microintegration, Department Micro Devices and Equipment and the Chemnitz University of Technology, Department Microsystems and Precision Engineering. In-house design, manufacturing and test allow all-embracing service delivered to our partners and customers.

2 Microsystems Design

2.1 Design Flow for MEMS

Microsystems design exploits various analytical and numerical methods for virtual prototyping of MEMS. The entire design procedure is illustrated in Fig. 1 and consists of the following steps:

- Low level system simulations,
- Process sequence and mask design,
- Process simulation and optimization,
- Component and device analyses and
- Simulation of the system behavior.

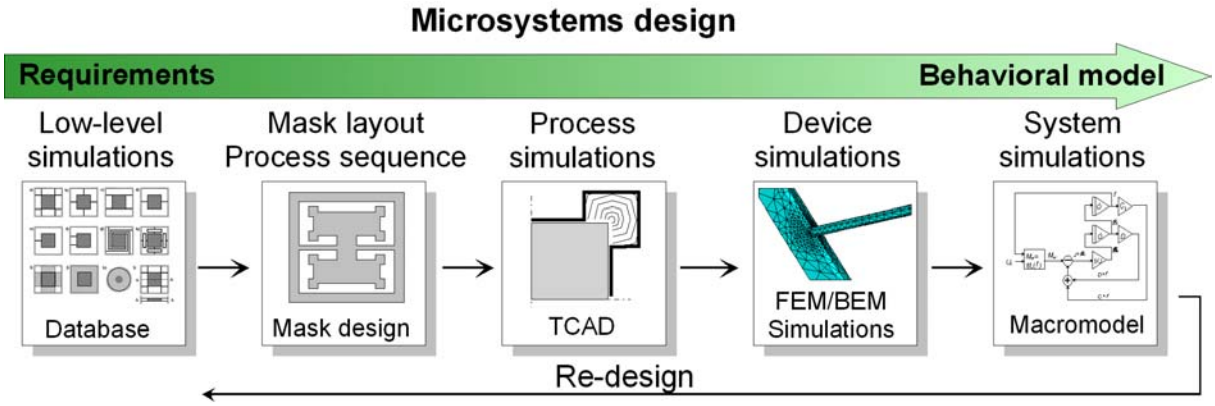


Fig. 1 Microsystems design procedure used for microelectromechanical devices.

2.2 Low level system models

The design process usually starts with low-level system models (block-diagram or lumped parameter models) in order to find a preliminary layout and process sequence. Simplified models are utilized for analyzing the cooperative play of different components and to estimate and optimize the system performance. Results are physical properties such as stiffness data, desired eigenfrequencies or inertial masses, damping ratios and electrostatic coupling terms needed for electrostatic actuation and capacitive detection.

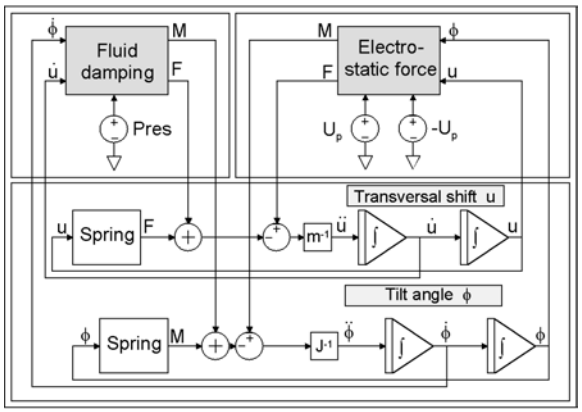


Fig. 2 Low level system model of a Micromirror Cell.

Next step will be to look for shape elements (components) which fulfill the physical properties obtained by low level analyses at reasonable costs and available technology. Databases with frequently used components are helpful to compare different layouts and to optimize geometrical dimensions.

2.2 Process level simulations

Process level simulations are employed to obtain structural solid models from the mask layout and process description. Often, material properties depend on chosen process parameters and must be simulated likewise.

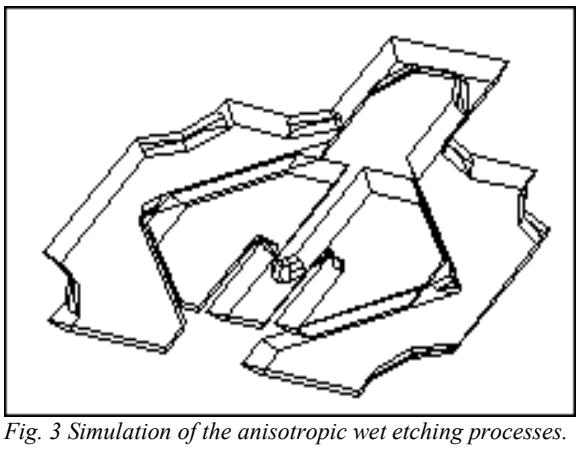


Fig. 3 Simulation of the anisotropic wet etching processes.

2.3 Component and device simulations

The physical behavior of micro components is described by partial differential equations which are typically solved by Finite Element or Boundary Element Methods. Device level simulations are classified in *single domain* and *coupled field* simulations.

Single domain simulations are state of the art and can be realized by a series of commercial software tools. For example, Fig. 4 shows the mechanical response of an accelerometer at external loads in operating direction.

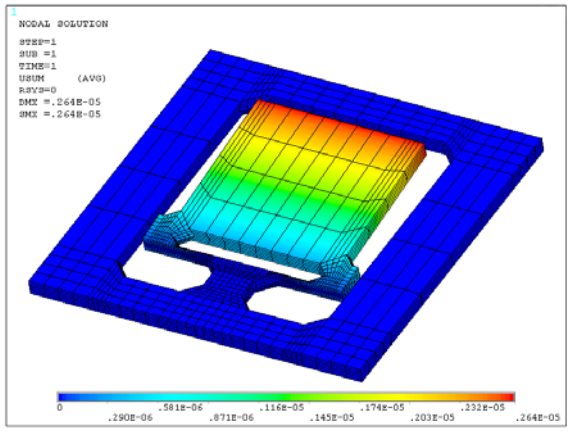


Fig. 4 Displacements at acceleration loads.

Coupled field simulations are vital to capture electrostatic-structural or fluid-structural interactions in sensors and actuators. Usually coupling algorithms must be adapted to special needs in order to account for non-linear effects which are inherent in MEMS devices.

For example, the performance of comb drive actuators is strongly affected by electrostatic fringing fields. This leads to levitation forces which lift the movable component out of the wafer plane. Eventually the forces may cause oscillations which disturb the system functionality.

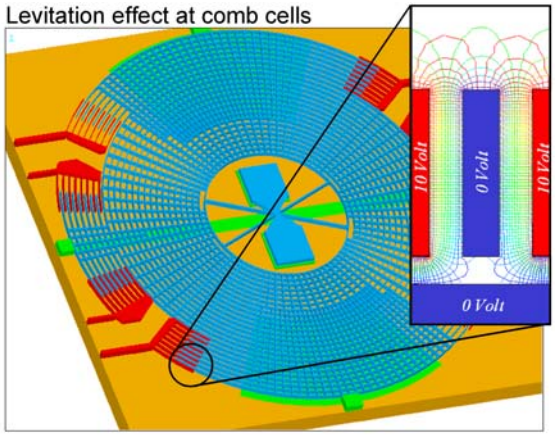


Fig. 5 Electrostatic fields at movable microcomponents.

Fluid-structural simulations are necessary to predict viscose damping of moving microstructures in the surrounding air. Resonant amplitudes and cross-talk of micromirror cells have been analyzed from the dynamic pressure change of air in the small gap between mirror plate and substrate.

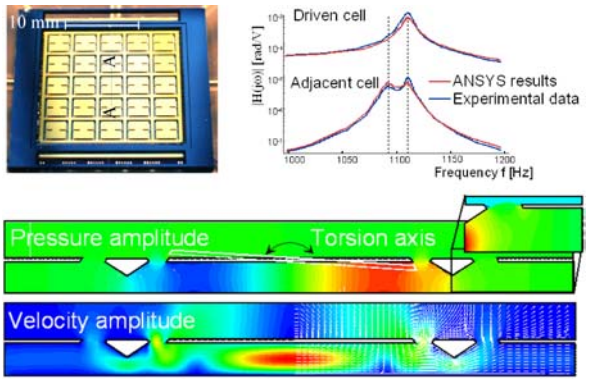


Fig. 6 Fluid-structural interactions in micromirror arrays.

2.4 System simulations of MEMS

Goal of system modeling is to study the cooperative play of microelectromechanical components, the controller unit and the electronic circuitry with the environment. For example, Fig. 7 shows a MATLAB/SIMULINK model which was utilized to predict the image quality of an micro optical laser projection system.

Component models deployed for the mirror cells are directly extracted from finite element models by Reduced Order Modeling techniques. Reduced order black-box models relate essential input signals (e.g. electrode voltage) to output parameter such as tilt angle, plate warp or mirror temperature needed for failure analyses.

Fig. 8 shows the controlled voltage time relationship needed for a saw-tooth like displacement function of image projection systems. In the lower part of Fig. 8, one can observe and evaluate signal distortions of the projected laser light.

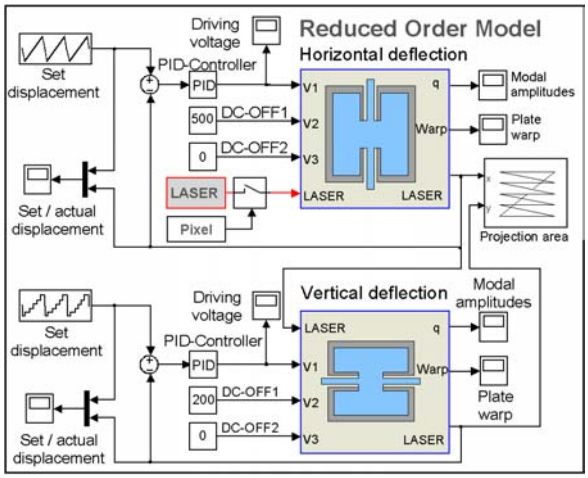


Fig. 7 System model of a micromirror laser display unit.

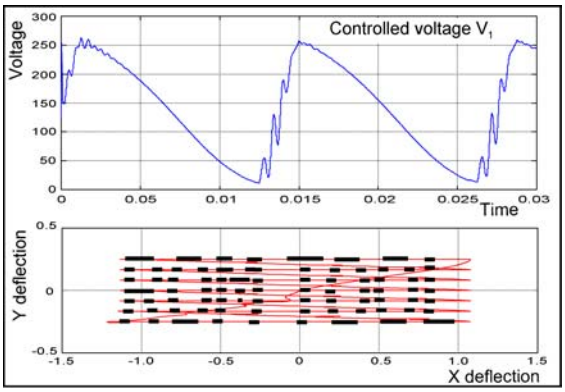


Fig. 8 System simulation results obtained in MATLAB.

3 Development work

Drawback of existing finite element and reduced order modeling techniques is that those algorithms can only analyze a single model configuration with specified dimensions and physical parameters. In practice, designers want to know the influence of parameter variations on the structural response in order to optimize the entire system and to assess the effect of tolerances.

Currently, parametric models of complex devices are extracted by numerical data sampling and subsequent function fit algorithms. Each sample point must be obtained by a separate finite element run whereby the change of geometrical dimensions is realized by mesh morphing or remesh functionality.

Current research work is focused on new "variational" finite element technologies which account for parameter variations in a single finite element run. The key idea of the new approach is to compute not only the governing system matrices of the FE problem but also high order partial derivatives with regard to design parameters by Automatic Differentiation algorithms. Results are Taylor series approximations which characterize the device and system behavior in the vicinity of the initial configuration.

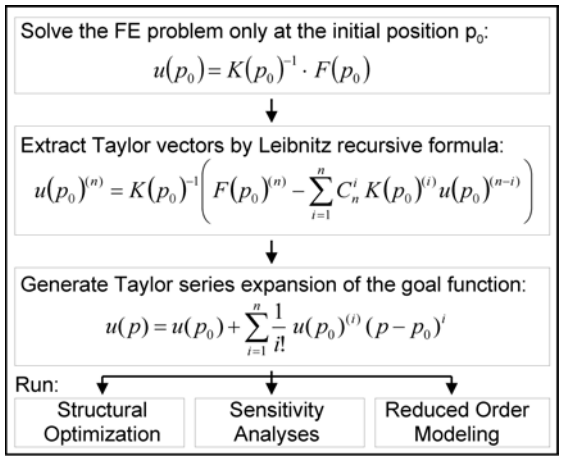


Fig. 9 Parameteric finite element modeling techniques.

Model Building, Control Design and practical Implementation of a high precision and high dynamical Acceleration Sensor

Wolfram, Heiko[a]; Schmiedel, Ralf[b]; Kurth, Steffen[c]; Mehner, Jan[c] ; Hiller, Karla[b,e]; Aurich, Torsten[d]; Günther, Wolfgang[d]; Dötzel, Wolfram[a]; Geßner, Thomas[e,b,c]

[a]Chemnitz University of Technology, Faculty of Electrical Engineering and Information Technology, Department of Microsystems and Devices,

[b]Chemnitz University of Technology, Faculty of Electrical Engineering and Information Technology, Center for Microtechnologies,

[c]Fraunhofer Institute for Reliability and Microintegration,

[d]GEMAC - Gesellschaft für Mikroelektronikanwendungen Chemnitz m.b.H.,

[e]Chemnitz University of Technology, Faculty of Electrical Engineering and Information Technology, Chair of Microtechnology.

Abstract

This project deals with the development of an acceleration sensor system. The starting point is a theoretical model, built from the physical principles of the complete sensor system, consisting of the MEMS (*Micro-Electro-Mechanical Systems*) sensor, the charge amplifier and the PWM (*Pulse-Width Modulation*) driver. The LTI (*Linear Time-Invariant*) system, derived at the operating point, is used to design a robust control with the *Mixed-Sensitivity H-infinity Approach*. The system contains an unstable pole and unstable zeros, resulting from the electrostatic spring softening and time delay, imposed by the A/D-D/A conversation delay and DSP computing time. Thus, limitations for the control design are given. Parameters of the real system, which are needed for the theoretical model description, are either inaccurate, because of tolerances in every sample. Or they are just unknown. Therefore, the theoretical model lacks of completeness or might be inaccurate. A new two-stage identification scheme is deployed to the system to overcome the instability and to obtain the parameters directly from the "real world". The first samples have archived a resolution of better than 500 μg and a closed-loop bandwidth of more than 200 Hz.

1 Introduction

MEMS play an important role in the realization of sensor/actor systems in micro and nano regions. One Advantage for such MEMS is the technology, which directly can be applied from the micro electronics. Another one is the simple and robust layout. Disadvantages for Control are the strong nonlinearity of the electrostatic field component and the nonlinearity of fluid damping. Simulation and practical tests have to show, if the robustness of the control is still sufficient for the highly nonlinear system.
The block description shows Fig. 1, consisting of

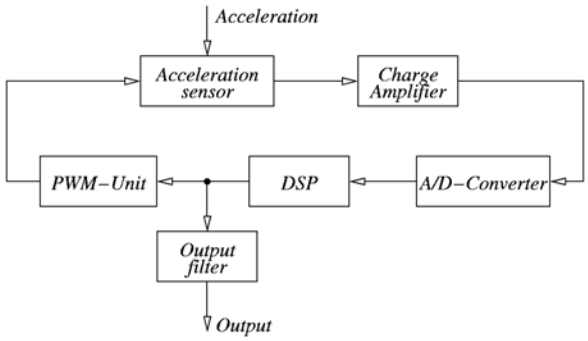


Fig. 1: System Block Diagram

the MEMS sensor, the charge amplifier, A/D conversion system, the PWM driver and DSP system.

2 Design

The sensor configuration shows Fig. 2. The sensor covers consist of glass to reduce the circuit effort in the detection electronics. The applied SiO_2-Bumpers at the edges of the seismic mass prevent the electrical contact with the outer electrodes.

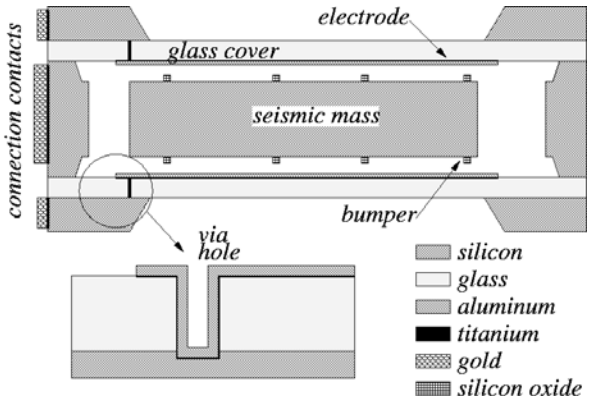


Fig. 2: Schematic configuration of the sensor chip

3 Model Building

The electrical actuated acceleration sensor can be generally described as a rotational mechanical spring-mass system

$$\left[-\omega^2 J + \mathrm{j}\omega\left(D + D_s(\omega)\right) + K + K_s\right]\varphi(\omega) = M_{ext}(\omega) + M_{el}\left(\varphi(\omega), u(\omega)\right) \quad (1)$$

with the moment of inertia J, the damping D and spring constant K, consisting of constant mechanical and frequency dependent squeeze-film parts, an acting mechanical moment M_{ext} from the outside, the electrostatic moment M_{el} and the rotation angle φ.
Just only the first torsional mode with the resonance frequency

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{K}{J}} \quad (2)$$

is controllable and detectable and is considered in the model. Since the resonance frequency can be measured easily, it is used to estimate the spring constant K, which directly specifies the DC-gain of the mechanical system.
The squeeze-film parts can be described with the *Reynolds Lubrication Equation*, a special simplification of the general *Navier-Stokes Equations* in the case of a small gap between two parallel moving plates, laminar flow and isothermal compression. Supposing that the motion of the plates and pressure variation are small, the equation can be further linearized and analytically solved, which was done in [1]. A mapping with the force-current analogy of the squeeze-film damping is described in [2]. The analytical description of the squeeze-film component was extended to a rotational motion for a variating rotation axis in [3] to describe the motion of the seismic mass.
The electromechanical moment is mainly responsible for the strong nonlinear behavior of the system. It results in the electrostatic spring softening effect at high voltage and also in a change in the open loop gain of the system. The electromechanical moment can be linearized and divided into two gain parts - The inner feedback part k_{el}, which is responsible for the spring softening and in the gain part k_u in the open loop.
The detection unit, the charge amplifier, amplifies the sensor difference capacity into a proportional voltage.
The applied sensor driver, the PWM unit, firstly governs the position of the seismic mass with changing the duty-cycle of the rectangular wave. It also realizes the charge flow for the capacity detection.
The whole LTI system model, needed for the control design, can be evaluated to

$$G_{emech} = \frac{k_u k_{pwm} k_{amp} G_{mech}}{1 - k_{el} G_{mech}} \quad . \quad (3)$$

4 Control design

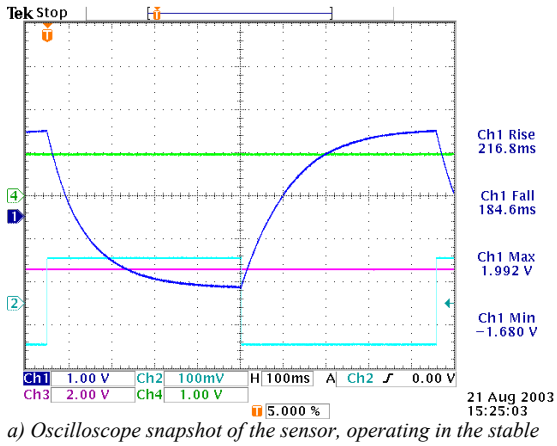
The S/KS/GS/T-Standard-Design Problem (*Mixed-Sensitivity-Approach*) is used for the control design. In this design, the transfer function matrix $\boldsymbol{N}$ will be minimized with the H_∞ Norm

$$\min_{\boldsymbol{K}} \left\| \boldsymbol{N}(\boldsymbol{K}) \right\|_\infty \quad (4)$$

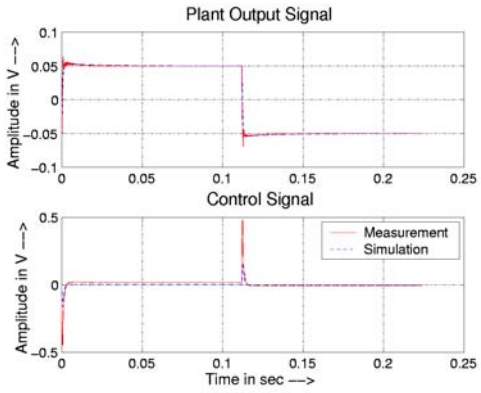
over all stable and proper controllers $\boldsymbol{K}$. In our case, the main objective is the minimization of the sensitivity transfer function $\boldsymbol{S}$, which optimizes the disturbance rejection. A constant bound is put on the control signal to further avoid actuator saturation.

5 Identification

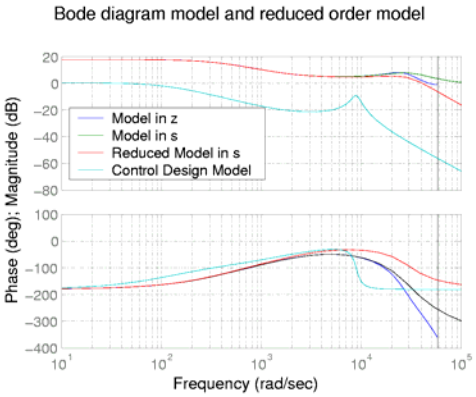
The sensor system is highly unstable under nominal operating voltage. Thus, a direct system identification is not possible in an open loop fashion way. Another way has to be found to get the system parameters from the “real world”.
In our case, the system will be identified in two stages. In the first stage a minimal sensor operating voltage $u_{b\,min}$ will be applied to the sensor. An electrostatic sensor excitation is now possible in the stable region. And the influence of the



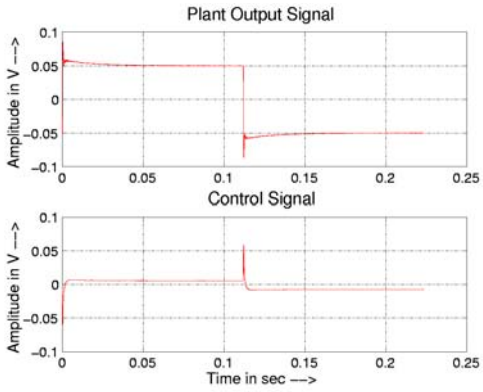
a) Oscilloscope snapshot of the sensor, operating in the stable region



b) Output and control signal of the simulation compared to the real system in- and output at operating voltage u_b = 10 V



c) Bode diagrams of the model of the second identification and the extended model of the first identification



d) Output and control signal after one iteration at operating voltage u_b = 20 V

Fig. 3: Results of one sample

electrostatic field is very low. In that case, the resulting normalized system can be equalized with the mechanical system. The control parameters will be synthesized from the extended model (3), where the field components under nominal sensor operating voltage u_b will be applied. In the second stage, another identification is made in closed-loop operation under nominal sensor operating voltage. This identification can be also seen as a system fine-tuning.

6 Results

The identification and control design routine have been successfully applied to several samples. The Results of one sample are shown in Fig. 3.

It was shown, that it is possible to control the highly nonlinear system with a robust LTI controller. The simulation of the system, shown in Fig. 4, also gives good results, which are comparable to practical tests. The controller was fond with a new introduced tow-stage identification scheme.

7 Future work

Further questions need to be answered:

- The seismic mass collision with the outer electrodes needs to be tested in simulation and practice,
- The system behavior during start up and in non-detectable regions,
- The influence of quantization effects and quantizer overflow
- System optimization, especially for resolution improvement.

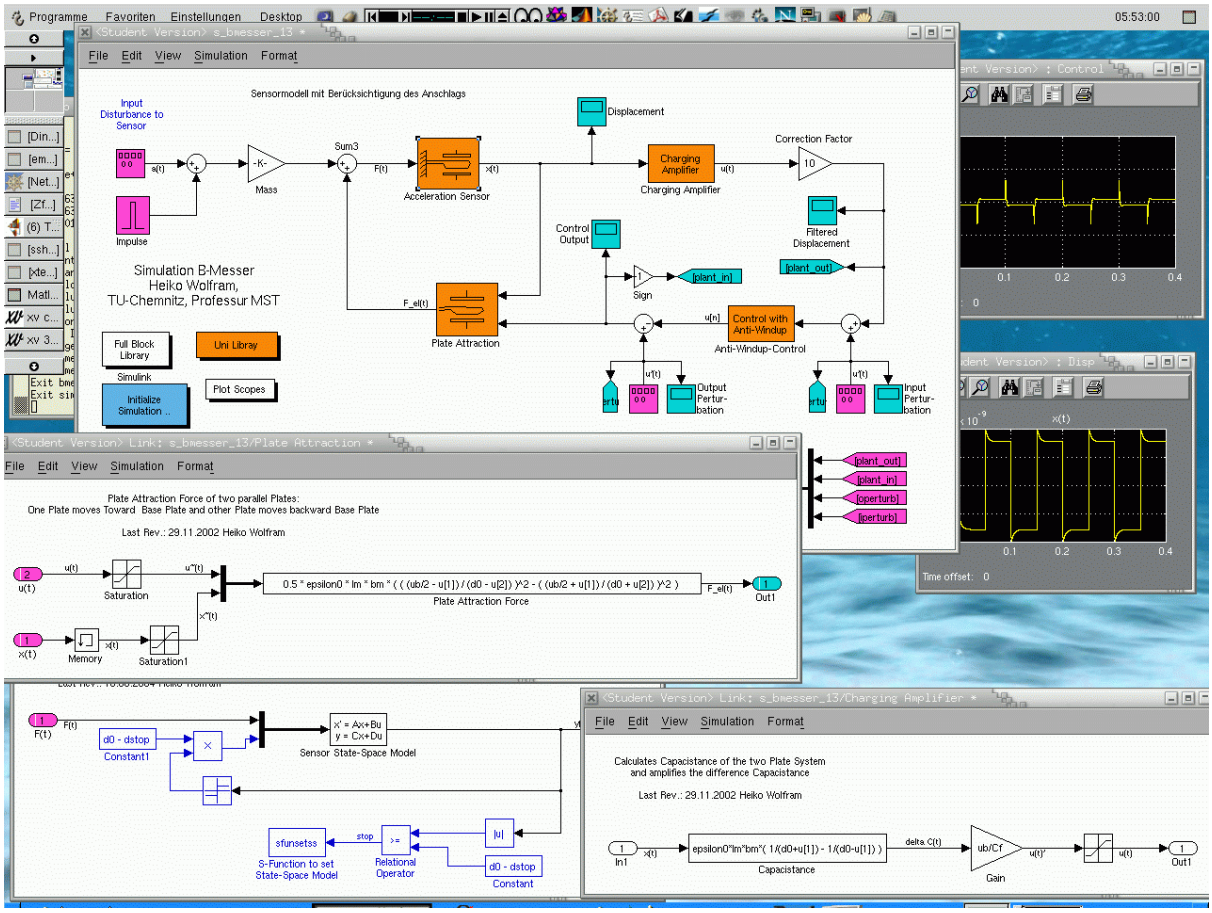


Fig. 4: Screen snapshot of the Simulink™ model

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MEMS Scanner for Laser Projection

Steffen Kurth[a], Christian Kaufmann[b], Ramon Hahn[b], Jan Mehner[a], Wolfram Dötzel[b], Thomas Gessner [a,b]
[a] Fraunhofer Institute for Reliability and Microintegration, Dep. MDE
[b] Chemnitz Univ. of Technology, Center for Microtechnologies

1. Introduction

High resolution laser projection demands antagonistic properties of the scanner, as large mirror size, high deflection angle and high scanning frequency[1]. The mirror curvature caused by bending due to mechanical stress of reflection layers and caused by dynamic deformation due to inertia and non perfect stiffness of the mirror can influence the far field spot of the laser beam[2] and should be lower than 1/10 of the smallest used wavelength. A design with a higher mirror thickness, proposed e.g. in Refs. [3,4] is the most common way to overcome this problem but it leads to higher inertia, stiffer torsion beams and to higher driving force in consequence.

In the following, a micromachined resonant scanner usable for horizontal deflection of the laser beam in a projection display is described and its analysis is reported. The approach followed here is based on a two degrees of freedom resonator. The magnitude amplification occurs at the resonant frequency of the second resonant mode. The relatively low deflection of driving plate in comparison to the mirror makes a very small electrode gap size possible. It leads to a high electrostatic force and low influence on the Q-factor of the used resonant mode caused by the air flow in the electrode gap.

2. Design

The device (Fig. 1) consists of a circularly shaped silicon plate which is suspended by torsion beams in the center of an elastically suspended driving plate. The moving part of the scanner basically consists of two mechanically coupled resonators. The inner resonator acts as scanning mirror. The outer resonator is used to drive this mechanical system. A resonator with two rotational degrees of freedom is arranged in this way. The rotation axes of mirror and driving plate are the same. A supporting part made of glass carries two electrodes in the region of the driving plate. A voltage between the electrodes and the driving plate produces electrostatic torque primarily onto the driving plate.

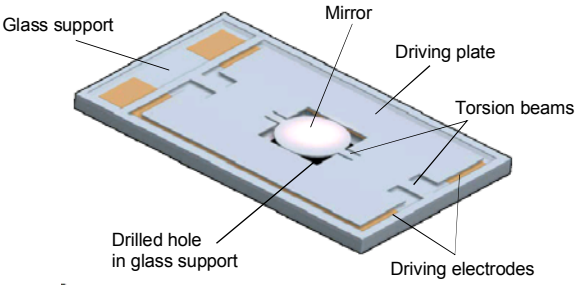

Fig. 1: Outline of the scanner

3. Modeling and simulation

3.1 General aspects

Neglecting motion in other direction than rotation concerning the axis of torsion beams, the mechanical system can be generally mathematically described by the corresponding differential equation of motion. The two angular eigenfrequencies are given by the square roots of the eigenvalues:

$$2\pi f_{0i} = \sqrt{Eigenvalue\ \left(\mathbf{J}^{-1}\,\mathbf{K}\right)} \qquad (1)$$

whereby **K** denotes the stiffness matrix and **J** denotes the matrix of inertia. The ratio of the amplitudes of each resonant mode is given by the eigenvector of the corresponding eigenvalue. After substitution of the stiffness and mass moments of inertia by ratios of both mass moments of inertia $A = J_1/J_2$ and of both rotational rigidities $B = k_1/k_2$ respectively, the ratio of both elements of the eigenvector corresponding to the 2nd eigenfrequency can be expressed by

$$\frac{\alpha_{01}}{\alpha_{02}} = \frac{2B}{A - B + AB + \sqrt{-4AB + (A + B + AB)^2}}. \qquad (2)$$

It reflects the ratio of angular deflections of mirror and driving plate illustrated in Fig. 2.
One can see that the deflection of mirror is much higher than the deflection of driving plate. In consequence, the deflection of the mirror is amplified in respect to the deflection of the driving plate 25…200 times within the boundaries of the diagram. The negative sign of the ratio indicates a paraphase motion of mirror and driving plate at the 2nd eigenfrequency. One can see that *A* strongly influences the amplification whereas the amplification is less sensitive regarding *B*.

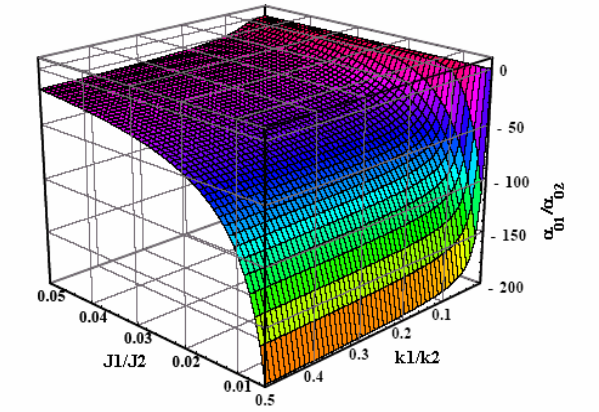

Fig. 2: 3D plot of the dependency of deflection amplification on the ratio of mass moments of inertia and of stiffness

The diameter of the mirror plate with D = 2.2 mm, the maximum mechanical angular deflection of $\alpha_{01} \geq 5°$ and the scanning frequency $f_{scan} = 48\,kHz$ are the main constrains for design. A suitable design of the properties of the two degrees of freedom resonator leads to a significant amplification of the oscillation of the mirror in respect to the oscillation of the driving plate. The first resonant mode is a rotation of both plates with nearly the same magnitude at a frequency of 5.5 kHz. The second mode with paraphase deflection at 24 kHz shows the amplitude amplification. We decided for 280 µm thickness of the mirror and driving plate in order to achieve sufficiently low dynamic mirror curvature. Thus the values of mass moments of inertia are determined by geometry and specific weight.

3.2 Damping

Damping moments acting on the mirror and on the driving plate originate from the energy dissipation within the surrounding air. For analysis of damping we consider two different parts of this space. The first one with main energy dissipation is the space in between the driving plate and the electrodes which is characterized by a viscose air flow. The other part comes from the flow above the driving plate and around the mirror plate. We analyzed the second part experimentally and included the damping in the model. The calculation of damping and the experimental procedure to determine the part caused by air flow above the mirror is explained within Ref. 5 in detail.

3.3 Analysis in frequency domain

An analysis of the mechanical system in frequency domain gives the magnitude and phase of the angular deflection of the mirror and of the driving plate as to be seen within Fig. 3. A voltage of 400 V_{pp} superimposed by 200 V_{dc} has been assumed for driving. One can clearly see both resonant peaks. Mirror plate and driving plate oscillate with nearly equal deflection magnitude and same phase at the first resonant frequency (5.5 kHz). The second resonant peak indicates a substantially higher Q-factor compared to the 1st one and a magnitude amplification of 53 at this frequency. It equals the ratio of the eigenvalues of characteristic equation without damping. The theoretic analysis gives a motion in paraphase of mirror and driving plate and a phase shift 1.5 π regarding the driving torque. The maximum mechanical deflection is calculated to be ± 5.7 deg.

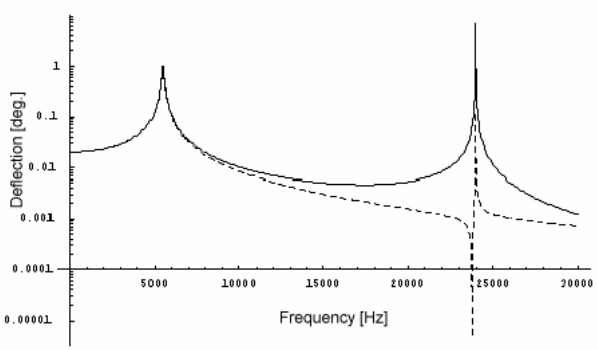

Fig. 3: Calculated magnitude of angular deflection of mirror and of driving plate

4. Results

4.4 Flatness of mirror surface

The aluminum reflection layer and the combination of silicon and glass with different thermal expansion coefficients are two main reasons for mirror and chip deformation induced by mechanical stress. The topography of mirror,

driving plate and torsion beams has been measured using a customized phase shift interferometer. The circular mirror surface is very smooth and flat. Its deviation from plane is less than ±15nm and lower than λ/10 in respect to the wavelength of visible lasers. (Fig. 4).

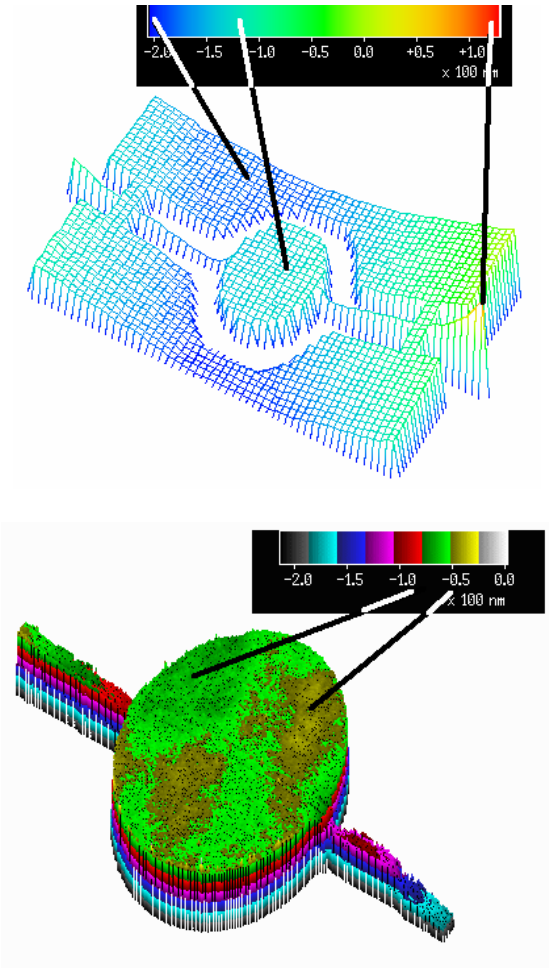

Fig. 4. Surface profiles of driving plate and mirror (upper image) and of the mirror (lower image) measured by a phase shift interferometer

4.5 Scan angle and frequency behavior

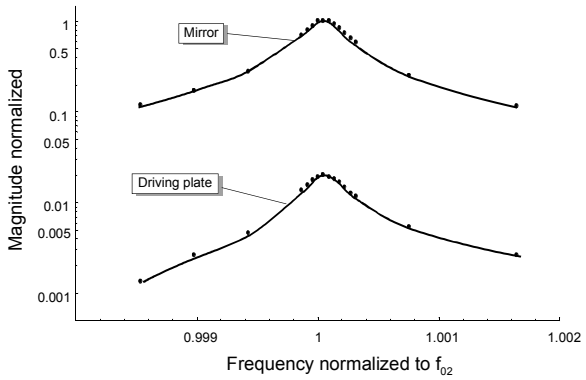

Fig. 5. Measurement result of deflection angle in dependency of frequency of the driving voltage

Applying a voltage of $380V_{pp} + 190V_{dc}$ with the frequency corresponding to the frequency of second resonant mode results in a mechanical deflection of ± 5.5 degrees (22 deg measured scan angle). The mechanical Q-factor is 5100 operating the scanner at atmosphere. It is expected that the high Q-factor leads to low jitter of scan angle. The mechanical bandwidth is approximately 5 Hz (see Fig. 5).

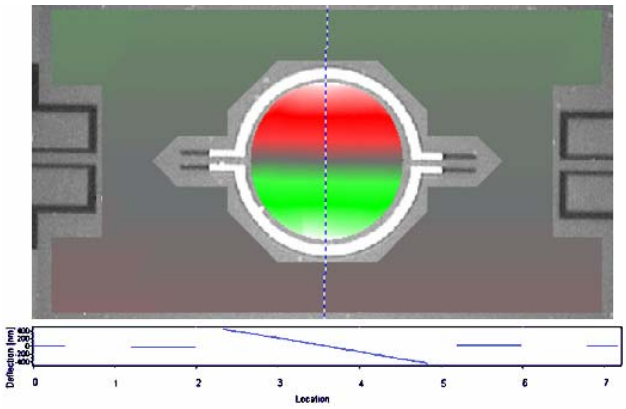

Fig. 6. result of measurement of dynamic behavior by Laser Scanning Vibrometer.

Fig. 6 shows a result of deflection measurement by a Laser Doppler Scanning Interferometer. It clearly shows the paraphase motion of mirror and driving plate and the amplification of the mechanical deflection. The theoretically predicted amplification of the deflection by a ratio of 53, the Q-factor, the resonant frequencies and the maximum mechanical deflection angle agree very well with the measured values.

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Tunable Fabry-Perot Filter for Infrared Radiation

Karla Hiller[1], Steffen Kurth [2], Norbert Neumann[3]
[1] Chemnitz Univ. of Technology, Center for Microtechnologies
[2] Fraunhofer Institute for Reliability and Microintegration
[3] InfraTec GmbH, Dresden

1. Introduction

This contribution deals with the design, fabrication and test results of a micromachined first order Fabry-Perot (FP) filter that is intended for use as a tunable filter in advanced infrared gas analysis. Flexibility and performance of such a device are more sophisticated than a simple fixed filter approach particularly if gas mixtures have to be analyzed in which the gases are characterized by adjacent or overlapping absorption bands. The new approach is based on a Fabry-Perot interferometer with an air cavity, which is electrostatically tuned (Fig. 1). In the intended infrared gas analysis application the FP filters require extremely flat, coplanar and smooth reflectors with a high reflectance to achieve a narrow bandwidth of about 50nm, a high tuning range of at least 1800 nm and a high peak transmittance of about 70%.

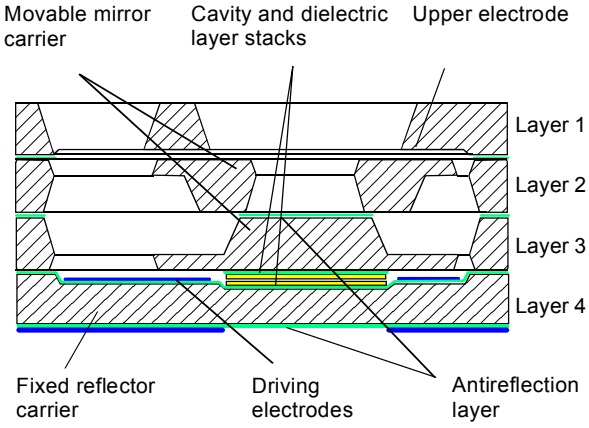

Fig. 1. Cross sectional drawing of the FP filter

2. Design and fabrication

The FP filter is fabricated by bulk micromechanics technology to achieve optimal interference conditions. Relatively thick (300 µm) silicon wafers are used as the carriers for both the fixed and the movable reflector. The reflector (2.2 x 2.2) mm² is located in the center of the driving electrodes, the suspension with diagonal beams, and the rim of the filter. Diagonal bending beams located in the corners of the rim elastically suspend the moveable reflector and are arranged to form a parallel spring suspension. This provides the necessary vertical movement and the necessary rigidity to minimize any tilting of the movable mirror carrier.

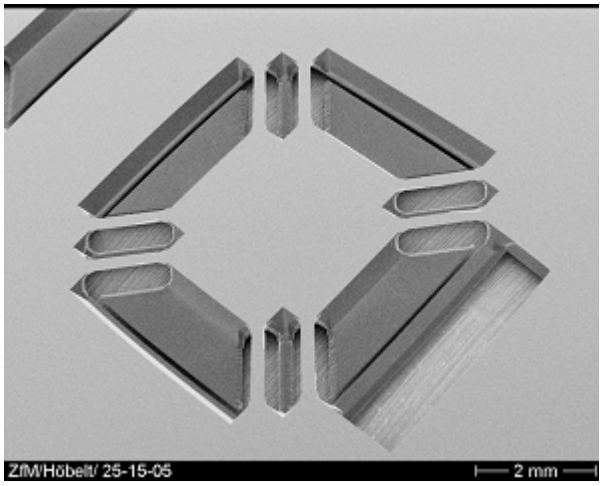

Fig. 2 SEM image of the movable mirror carrier with the parallel spring suspension

In a first approach the springs have been formed in layers 2 and 3, and the parallel spring suspension was created by bonding these layers together (see Fig. 1). The new approach can realize the parallel springs within one wafer by using asymmetric masks (one on each side) and a simultaneous, symmetric wet etch process. 12 diagonal bending beams with a trapezium cross section are formed (Fig. 2). With this method the number of layers can be reduced, which leads to a simplified technology and an increased process yield.

3. Optical design

Distributed Bragg Reflectors consisting of deposited alternating quarter-wave layers of low refractive index silicon dioxide and high refractive index polycrystalline silicon are used as reflectors. Because of the relatively high ratio of refractive indexes n_H/n_L of 2.4 a wide high-

reflective zone from (3…5) µm and a high maximum transmission of 94% were obtained already with a $(HL)^2$ layer stack (Fig. 3 and Fig. 4). High effort was necessary to minimize curvature and roughness of the reflector and to improve the antireflection coating of the reflector carrier. The roughness of the layer stack has been reduced to 1.7 nm applying low-temperature deposited polycrystalline silicon as high refractive index material.

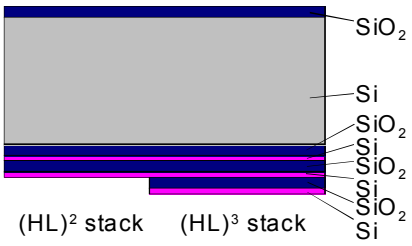

Fig. 3. Configuration of the $(HL)^2$ and of the $(HL)^3$ reflection layer stack

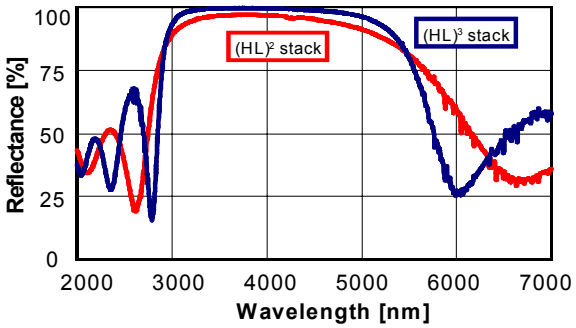

Fig. 4. Spectral reflectance of the reflection layer stacks (measured data)

4. Test results

Fig. 4 shows the reflectance measured on $(HL)^2$ and $(HL)^3$ reflection layer stacks. The optical and electromechanical concept has been proven on etalons with a fixed resin (SU8) spacer and on tunable FP filters. The results (presented in Fig. 5) confirm the suitability of smooth layer stacks to achieve a transmittance of about 75% and a spectral bandwidth of 50 nm. A broadband multilayer antireflection coating (ARC) improves the transmittance in the entire spectral range of (3…5) µm and reduces the ripple caused by internal reflections in the silicon substrate. It is obvious that a single quarter-wave ARC consisting of silicon dioxide or silicon nitride shows reduced performance in comparison to the multilayer ARC.

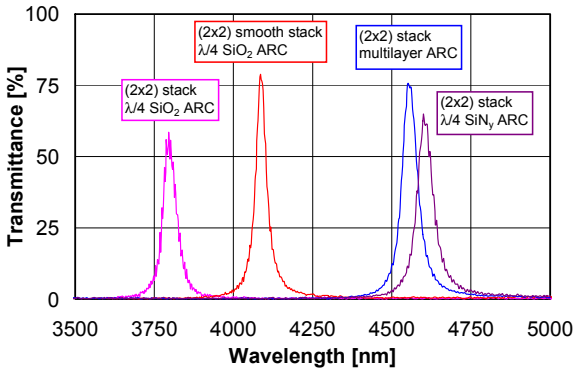

Fig. 5. Transmission characteristic of FP filters with various fixed cavity size

The tunable FP filters were designed with an optical reference wavelength of 3600 nm. Two different types have been completed. A first one provides a variation of the cavity spacing between 1300 nm and 1850 nm for a tunable wavelength of (4…3) µm. A second one performs a variation of the cavity spacing between 1300 nm and 2550 nm in order to cover a spectral range of (5...3) µm. The spectral bandwidth of the short-cavity filter is about 60 nm and the peak transmittance about (60…50)%. Applying a voltage of 24V a high tuning range from 3900 nm up to 3000 nm is achieved (see Fig. 6). The spectral bandwidth of the long-cavity filter at the long-wavelength end is broadened and the blocking is less compared to shorter wavelengths. It is assumed that the lower reflectance of the reflector at about 5µm (see Fig. 4) is the reason for this phenomenon. A narrow pass band of 50 nm bandwidth has been observed in the range of shorter wavelength.

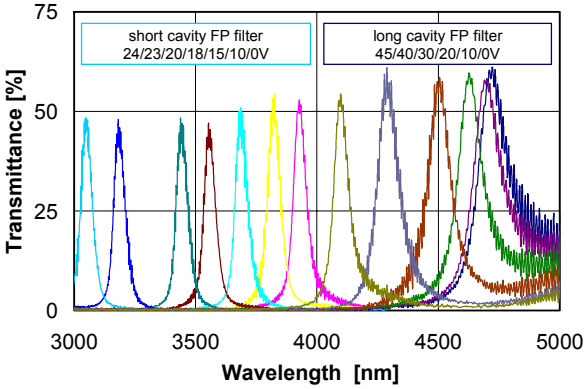

Fig. 6. Transmission characteristic of tunable short cavity and long cavity FP filters with different tuning voltage

Micro Mirror Spectrometer

Saupe, Ray[1] ; Otto, Thomas[2] ; Gessner, Thomas[1,2]
[1]Chemnitz University of Technology, Center for Microtechnologies,
[2] FhG-IZM Chemnitz, Abteilung MD & E

1 Introduction

Infrared analysis is a well-established tool for measuring composition and purity of materials in industrial-, medical- and environmental applications. Traditional spectrometers , generally designed for laboratory use are too large and delicate or too costly for a lot of applications. In order to realize more compact and in particular cost-effective spectrometers MOEMS technology offers attractive possibilities. Therefore a micro mirror spectrometer has been developed. A scanning micro mirror is the essential element of this miniaturized basic monochromator set-up. Thereby polychromatic radiation is periodically dispersed into its spectral components and by an infrared detector. By means of rapid prototyping methods the micro mirror spectrometer is manufactured for the spectral range from 2 to 5 µm.

2 Functional Principle

The optical design of the spectrometer module is realized in a simple optical set-up according to a Littrow alignment. A scanning micro mechanical torsion mirror optimized for that application is the central component. The mechanical properties of this micro component strongly influence the device performance parameters like resolution and accuracy. The large mirror surface together with a large tilt angle effects a high throughput and broad working range compared to other MEMS devices [1].
The functional principle is shown in Figure 1. After passing the sample transmitted light, generated by an infrared source, enters the spectrometer through a narrow entrance slit. A spherical mirror collimates the incident radiation towards the micro mechanical torsion mirror. There the radiation is reflected to a diffraction grating, which disperses the radiation into its spectral components and different orders of diffraction. According to the wavelength depended reflection angle the desired part of diffracted light reaches the exit slit via both micro mirror and collimator. Behind the exit slit a Mercury Cadmium Zinc Telluride (HgCdZnTe) detector and transimpedance amplifiers are arranged, which convert the monochromatic radiation acquired by the detector into electrical signals for processing.

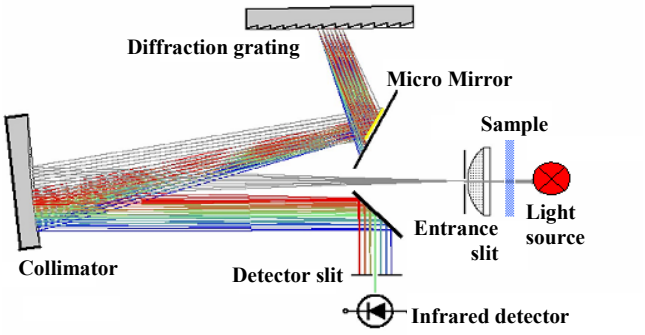

Fig. 1 : Optical diagram of the spectrometer

The wavelength selection depends on the tilt of the torsion mirror, which is driven by an alternating high voltage signal at its resonance frequency of about 270 Hz. During one half period of the mirror one complete spectrum is scanned – thus one basic measurement takes about 2 milliseconds. A position sensor observes the current mirror angle permanently. All preamplified signals from position and radiation sensors are sampled by analog to digital converters simultaneously. Subsequent digital signal processing ensures the elimination of MEMS tilt deviations. All data are preprocessed by embedded computing modules. These modules implement the control of the MEMS device, the analogue to digital conversion, the averaging of raw spectra and the data transfer to a personal computer, which calculates the transmission spectrum of the measured sample.

3. Packaging

The micro mirror spectrometer is manufactured by using rapid prototyping methods. Thereby the construction data are converted into volume data and transferred to a selective laser sintering

machine, which builds up the prototype layer by layer from polyamide powder. No specific tools, moulds or any other mechanical processes are required. Post processing except thread cutting is unnecessary, too. This method allows a fast development and flexible design. Almost all electrical, optical and mechanical components can be integrated directly (Figure 2).

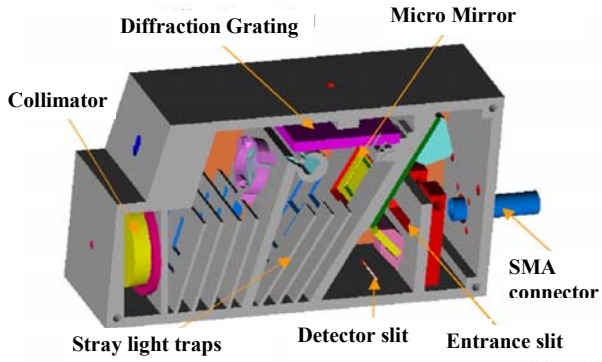

Fig. 2: Monolithic spectrometer set-up

4. Experimental Results

Beside spectral range and spectral resolution, important criteria for the selection of a spectral sensing device are the signal to noise ratio (SNR), signal stability, linearity and wavelength accuracy. The device has been evaluated with respect to these requirements. Both broadband and monochromatic radiation sources were used for characterization. Measurements were performed using conventional monochromators, interference filters and reference samples.

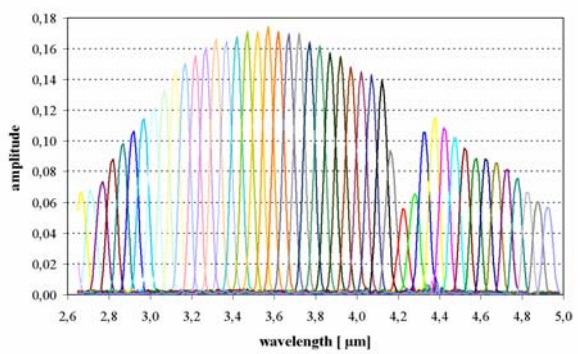

Fig. 3: Wavelength chart by measuring monochromatic light provided by a conventional monochromator

The spectrometer spectral range is determined by the diffraction grating properties as well as the maximum tilt angle of the micro mirror. Sensitivity within this range is determined by the spectral efficiencies of all components including radiation source and detectors. The spectral resolution was determined to be about 32 nm at full width at half maximum (FWHM) for slit widths of 230 µm. Figure 3 illustrates a wavelength chart obtained by measuring monochromatic light provided by a conventional monochromator at several wavelengths. The certain wavelength dependent shapes of peak amplitudes to be observed result from both monochromator output power and spectrometer efficiency. Furthermore it shows no wavelength deviation of the spectrometer signal from the monochromatic input. Basic measurements at spectral resolution of 40 nm yielded a SNR of approx. 35 to 1. It can be improved substantially by averaging to about the square root of the original values. Measuring the wavelength accuracy of a spectral line, a shift less than 1 nm per measurement time was recorded during 5 hours. Furthermore no significant amplitude deviations were obtained.

5. Summary

Micro mirror technology, developed, qualified and first deployed for the communication and laser technology, is also well suited for the realization of miniaturized and truly low priced spectrometers. The functional principle of such spectrometer modules was presented. Further versions of the system for different wavelength ranges, resolutions and instrument performances are in development.
Due to the flexible set-up and its cost-effective realization as well as the fast measuring time, the micro mirror spectrometer offers promising advantages compared to conventional spectrometers with respect to many more application possibilities. Small size and roughness of the device especially allow their application in harsh environments, for instance in process control [2].

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Laser Trimming of Silicon Micro Mirror Devices by Ultra Short Pulse Lasers

B. Keiper[1], M. Weber[1], J. Hänel[1], T. Petsch[1], J. Mehner[2], C. Kaufmann[3]
[1]3D-Micromac AG, Max-Planck-Straße 22b, Chemnitz
[2]Fraunhofer Institut for Reliability and Microintegration, Department Micro Devices and Equipment
[3]Chemnitz University of Technology, Center for Microtechnologies

1 Introduction

Laser-trimming of microstructures is a promising approach to overcome manufacturing tolerances and to tune sensors and actuators for certain operating conditions. A joint research project between 3D-Macromac AG and the Chemnitz Center for Microtechnologies investigates new technologies for wafer level stiffness and frequency tuning of silicon microstructures by ultra short laser pulse tuning. Goal of the development work is to establish a novel technology which allows for in-line measurement of mechanical properties and laser treatment in order to calibrate performance parameter of MEMS. Particular features of laser trimming will be demonstrated on Micro Mirror Devices (MMDs) which are widely used for image projection applications Fig. 1.

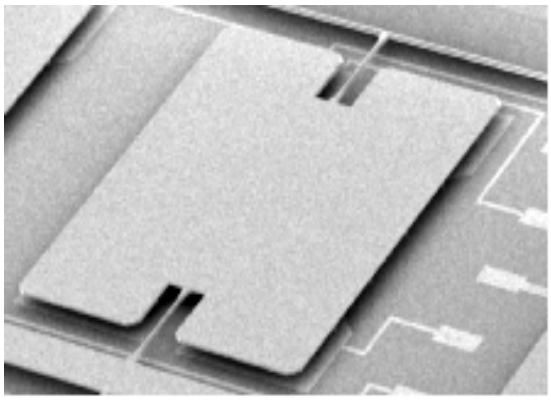

Fig. 1 SEM photography of a Micro Mirror Device.

Advanced optical projection systems (e.g. head-up displays for cars) require micro mirror cells where the resonance frequency lies in a narrow spectral range of about 1% what can hardly be realized in manufacturing facilities. The new idea is to tune the stiffness or inertial mass of micro devices by laser thinning or laser cutting processes. Fig. 2 shows our general approach schematically. Challenging issues for the project are how to prevent contamination by emitted particles and how to reduce surface damage or warp due to laser treatment.

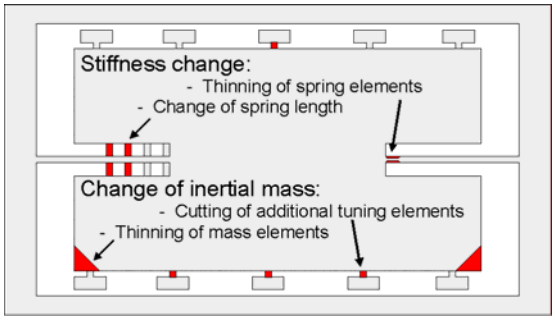

Fig. 2 Possible options for resonant frequency tuning.

2 Laser Trimming Techniques

Tuning of MEMS can be accomplished with extremely high precision by laser ablation. However, when utilizing a conventional long-pulse laser, processing is accompanied by the deposition of heat in the material. Due to the excitation of phonons in superficial regions of the sample, melting occurs and molten material evaporates from the sample. This process is associated with the formation of a heat-affected zone possessing much elevated temperatures. The spatial extent of such zones depends on material parameters including thermal conductivity and laser parameters such as wavelength and pulse duration.

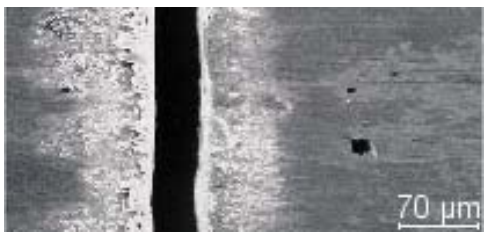

Fig. 3 Extended heat-affected zones on both sides of a ns-laser cut trench.

Fig. 4 Virtually absent heat-affected zones adjacent to fs-laser cut trench.

By contrast, ultra-short laser pulses interact thermally with solid matter by the generation of a highly excited electron-hole plasma. Since the extraordinarily high energy contained in the ultra-short laser pulses (several gigawatts per pulse) is directly coupled into the electronic structure and no phonons become excited, a heat-affected zone is almost completely absent and no melting or splashing of droplets is observed. The ablation energy is almost completely carried with the plasma expanding away from the sample (Fig. 4). For this rationale, trimming of MMDs with ultra-short laser pulses is to be preferred over the usage of long-pulse laser radiation.

Fig. 5 Femtosecond Workstation

Yet another problem consists in the generation of debris, since the wafer containing the MMDs has to become further processed and e.g. upon bonding, superficial particles or an increased roughness are highly problematic. When processed under ambient pressure, ablated material has a mean free path of less than a few hundreds of micrometers. Two approaches have been validated


Fig. 6 Picosecond Workstation PS-1064

capable of resolving this issue: processing under a rapidly flowing gas (a crossjet nozzle was placed close to ablation spot) and micromachining inside a vacuum chamber. While in the former setup, particles continued to condense on the sample (the spatial distribution, however, was no longer symmetric around the ablation location), processing in vacuum proved to give much better results.

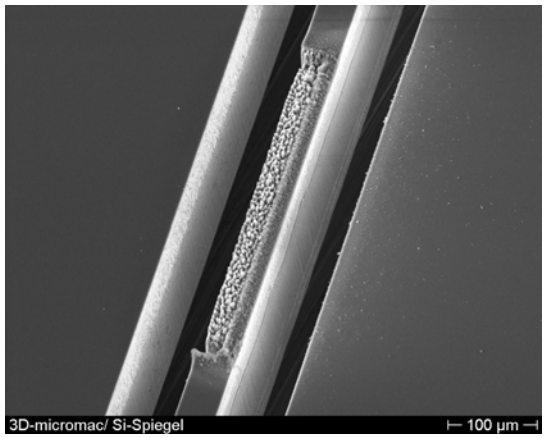

Fig. 7 Processed spring bar of a MMD.

A thinned spring bar is depicted in Fig. 7 and 8. The examples shown have been micromachined with a femtosecond-laser workstation developed by 3D-Micromac AG. At a wavelength of 775 nm and a pulse width of ~ 150 fs, processing was performed using a 50 mm objective resulting in a minimum focus diameter of 7.5 µm. Thinning has accomplished by scanning the beam sixty times at a parallel offset of 1 µm.
The Center for Microtechnologies (ZfM) and 3D-Micromac AG have successfully developed and tested strategies for laser trimming of microstructures. Aim of the collaboration is to investigate achievable accuracy and efficiency as well as developing new laser systems and equipment for in-line laser treatment of MEMS.

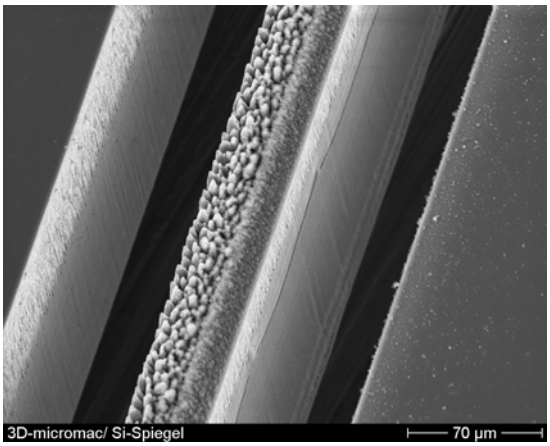

Fig. 8 Femtosecond-laser machined spring bar of a MMD (enlarged section of Fig. 4).

Optical Characterisation Methods for MEMS Manufacturing (OCMMM); Part A: On-chip Integrated Techniques in Combination with Micromirrors

Andreas Bertz[1]; Rolf Hoffmann[1]; Danny Reuter[1]; Thomas Gessner[1,2]
[1]TU Chemnitz, Fakultät für Elektrotechnik und Informationstechnik, Zentrum für Mikrotechnologien
[2] FhG-IZM Chemnitz, Abteilung MD & E

in collaboration with:

Christophe Gorecki[3]; Lukasz Nieradko[3]; Mihail Józwik[3]; Paul V. Lambeck[4]; Geert Altena[4]; Meindert Dijkstra[4]; Hugo J.W.M. Hoekstra[4];
[3]Département LOPMD, Institute FEMTO-ST, Besançon, France
[4]MESA[+], University of Twente, Enschede, The Netherlands

1 Introduction

The European GROWTH project (Ref. G1RD-CT-2000-00261) "Optical Characterisation Methods for MEMS Manufacturing" (OCMMM) will be finished in 2004. Starting in 2001 the proposed project aimed at strengthening MEMS testability at all stages, from the design to the end of life of a microsystem. Electrical characterisation of these devices is a well-proven technique. However, the micromechanical characterisation plays a crucial role as well, both during design and development of microstructures and during chip-production, assembling and life cycles of the finished products. Two optical approaches were pursued to improve the MEMS testability: on-chip integrated techniques as well as external full-field interferometry. The ZfM activities were mainly focussed on the first one, the on-chip integrated optical demonstrators providing local in-situ measurements using Integrated Optics (IO). The micromechanical parameters of actuated MEMS structures are monitored by use of an optical read out, based on a Mach-Zehnder Interferometry (MZI). In loaded demonstrators, an MZI is monolithically integrated into the micromechanical part, while unloaded demonstrators use evanescent field MZI read-out. The first demonstrator was a movable micromirror loaded with the sensing branch of an MZI in collaboration with LOPMD. As unloaded demonstrator a rotatable mirror with evanescent field read-out by MZI has been fabricated in collaboration with MESA+, research institute at the University of Twente, the Netherlands.

2 Loaded type demonstrator

According to the idea of this demonstrator type the mechanical behavior of the mirror system can be characterized by the deformation of waveguide films forming a sensing arm of an MZI on top of the mirror and crossing the hinges. The second arm of the MZI is located on top of bulk-Si (Fig. 1). Inserting a light wave, the MZI output signal contains the required information about the optical path difference. The changes of the sensing arm are a result of mirror membrane/ hinge deformations due to local changes of the waveguide refractive index. This offers the extraction of information about the mechanical performance of the micromirror (rotation, out-of plane displacement of mirror plate etc.) [1].

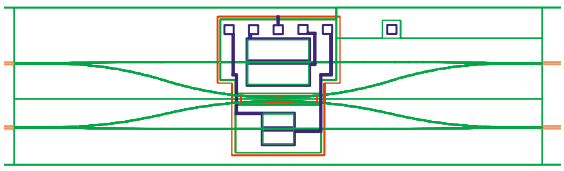

Figure 1. Schematic drawing of the loaded type demonstrator structure including two types of mirror

For the MZI structure a single mode buried channel waveguide based on silica/silicon oxinitride/silica structure was selected, performing a low optical attenuation (0.9 dB/cm) and acceptable coupling efficiency (around 50%) from waveguide to a standard fibre. One of the main difficulties of integrating such waveguides is the modification of mechanical properties of the mirror due to the compressive stress caused by PECVD deposition of waveguide films. Despite this and a lot of other challenges: KOH

compatibility of waveguide films, adhesion issues, wafer bonding and the multiple wafer exchange between LOPMD and ZfM, finally demonstrators have been fabricated successfully. An integrated device is shown in Fig. 2.

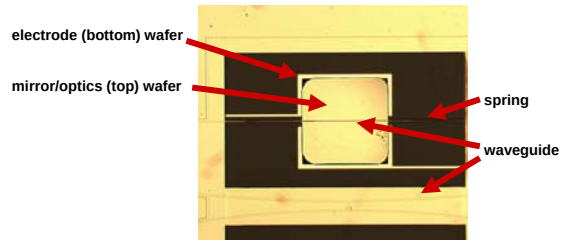

Figure 2. Microphotograph of an integrated loaded type demonstrator structure after fabrication

As illustrated in Fig. 3, prototypes of these structures indicate that light is propagating through the waveguide structures. Measurements are still in progress at LOPMD and Warsaw University - Faculty of Mechatronics.

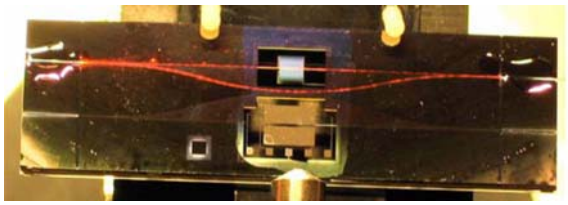

Figure 3. MZI loaded demonstrator in operation - light path (red) crossing the small mirror is clearly visible; photograph and test assembly from LOPMD

3 Unloaded demonstrators using evanescent field MZI read-out

This work package was established as an alternative method in order to avoid the mechanical contact between waveguide structure and MEMS [2]. Evanescent field sensing of movable objects requires a penetration of the evanescent field of a guided mode by this object, affecting the refractive index distribution within the concerned region. Following this idea a joint concept has been developed enabling a separate fabrication of the mirror and the evanescent field sensing device (Fig.4).

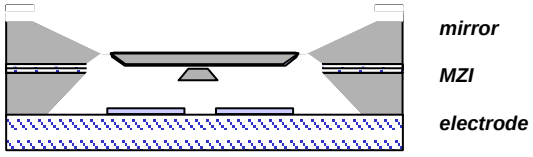

Figure 4. Schematic drawing of the unloaded demonstrator

Due to the decoupling of both technologies (MEMS, waveguide structure), the yield of mirror structures fabricated at wafer level (electrode and mirror wafer) was nearly 100 %. The most critical challenge for the completion of this kind of demonstrator turned out to be the wafer bonding processes. The silicon fusion bonding (SFB) of the mirror wafer and the optics wafer is complicated due to an increased surface roughening (caused by etching processes) and by the required metallization of the mirror surface (backside) in order to increase the effect onto the evanescent field sensing. However there is no other option because the distance between sensing device and mirror surface has to be well-defined.

In order to bond this wafer stack with the electrode wafer, adhesive bonding procedures were examined. This way a novel bonding process has been developed by using an epoxy resin [3]. It is characterized by low temperature and a photolithographic patterning. From experimental measurements a surface energy up to 20 J/m^2 is obtained. An additional distance between the wafers according to the resin thickness should be not critical in case of the electrode bonding. Demonstrator devices as shown in Fig. 5 are characterized now at MESA$^+$.

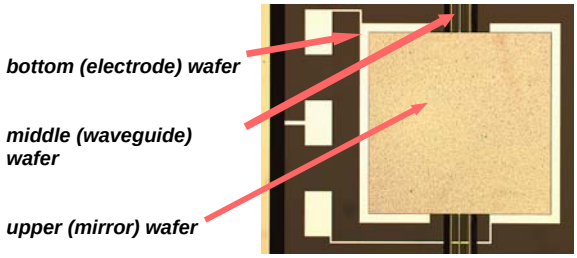

Figure 5. Unloaded demonstrator after fabrication (at wafer level)

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A Novel Microactuator Based on the Working Principle of a Step-by-Step Switchgear

B. Schröter[1], J. Mehner[2], K. Hiller[1], T. Geßner[1,2], W. Dötzel[1]
[1] Chemnitz University of Technology
[2] Fraunhofer IZM

1 Introduction

Switchgears are to be found in many classical applications, e.g. mechanical clockworks, film projectors or typewriters. They are able to start up predefined positions and hold them subsequently [1,2]. A microstructure has been developed that works alike.

There is plenty of examples where scaling down established operational principles has led to successful micromechanical applications [3]. Various sensors like accelerometers [4], pressure gauges [5], gyroscopes [6] or vibration sensors [7] have been realised. Actuation principles are subject to miniaturisation, as well. Micromirrors for laser scanning devices [8] or mirror arrays for highly sophisticated optical applications [9, 10] have been previously demonstrated.

The micromechanical switchgear described in this paper makes use of single-crystal silicon, the most important material in semiconductor technology, as structural material. Due to the development of microelectronics, hyperpure silicon of crystalline perfection is available and can in many ways be structured by etching techniques. In addition to its excellent electrical properties, this material has very good mechanical properties [11]. Single-crystal silicon has a comparatively high strength. In a wide range it exhibits linearly elastic behaviour and does hardly exhibit hysteresis and fatigue effects, which enables the manufacture of springs with very well reproducible force-displacement characteristics. The elastic constants exhibit a relatively low temperature dependence. Compared to other materials, silicon has a low thermal expansion, is corrosion-resistant and can also be used at high temperatures. No ageing of any kind is observed.

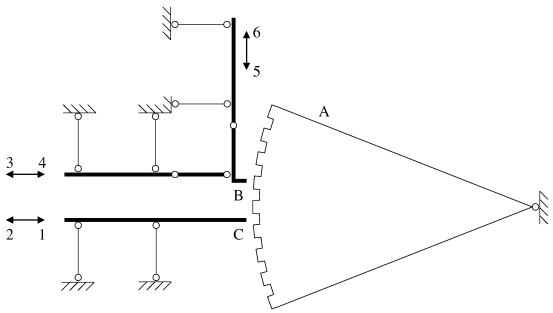

Fig. 1: *Working principle, A: Toothed segment, B, C: shift dogs, 1...6 stops*

2 Working principle

Figure 1 is a schematic drawing of the microstructure presented in this work. A toothed segment (A) performs a pivoting motion within the wafer plane. For this purpose the lower shift dog (C) can be engaged with the teeth by means of a straight-line infeed movement. In addition to this, the upper shift dog (B) can be deflected upwards and downwards by half a cycle size, i.e. 5µm. Advancing to the next position by one tooth is effected in six individual steps, at least one of the shift dogs having to be engaged in each case in order to keep the current position. Stops limit the travels. That way, no position control is needed. The activation takes place by means of a logical circuit, which drives the individual electrodes via driver transistors.

3 Design

The radius of the toothed segment of approximately 1.9 mm, results from the designing guidelines that a make-and-break cycle has to correspond to a length of arc of 10µm and an angle of 0.3 degrees. Thus an overall-angle of 15deg. can be passed through in fifty cycles. The electrostatic drives have been dimensioned for an operating voltage of 50 V. The thickness of the upper wafer (see fig. 4) and thus freely movable structures amounts to 50µm. The individual electrodes are insulated from each other by

separation trenches and thermal oxide situated below them.

All hinges, drawn as circles in fig. 1, are local compliances. They have been designed to a length of 25µm and a width of 3µm. Flexible hinges have been chosen, because rigid bodies in solid pairing (sliding or rolling pairing with friction and wear) are restricted in their use in micromechanics [12]. That way, the entire structure becomes monolithic and no assembly is required. This avoids handling problems and there are no adjustment errors or manufacturing tolerances that keep the device from functioning correctly.

The drives make use of the electrostatic force. Fig. 2 shows this with respect to the displacement of shift dog B in direction 5 (or 6, symmetry, see fig. 1). The restoring force produced by the hinges implemented as leaf springs is a linear function of the displacement and tends to pull back to neutral position. Both forces sum up to the resulting force that causes the toothed segment to move on by one step.

Fig. 3 is a light micrograph of the microstructure which has been made. The pivotally mounted toothed segment and parts of the electrostatic drives are to be seen. The individual trapeziform teeth are shown in Fig. 4, which is a SEM micrograph.

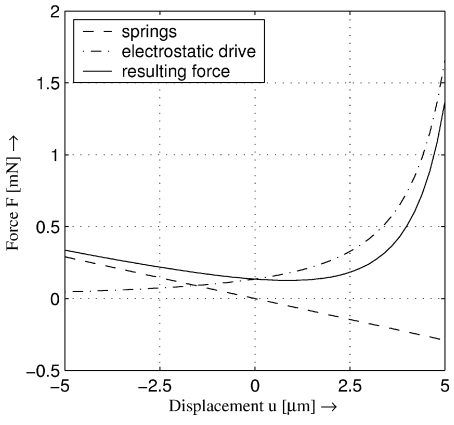

Fig. 2: Force vs. Displacement plot

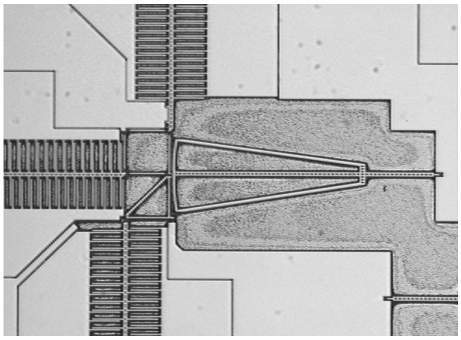

Fig. 3: *Light micrograph of the microactuator, the toothed segment is 1.9mm long*

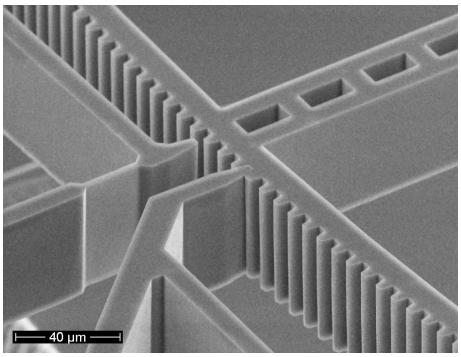

Fig. 4: *Close-up SEM micrograph of the teeth and shift dogs, the lower shift dog is engaged*

4 Measurements

For dynamic measurements a setup according to figure 6 is used. The specimen is sitting under a microscope (1) which is coupled via an optical fibre (3) to a laser-doppler interferometer (4). Its output signal is observed on a digital sampling oscilloscope (5) or a spectrum analyzer, respectively, depending on the desired information. If necessary, the data is transferred to a computer (6) for further calculations. A beam splitter (2) passes the picture through to a CCD camera (7) so the experiments can be observed on a video monitor (8).

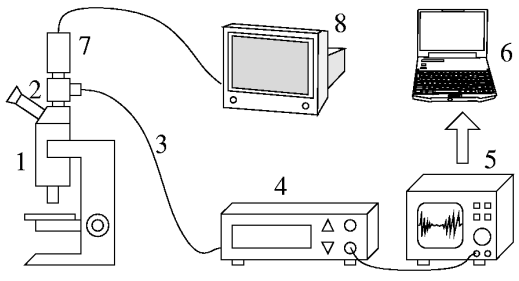

Fig. 6: Setup for dynamic characterization

5 Results

The geometrical measurements revealed, that the structures are on the top side about 0.4µm wider than on the bottom. The DRIE process had been adjusted to yield to such a profile rather than the trenches close with increasing depth. Thus, the vertical walls are slightly undercut with an angle of 0.2 degrees. This assures that no clamping between shift dogs and teeth occurs.

Fig. 7 shows the displacement vs. time characteristics of a forward step obtained with the setup drawn in fig. 6. Shift dog B is engaged with the toothed segment A. Drive 6 is switched off as drive 5 is activated. After a short time of about 14µs drive 6 has been discharged and parts B and A start to move towards stop 5. After another 50µs the end position is reached. Due to the large holding force (see fig. 2), hardly any chattering occurs.

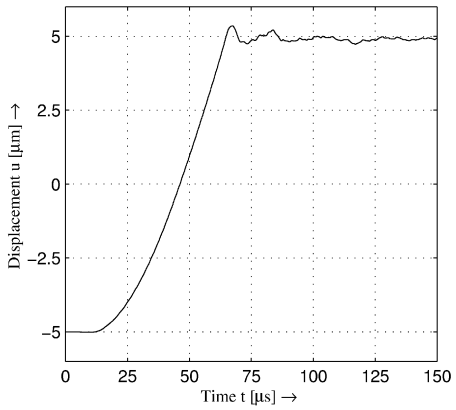

Fig. 7: *Displacement vs. Time plot*

Operating all drives according to table 1, switching frequencies of up to one Kilohertz have been reached.

6 Conclusion

We succeeded in scaling down the operating principle of a step-by-step switchgear as it is known from precision engineering to micromechanical dimensions, adapting it to micro techniques and proving its functionality. High working frequencies could be reached because of the small moving masses. The introduced microstructure represents a new class of microactuators.

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Fabrication of SOI substrates with buried silicide layers for BICMOS-applications

M. Wiemer[1], S. Zimmermann[2], Q.T. Zhao[3], B. Trui[4], C. Kaufmann[2], S. Mantl[3], V. Dudek[4], T. Gessner[1,2]

1) Fraunhofer IZM, Department Micro Devices and Equipment, 09126 Chemnitz, Germany,
2) Chemnitz University of Technology, Center for Microtechnologies, 09107 Chemnitz, Germany
3) ISG 1-IT, Forschungszentrum Jülich, 52425 Jülich, Germany
4) ATMEL Germany GmbH, 74072 Heilbronn, Germany

A new approach for fabrication of special SOI substrates offering the possibility of high performance CMOS and high performance bipolar technology on the same SOI substrate will described. The new substrates consist of a buried silicide layer on top of the buried oxide covered with a thin silicon film for the device fabrication.

There are two versions to prepare a SOI substrate with a buried $CoSi_2$ layer. The first technology, is a combination of the cobalt-salicide [1] process and a technique, which includes different CMP-processes and a wafer bonding step. This means the first technology includes a modified BESOI regime and has several similarities with the BESOI process, described in [2]. The process flow is shown in fig. 1.

The starting point for the first version is a commercial SOI wafer with 1 µm buried oxide and a 300 nm thick Si device layer. After the removal of the native oxide 30 nm cobalt and 8 nm Ti were deposited without a vacuum break. The conversion of the cobalt film into a $CoSi_2$ includes two RTA steps and one wet chemical process. The process results in a structured $CoSi_2$ film on silicon and is known as cobalt salicide process. To get plan surfaces for the bonding process, 500 nm PECVD-SiO_2 were deposited and the steps were removed using an oxide CMP process. The final thickness after the CMP process was 250 nm. All CMP processes were performed using an Applied Materials Mirra polisher. Afterwards the wafer was bonded to a handle substrate deposited with 250 nm oxide by high temperature silicon direct bonding. The result is the structure presented in fig. 1. The handle wafer with oxide is on the bottom and on the top is the SOI-substrate with the buried $CoSi_2$ layer. To finish the SOI-substrate it is necessary to remove the former handle wafer of the SOI-substrate. In a first step the handle wafer of the SOI substrate was grinded back to a final silicon thickness of 20 µm. The last 20 µm were selective etched to the buried oxide of the SOI substrate using a spin etch tool. In a next step the buried oxide of the SOI substrate is etched back chemically in diluted HF. In the last step a silicon CMP process removed the surface roughness of our new SOI substrates.

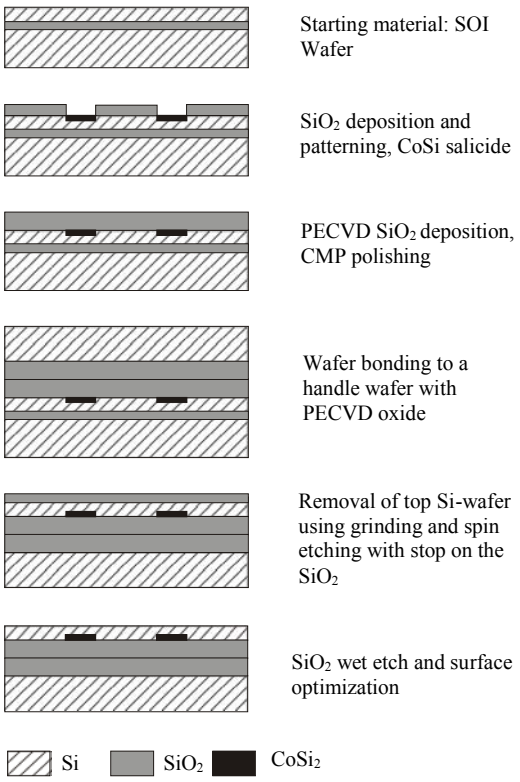

Fig. 1: Process flow to prepare a SOI substrate with buried silicides using the modified BESOI regime

The second version to fabricate SOI substrates with buried silicide is a combination between cobalt salicide process, silicon layer transfer by hydrogen implanted layer splitting (HILS) and silicon direct wafer bonding. The process flow is shown in fig. 2.

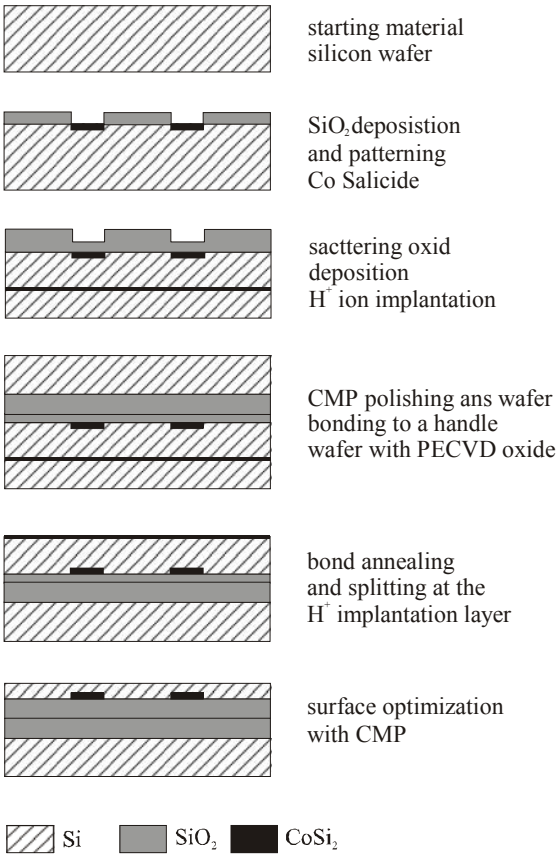

Fig. 2: Process flow to prepare a SOI substrate with buried silicides using the hydrogen implanted layer splitting regime (HILS)

An IR image of a bonded wafer pair is shown in fig. 3. We tested LP-CVD and PE-CVD SiO_2 to find the most suitable interface material for the wafer bonding process. The best results were obtained with PE-CVD SiO_2. But it is necessary to anneal the wafers before the bonding process. This step was performed to suppress hydrogen out gazing during the bond annealing. After the bonding process an annealing at 800 °C for 4h in N_2 is necessary to improve the bond strength.

The roughness of the $CoSi_2$/Si interface was measured with AFM after the removal of the silicide with 35 % HF solution. The measurements show a roughness average value of 11nm.

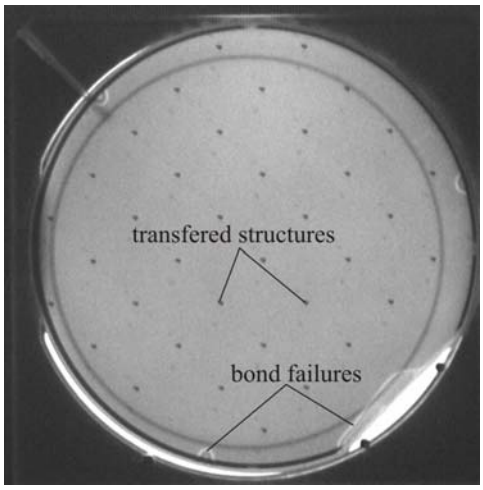

Fig. 3: IR image of a bonded wafer pair

A cross section through such a structure is shown in fig. 4. It can be seen that the $CoSi_2$ surface is moving into the silicon because the large silicon consumption during the cobalt silicidation.

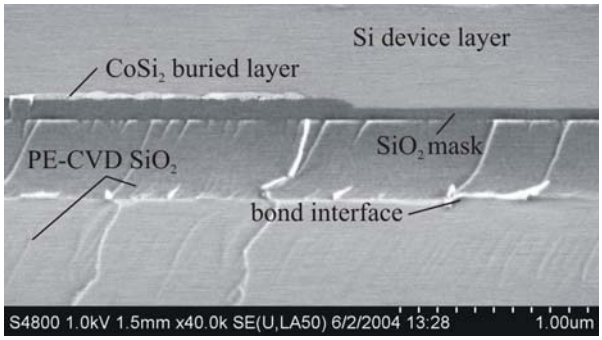

Fig. 4: SEM cross section of the SOI substrate with buried $CoSi_2$

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Key words

Silicides, SOI, silicon direct wafer bonding, hydrogen implantation

Micro Igniters based on WSi_x thin films

Löbner, Bernd[1]; Nestler, Jörg[1] ; Gessner, Thomas[1]; Weiß, Uwe[2]
[1] Chemnitz University of Technology, Center for Microtechnologies
[2] FLEXIVA automation & Robotik GmbH, Chemnitz

1 Introduction

Thin film based ignition elements for airbag systems have faster ignition times and require a lower ignition energy compared to commercially available wire-based igniters. Thus, WSi_x based igniters on a silicon substrate were developed and investigated. Their properties were then adjusted to fit certain fire and no-fire conditions.

2 Design and Fabrication

Ignition chips of different geometries were designed and fabricated on 4 inch silicon wafer substrates. A SiO_2 layer was grown on the silicon to provide electrical insulation to the substrate. Subsequently, WSi_x was sputtered and tempered. For the electrical contact pads an aluminium layer was sputtered on the WSi_x film.

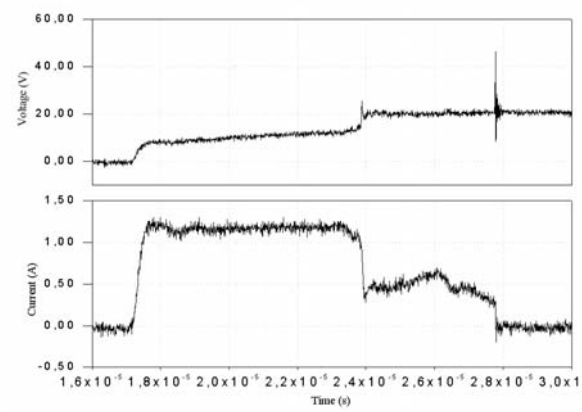
3 Packaging and Characterization

3.1. Resistance and fire conditions

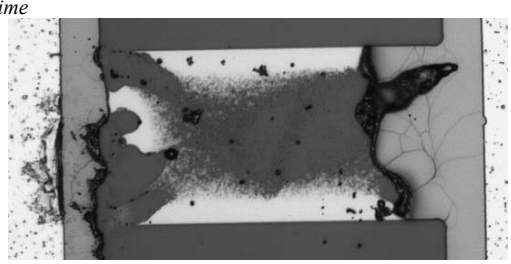
The fabricated ignition elements were electrically characterized. After resistance measurements, some of the structures were ignited by a constant current of 1,2A or 1,75A. Fig. 3.1.a shows an example of the measured current and voltage during the ignition process. The destruction of the bridge starts where the current drops to a significant lower value, and ends, when the current drops to zero. A destroyed igniter bridge is shown in Fig. 3.1.b.

3.2. Heating and destruction process

For better understanding of the working principle of the ignition process, different currents were applied to WSi_x bridges with dimensions of L=200µm, W=100µm (Fig. 3.2). These relatively large dimensions were chosen to slow down the heating process and therefore getting better time and current resolution.



a) Voltage and Current during the ignition process as function of time



b) Destroyed WSix bridge after I=1,2A

Fig. 3.1: Ignition of a WSix Bridge (L=100µm, W=50µm) with a constant current of I=1,2A

Until a certain current $I_{nofire1}$, the temperature due to the current density in the structure is not sufficient to destroy the WSi_x bridge even after a time of more than 1,5ms. The resistance increase, which is correlated to the temperature of the structure, was found to be reversible and no damage could be seen or measured at the bridge afterwards. Since the resistance increase for currents below $I_{nofire1}$ follows an asymptotic behaviour, reversibility can also be assumed after a much longer time than shown in Fig 3.2.
The temperature inside the bridge mainly depends on the current density and the heat dissipation to the substrate, which also has been verified by FEM simulations. Both, current density and heat dissipation were adjusted by changing bridge geometry and process

technology to fulfil certain all-fire and no-fire conditions.

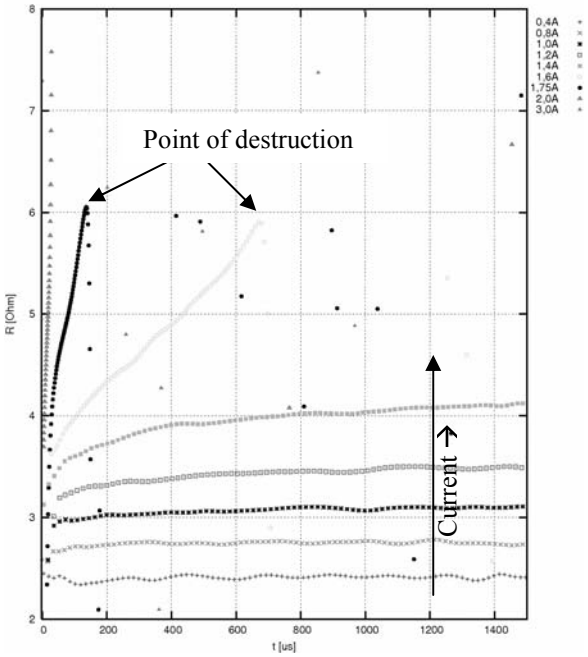
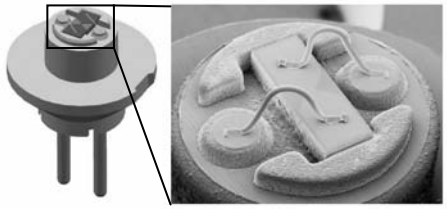


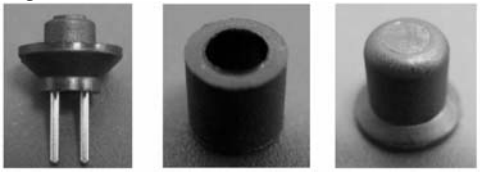
Fig. 3.2: Resistance of a large WSi_x bridge (L=200µm, W=100µm) as function of time for different currents. A higher current leads to a faster increasing of temperature. If the temperature is sufficient to destroy the structure (ignition point), the current defines the ignition speed.

3.3 Packaging and Pyrotechnics

A full-plastic igniter package was developed by the company Fahrzeugelektrik Pirna GmbH. For ESD protection an additional capacitor was integrated into the package.
The igniter chips fabricated at the Center for Microtechnologies were mounted and wire-bonded to the contact pins of the package base (Fig. 3.3).



a) CAD drawing of the package base and SEM picture of igniter chip which has been wire-bonded to the contact pins of the package base.



b) Photographs of the parts of the igniter package (package base with contact pins, charge holder, cap)

Fig. 3.3: Full-plastic igniter package

Subsequently, a charge holder was ultrasonically welded on the package base.
The cavity inside the charge holder was then filled with liquid pyrotechnics provided by the company NICO Pyrotechnik GmbH and successfully ignited. Fig. 3.4 shows voltage, current and light emission of the full ignition process.

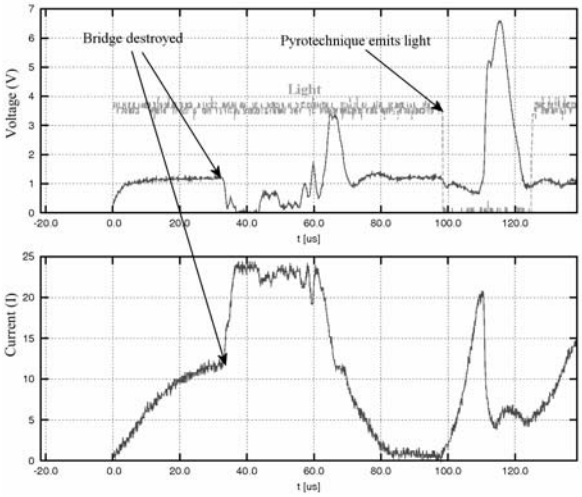


Fig. 3.4: Voltage and current as function of time during ignition of a igniter filled with pyrotechnics. The delay between destruction of the bridge and ignition of the pyrotechnics (indicated by the light emission) is about 40..50µs

4 Conclusion

Micro igniters based of a WSi_x thin film bridge were successfully developed and integrated into a full-plastic package. The ignition parameters of these WSi_x bridges are adjustable in a wide range according to the desired application. The Micro igniter chips together with the package showed good and reliable ignition behaviour both with and without pyrotechnics. First tests showed good ESD stability, but additional ESD, EMD and climatic tests have to be performed.

5 Acknowledgments

We would like to thank the company NICO Pyrotechnik GmbH for providing the liquid pyrotechnics and the test environment.
The project was a joint research project with the companies Fahrzeugelektrik Pirna GmbH (FEP) and FLEXIVA automation & Robotik GmbH and supported by SMWA (Sächsisches Staatsministerium für Wirtschaft und Arbeit).

Micro Systems Applications in Biotechnology and Health Care

Jörg Nestler[1], Mario Baum[2], Thomas Otto[2], Thomas Gessner[1,2]
[1] Chemnitz University of Technology, Faculty of Electrical Engineering, Center for Microtechnologies (ZfM)
[2] Fraunhofer Institute for Reliability and Microintegration IZM, Dept. Micro Devices and Equipment Chemnitz

1 Introduction

After the commercialisation of MEMS (Micro Electro Mechanical Systems) in general, the fields of biology and medical care are about to create a new big market for micro systems. Biomedical applications mean both biotechnology and medical applications. The combination with micro system technologies is called BioMEMS, micro systems for biomedical applications.

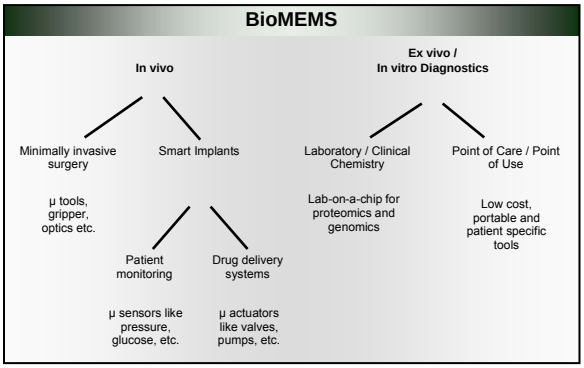


Fig.1: BioMEMS – a survey

2 *In Vivo* applications

From the *in vivo* application fields shown in Fig. 1, some essential requirements like small device dimensions, high reliability and durability, a high level of integration, and special durable biocompatible packages for *in vivo* MEMS devices can be derived.
Despite of the last one, all these points would be fulfilled by classical silicon based micro systems or other established technologies (like microelectronics).
For example implantable pressure sensors are being developed. Potential applications for such sensor implants will be the continuous monitoring of the pressure of blood, eyes or bladder. [1][2]
Other sensor developments with high impact are implantable glucose sensors for diabetes patients. These sensors would be able to monitor the glucose concentration in the blood in real-time, hence making self-testing several times a day unnecessary. This would bring a new standard of living for the increasing number of diabetes patients.
However, a challenge for the usage of micro systems in these applications is that sensors as well as actuators have to have direct contact with the human body. Thus, "encapsulation" of the sensor by cells or degradation of the sensing surface layer is one of the biggest problems to be solved. At present, subcutaneous implantation of the glucose sensors seems to be the most promising alternative. Several companies have already started to follow this route, but a real break through for long term application has not come yet. [3][4]
From this simple example it can be seen, that biocompatible packaging issues are one of the most challenging problems for the *in vivo* application of micro systems. Solving these problems can be the necessary impulse needed for commercialization of a great variety of micro systems for *in vivo* applications. Therefore, strong interdisciplinary research in the area of biocompatible packaging is necessary.
Once these problems have been overcome, future developments will combine these sensor technologies with micro scaled actuators like drug delivery systems. Larger implantable systems, especially for insulin dosage are already available on the market.

3 *In Vitro* applications

In some of the i*n vitro* application fields shown in Fig. 1 (especially point-of-care) the same kinds of sensors as for the above mentioned prostheses are applicable. These sensors could be pressure, acceleration, angular rate, vibration and inclination sensors that monitor the current "state" of patients or of elder persons.
The bigger share of in vitro applications is diagnostics, mainly *point-of-care* diagnostics and novel analytical systems for in-lab use. For both a high need for disposable systems is recognized. Disposable systems in general should be cheap,

thus material selection and their processing has to be cost-effective.

In general, *point-of-care* sensor systems have to be easy to use, while for in-lab systems high throughput analysis is important. However, in both cases sensors have to interact with biological samples. Due to the reasons outlined above, the following general properties and requirements for disposable micro systems in biotechnological applications (mainly sensor systems) could be derived:

- larger sensing area or parallel analysis necessary to overcome statistical uncertainty , to improve cross sensitivity or to enable the device for parallelisation
- low material price, since batch processing is limited due to minimal possible sensor size
- low technological processing costs
- sterilization is still critical for these applications (which is one of the reasons for the devices to be disposable)
- Chemical and biological compatibility with conventional systems and reagents

Most of these points can be better fulfilled by other materials than silicon. Especially polymers play a major role for disposable devices, but their processing in micro scale is not that far developed yet as for silicon based devices.

Another advantage of polymers is their lower price compared to silicon, and the possibility to precisely replicate polymer devices using technologies like hot embossing [5], micro injection moulding and UV casting.

First developments therefore concentrated on applications for simple micro structured polymer substrates.

Due to the ease of polymer structuring and their optical transparency, it is comparably easy to integrate passive optical parts like waveguides, gratings or lenses. Since optical detection methods play a major role in biotechnology integrated optics can bring a new quality to micro structured devices for applications in biotechnology.

The evolution of polymer electronics, polymer based electro-optical components and electrically deformable polymers could bring up a new generation of disposable polymer based sensor systems for biomedical applications. Such sensor systems would include also active optical sensing components and fluid actuation components for sample preparation and sample transport. Especially in the point of care fields, where accuracy is not as important as in laboratories, these sensors developments could have a high potential due to their combination of comparative price for high volumes and high functionality.

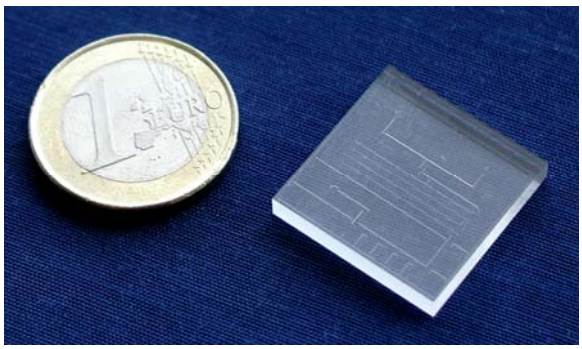


Fig.2: Polymer chip with micro structured fluidic channels and integrated optical waveguides

4 Conclusions

BioMEMS will have a high impact to in vivo as well as in vitro biomedical markets. Especially both fields implantable miniaturized systems and low cost analysis chips as shown are preferred markets for micro systems. However, the main challenges are not arising from the field of micro technology, but from the interface between biological and technical systems.

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Bulk Micromachined Ultrasonic Transducers

Chenping Jia[1], Maik Wiemer[2], Thomas Otto[2], Thomas Gessner[1,2]

[1] Chemnitz University of Technology, Center for Microtechnologies, D-09107, Chemnitz, Germany
[2] Fraunhofer-IZM, Department of Micro Device and Equipment, D-09126, Chemnitz, Germany

1 Introduction

Ultrasonic transducer has extensive applications in non-destructive evaluation (NDE), medical imaging and so on. In order to improve the impedance matching property of airborne transducer, and introduce such transducers into scanning application, a bulk micromachined ultrasonic transducer is designed and fabricated. Initial investigation results showed that, this newly developed transducer has the advantages of uniform cavity, consistent elements, and reliable vibration membrane. It is expected that this innovative invention will surpass most traditional cMUTs design, and win wide acceptance in air-coupled ultrasonic application.

2 Fabrication Process

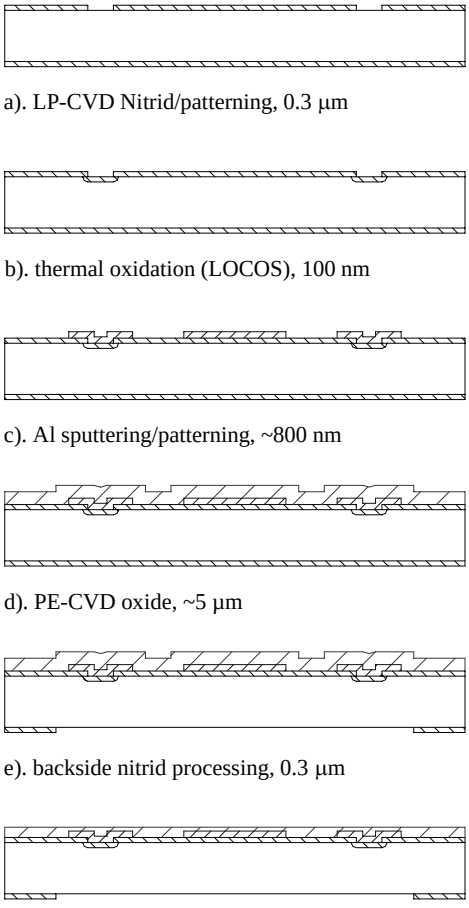
Fabrication of the proposed transducer involves the individual preparation of membrane and cavity wafer, as well as the bonding of these two components. This will be illustrated in detail in following sections.

2.1 Membrane Wafer Fabrication

Fabrication procedure of membrane wafer is depicted in Fig. 1. First, 300 nm LP-CVD nitride is deposited and patterned. Next, 100 nm LOCOS oxide is grown on some local regions of the wafer, with nitride as mask. Following thermal oxidation, 800 nm Al is sputtered. This Al layer acts as the top electrode of the proposed transducer. When the metal electrode is made ready, 5 µm PE-CVD oxide is deposited on it. This oxide layer has two functions: first, it provides enough buffering for future CMP polishing; second, it protects the Al layer from damaging and establishes a good insulation.

Before further processing, mask windows are etched in the nitride layer on the backside of the wafer. This step is necessary for future perforation etching, because at the end of the process flow, the membrane will be released from backside.

When the window etching is successfully transferred, a CMP process is employed to planarize the unevenness of the front side and to improve the surface smoothness. Such smoothness and flatness are very important for future wafer bonding.



a). LP-CVD Nitrid/patterning, 0.3 µm

b). thermal oxidation (LOCOS), 100 nm

c). Al sputtering/patterning, ~800 nm

d). PE-CVD oxide, ~5 µm

e). backside nitrid processing, 0.3 µm

f). frontside CMP, 4 µm removal

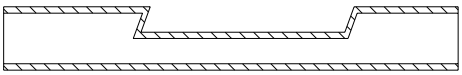
Fig. 1: Membrane wafer fabrication.

2.2 Cavity Wafer Preparation

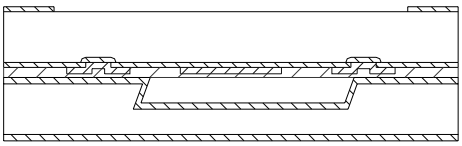
Preparation of cavity wafer is relative simple: patterns are transferred into bulk silicon and cavities are etched in it. Depending on the desired cavity geometry, wet or dry etching process can be utilized. For our application, hexagonal structures are preferred, hence, a combined dry and wet etching is adopted.

2.3 Wafer Bonding

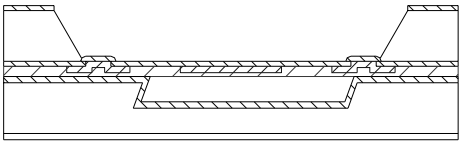
When both wafer components are ready, they are joined together by silicon direct bonding (Fig. 2). The bonding is carried out in a wafer bonder under vacuum, because lower pressure in the sealed cavity is preferable to the normal operation of the transducers.



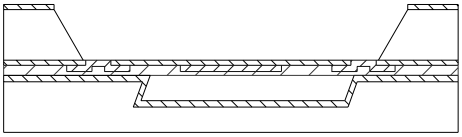
a'). cavity wafer preparation



b'). SFB/360°C annealing, in vacuum



c'). perforation etching



d'). oxide etching (wet or dry), 100 nm

Fig. 2: Cavity wafer preparation.

After bonding, an in-site annealing process is operated. This step is used to increase the strength of the bonding. Following that, the wafer pair is dipped in KOH solution for perforation etching. To expose the Al bonding pads, an additional HF etching is also carried out. A bonded wafer stack is shown in Fig. 3, achieving a yielding rate of almost 100%.

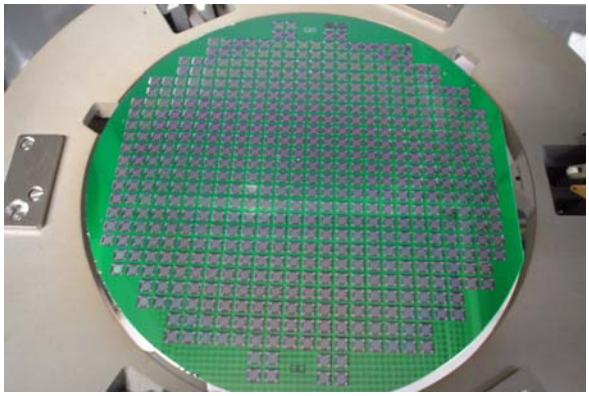


Fig. 3: Ultrasonic transducers fabricated on a 6" wafer.

3 Sample Quality Inspection

To inspect the quality of the fabricated transducer, as well as the appearance of the cell array. SEM is used. Fig. 4 shows a top view of the cleared membrane after perforation etching, presents whose completeness and homogeneity.

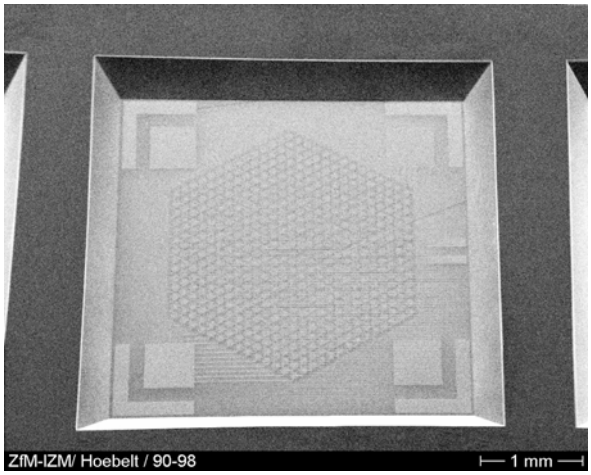


Fig. 4: SEM photo of the honeycomb-like transducer array.

To further evaluate the quality of the metal electrode and the cavity component, some optical photos were taken. Fig. 5 shows one of these photos. With this photo, one can see that both the cavities and the electrodes are tide and regular.

Fig. 5: Detailed image of one transducer element.

4 Discussions

The transducer proposed in this report is fabricated by bulk process, therefore, very uniform vibration membrane and arbitrarily large electrodes gap can be realized. Since such arrangement greatly improves the consistency of the cell elements, and avoids the risk of stiction during membrane releasing, it is expected that this process will win great acceptance in transducer fabrication.

Oscillations of the direct tunneling current in a MOS capacitor with ultra- thin gate dielectrics

E. P. Nakhmedov, C. Radehaus and E. Nadimi
TU Chemnitz
Faculty of Electrical Engineering, Chair Opto- and Solid State Electronics

Abstract

A novel quasi- classical expression is derived, that expresses the gate oxide thickness by the electric field strengths corresponding to two subsequent extrema in the leakage current oscillations. By analyzing various experimental gate current data, the new formula is successfully applied to determine the oxide thickness.

1. Introduction

Oscillations of the electron transmission through the triangular barrier has been firstly studied theoretically by Gundlach [1] in Metal-Insulator- Metal (MIM) structures. Although the leakage current oscillations have not been observed in MIM capacitors, experimental evidence toward the oscillations at high gate voltage has been revealed firstly by Maserjian et al. [2, 3] in Metal- Oxide- Semiconductor (MOS) structures with thin gate oxide.

To explain the electric field (F) dependence of the measured tunneling current, the Fowler- Nordheim (FN) quasi- classical expression $J_0(F)$ for the tunnelling current is usually combined with the oscillatory amplitude B of Gundlach's quantum- mechanical expression for the transmission coefficient, which is responsible for the oscillation of the total tunnelling current $J(F)$:

$$J(F) = B\,J_0(F), \qquad (1)$$

where $J_0(F) = AF^2 \exp(-C/F)$ and (2)

$$B = \left[\, Ai^2(-aL_{cb}) + (a/k)^2\, Ai'^2(-aL_{cb}) \right]^{-1}. \qquad (3)$$

A and C in the FN expression (2) are defined as:

$A = q^3 m_{si}^* / (16\pi^2 \hbar m_{ox}^* \phi_B)$

and

$$C = 2\int_0^{\phi_B} k[\phi]\, d\phi = \left(8\pi/3q\hbar\right)\left(2m_{ox}^*\phi_B^3\right)^{1/2}$$

where ϕ_B is the semiconductor- oxide barrier height, m_{si}^* and m_{ox}^* are the electron effective masses in the silicon substrate and gate oxide, respectively. $Ai(x)$ and $Ai'(x)$ in Eq.(3) are the Airy function and its derivative, respectively. The coefficient a and the distance L_{cb}, travelled by the electron with energy E in the conduction band of SiO_2 are given by $a = \left(2m_{ox}^* qF/\hbar^2\right)^{1/3}$ and $L_{cb} = t_{ox} - (\phi_B - E)/qF$, respectively.

Analytical investigations of the oscillatory gate current shows that the positions of the extrema in the current oscillation depend on the internal characteristics of the system. These are the gate oxide thickness t_{ox}, the barrier height ϕ_B, the effective mass and the Fermi energy of electrons E_F in the system, and also on the strength of the applied electric field F. This fact allows us to express the oxide thickness via the values of the electric field strength F at the extrema of the oscillations $F = F_n$. The conventional method to determine the gate oxide thickness is based on the oscillative nature of the quantum prefactor B given by Eq.(3), which gets maximal values at zero points of the Airy function, $Ai(-aL_{cb})_{F=F_n} = 0$, and minimal values at zero points of the derivative of the Airy function, $Ai'(-aL_{cb})_{F=F_n} = 0$.

We present a new quasi- classical method to determine the gate oxide thickness by measuring the electric fields corresponding to two subsequent extrema of oscillations [4]. Careful analyses of experimental data of the gate current oscillations, to determine the oxide thickness by applying our method as well as the conventional method, shows that accuracy of our method is higher than that of the conventional method.

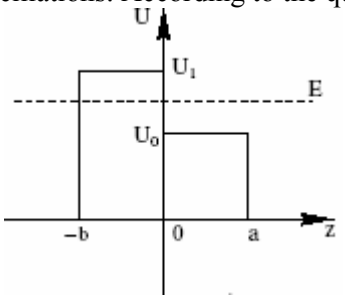
2. Determination of the oxide thickness from the oscillation period

To determine the oxide thickness t_{ox} by the conventional method [5], the following qualitative relation between t_{ox} and the measured values of the electric field F_n at the n th maximum (or n th minimum) is used:

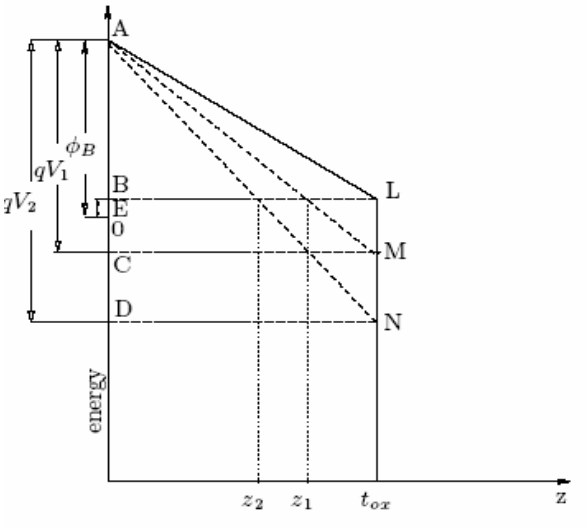
$$\left(\frac{2qm_{ox}^{*}F_n}{\hbar^2}\right)^{1/3}\left(t_{ox}-\frac{\phi_B-E_F}{qF_n}\right)=K_n, \qquad (4)$$

where K_n is the nth zero of the Airy function (of the derivative of the Airy function).

We suggest a quasi- classic theory to determine the oxide thickness by knowing the positions of two subsequent extrema in the current oscillations. According to the quantum-



(a)



(b)

Fig.1: (a) Tunneling of a particle with energy $U_0 < E < U_1$ through a quantum barrier of width b with subsequent transmission over a barrier of width a. (b) Tilting of the conduction band edge of SiO_2 under the gate voltage. The line *AL* corresponds to the voltage, where a crossover from the WKB regime to the FN regime by increasing the gate voltage takes place. The lines *AM* and *AN* characterize the conduction band tilting under the voltages V_1 and V_2, corresponding to two subsequent extrema in the current oscillations.

mechanic the transmission over a potential well or a potential barrier of width a, the transmission coefficient $|T|^2$ reaches the extremal values at the points $ka=\pi(n-\alpha)$ $n=1,2,3,...$, which correspond to maxima for $\alpha=0$ and minima for $\alpha=1/2$. Since the depth of a potential well $-U_0$ or the height of a barrier U_0 is constant, the wavelength $k=\sqrt{2m(E-|U_0|)/\hbar^2}$ of the transmitted particle with energy *E* takes also constant values at every point of motion over the well or barrier. If the spatial distance between two subsequent maxima or minima is Δa, then $\Delta a\, k=\pi$.

To understand the nature of oscillations deeper, we have studied the transmission of a particle with energy $U_0 < E < U_1$ through the more complicated structure, shown in Fig.1a analytically. Minimizing $|T|^2$ with respect to a gives the following condition for the extremal points:

$$\tan(2ka)=\frac{2k\kappa(q^2+\kappa^2)\tanh(\kappa b)}{\kappa^2(k^2-q^2)+(k^2q^2-\kappa^4)\tanh^2(\kappa b)} \qquad (5)$$

where $q^2=2mE/\hbar^2$, $\kappa^2=2m(U_1-E)/\hbar^2$.

The transmission coefficient $|T|^2$ can be seen from Eq.(5) to take maximal and minimal values at $ka=\pi(n-\alpha)+\delta\alpha/2$ for $\alpha=0$ and $\alpha=1/2$, correspondingly. The shift $\delta\alpha$ occurs due to tunnelling of an electron through the potential barrier of width b. $\delta\alpha$ vanishes as $b\to 0$ or $U_1\to U_0$, and it does not depend neither on the distance a nor on the electric field. The distance Δa obeys again the relation of $\Delta a\, k=\pi$.

The wave number of an electron, which propagates in the tilted conduction band of silicon oxide, depends on the spatial coordinates, instead of $k=const$ as in the previous examples of electron motion over a potential barrier or well. Fig.1b shows the conduction band tilting of silica for different voltages. Imagine that an electron moves the distance $(t_{ox}-z_n)$ over the conduction band of SiO_2 under the applied voltage V_n, which corresponds to the nth maximum or minimum. Dividing the distance of $(t_{ox}-z_n)$ to *N* equal portions with length of Δz_i around the point z_i, an electron wave number $k(z_i)=\sqrt{2m_{ox}^{*}(E-U(z_i))/\hbar^2}$ can be roughly considered to be constant moving over a

rectangular barrier of width Δz_i. Summing up over all portions and taking $N \to \infty$ we get the condition to determine the position of nth maximum for $\alpha = 0$ or nth minimum for $\alpha = 1/2$:

$$\int_{z_n}^{t_{ox}} \sqrt{\frac{2m_{ox}^*}{\hbar^2}\big(E - U(z)\big)}\, dz = \pi(n-\alpha) + \delta\alpha, \quad (6)$$

where $\delta\alpha$ is a phase shift, $U(z) = \phi_B - qFz$. The distance z_1, e.g. for the first maximum or minimum can be found in Fig.1b from the triangle ACM as $z_1(\phi_B - E)/qF_1$. Routine calculations give the final formula for the oxide thickness t_{ox} by the values of the electric fields at two subsequent maxima or minima F_1 and F_2:

$$3\sqrt{2m_{ox}^*}/2\hbar\{(qF_2 t_{ox} - \phi_B + E)^{3/2}/qF_2 - (qF_1 t_{ox} - \phi_B + E)^{3/2}/qF_1\} = \pi \quad (7)$$

To check the validity of our quasi-classical oxide thickness determination method, we utilize experimental data for two subsequent maxima or minima of the gate voltage ($V_{\max 1}$, $V_{\max 2}$ or $V_{\min 1}$, $V_{\min 2}$) and the corresponding electric fields ($F_{\max 1}$, $F_{\max 2}$ or $F_{\min 1}$, $F_{\min 2}$) from three different measurements [2, 6, 7]. In the estimations we used $\phi_B = 3.1eV$ for the oxide barrier height and $E = E_F = 0.275eV$ for the electron energy that has been obtained in [8] from self- consistent solutions of the Schrödinger- Poisson system for the MOS capacitor. The effective masses of electrons in the Si substrate and in the gate oxide are taken to be $m_{si}^* = 0.916\, m_0$ and $m_{ox}^* = 0.51\, m_0$, respectively, where m_0 is the free electron mass. The comparative estimations of the oxide thicknesses by applying our method and the conventional method are presented in Table I. The oxide thickness determined by our method differ from experimental results less than 5%. Errors in the oxide thicknesses determined by the conventional method reach up to 90%.

Table I: Estimations of the oxide thickness from the current oscillations data of Refs.[2, 6, 7].

$V_{\max}$ ($V_{\min}$) (in Volt) or $F_{\max}$ ($F_{\min}$) (in MV/cm)	**Exper. Values** t_{ox}, nm	**Our Method** t_{ox}, nm (**Error**,%)	**Conven. Method** t_{ox}, nm (**Error**,%)
Ref.[2]			
$V_{\min 1}$=5.15	4.5	4.47 (0.6)	0.4 (91)
$V_{\min 2}$=6.12			
$V_{\max 1}$=5.58	4.5	4.73 (5.0)	1.2 (73)
$V_{\max 2}$=5.58			
Ref.[6]			
$V_{\min 1}$=5.05	4.5	4.52 (0.4)	0.44 (90)
$V_{\min 2}$=6.00			
$V_{\max 1}$=5.50	4.5	4.60 (2.0)	1.24 (72)
$V_{\max 2}$=6.47			
Ref.[7]			
$F_{\min 1}$=7.9	4.2	4.24 (1.0)	2.8 (33)
$F_{\min 2}$=10.2			
$F_{\max 1}$=7.4	5.2	5.30 (2.o)	3.7 (28)
$F_{\max 2}$=8.8			

3. Conclusions

The tunnelling current oscillations provide a valuable tool to determine the thickness and to check the quality of ultrathin gate oxides. We suggest a novel quasi- classical method to find the oxide thickness. Our expressions (6) and (7) depend, apart from the electric field, also on the effective mass of an electron in the oxide and on the barrier height, which allow us to determine m_{ox}^* and ϕ_B for a sample with a given thickness.

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Schrödinger-Poisson solver for half-open MOS structures

E. Nadimi, E. Nakhmedov, and C. Radehaus
TU Chemnitz
Faculty of Electrical Engineering, Chair Opto- and Solid State Electronics

1. Introduction

Since the dimensions of Metal- Oxide-Semiconductor (MOS) transistors are shrunken, quantum mechanical effects play a growing role in device operations and performance. The thickness of the gate insulator layers reaches up to 2 nm in modern state of the art devices. The size scaling of oxide layer leads to a dramatically rise of the gate leakage current, which produces a large amount of heat in the devices. Therefore, deeper theoretical investigation of the leakage current, to suggest preventive measures how to reduce it, become very important.

Suggestion of quantum corrections to the classical characteristics in the framework of classical models is one of the widely used method. The effective potential (EP) approach [1-3] and the density gradient (DG) [4-5] approach which are based on the Bohmian interpretation of quantum mechanic are the most important models in this category. Although the quantum corrections improve the classical data, these approaches are not able to model and to predict all quantum mechanical effects. Modern studies of the leakage current in ultrathin oxides are focused on pure quantum mechanical modelling of field- effect devices.

In a fully quantum mechanical continous material model the Schrödinger and Poisson equations are solved self consistently. The Schrödinger equation is solved within the effective mass approximation. The boundary condition of the Schrödinger and Poisson equations are also an important issue. In many activities the Schrödinger equation has been solved in a quantum box with closed boundaries, containing only the semiconductor substrate [6-8], or the semiconductor substrate and the gate insulator [9-12], or even the whole device [13].

In this work we present results of our self-consistent computation of quantum- particle distribution in a MOS with closed boundaries in the inversion regime. Using closed boundary condition one obtains quantum mechanical bound-states in the inversion layer.

By improving this model, we have solved the Schrödinger equation with one open boundary condition to understand the effect of open boundarys and the mechanism of crossover from bound states into a quasi bound states.

2. Self-consistent solution with closed boundary condition

In the effective mass approximation, the one- electron wave function is given by the product of Bloch functions in x, y directions parallel to the $Si-SiO_2$ interface with an envelope function in z-direction perpendicular to the interface, which is the solution of the following one dimensional Schrödinger equation:

$$-\frac{\hbar^2}{2m_j^*}\Delta\Psi_j(z)+V(z)\Psi_j(z)=E_j\Psi_j(z), \quad (1)$$

where $\Psi_j(z)$ and E_j are the envelope function and the energy eigenvalue of the jth sub-band; m_j^* is the effective mass in z-direction and $V(z)$ is the potential energy. The above equation is solved in a closed quantum box under the following boundary conditions:

$$\Psi_j(0)=0 \quad \text{and} \quad \Psi_j(L)=0. \quad (2)$$

Using the Fermi- Dirac statistic and summing up over all x, y direction quantum states, the electron distribution can be expressed by the following equation:

$$n_s(z)=\sum_j \frac{n_{vj}m_{dj}^* k_B T}{\pi\hbar^2}\left|\Psi_j(z)\right|^2 \ln\left[1+\exp(\frac{E_F-E_j}{k_B T})\right] \quad (3)$$

where E_F is the Fermi energy, n_{vj} is the valley degeneracy and m_{dj}^* is the density of states effective mass per valley. The potential $V(z)$ is obtained as a solution of the Poisson equation

$$\frac{d^2V(z)}{dz^2}=\frac{e\rho(z)}{\varepsilon_0\varepsilon_s} \quad (4)$$

under the following boundary conditions:

$$V(0)=0\,,\ \frac{dV}{dz}|_{z=L}=0$$

To find the eigenfunctions and eigenenergies of a particle, the Schrödinger equation (1) has to be solved self-consistently with Eq.(4).

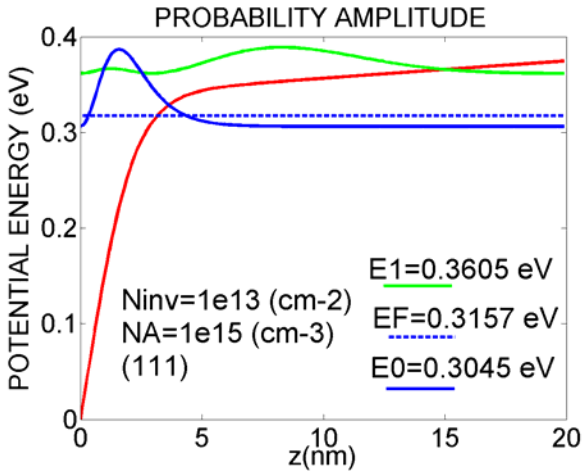

Fig.1. *The probability amplitude for the first two sub-bands at the inversion layer of a p-type semiconductor.*

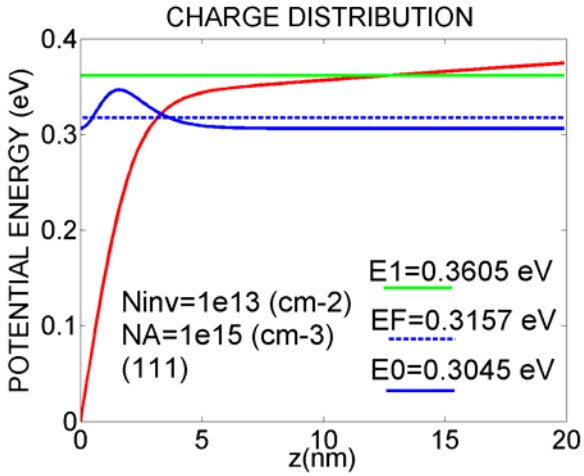

Fig. 2. *Charge distribution and the contribution of two first sub-bands to the electron density at the inversion layer.*

Figs. 1 and 2 show the bound-states, wave functions and charge distribution of the first two sub-bands at the inversion layer for a p-type semiconductor.

As it is shown in Fig. 2 the main contribution of the electron density comes from the first sub-band and the contribution of the higher sub-bands are nearly zero. Fig. 3 shows the total electron distribution at inversion layer. The average distance of the charge distribution is shifted about 2 nm from the interface. The quantum charge- distribution
strongly differs from the classical distribution, where the maximum of charge distribution is placed at the Si/SiO_2 interface.

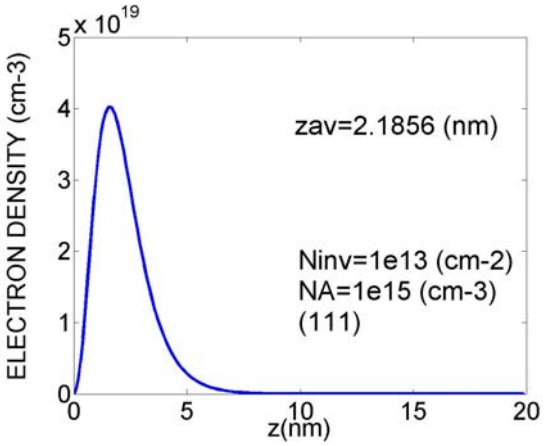

Fig. 3. *Total electron distribution at the inversion layer for a p-type semiconductor.*

3. Open boundary and the quasi bound-states

Bound character of electronic states near the Si/SiO_2 interface, formed due to the band bending, means that there is no leakage from such states and, therefore there is no tunnelling current from inversion layer into the gate. This is an acceptable assumption, if the oxide layer is thick enough ($t_{ox} > 4\,nm$). Unfortunately this assumption is not reasonable for MOSFETs with ultra-thin oxide layers.

Simulation of devices with extremely thin oxide layers require to solve the Schrödinger equation using open boundary condition. As soon as the boundary is opened the bound-states change into quasi bound-states. An electron can never leave a bound state. In other words, the life time of electron in a bound-state is infinite. But electrons in quasi bound-states can leave the state by tunnelling through the barrier; therefore they have a finite life time. In order to characterize quasi bound-states we need to define the eigenenergy and the wave function of a quasi- bound state, like for a bound-state, but also the life time for this state.

Big effort has been done to indirectly calculate the life time of a quasi bound-state in inversion and accumulation layer of MOS structure, using the transfer Hamiltonian approach [10], transverse resonant method [11] and Breit-Wigner theory of nuclear decay [12].

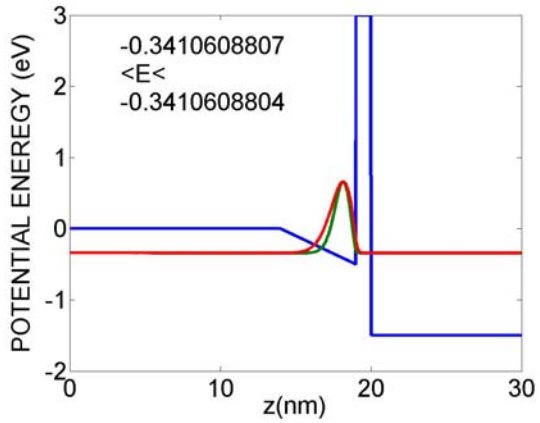

Fig. 4. *The first quasi bound state in a potential well with a 3 eV high and 1 nm thick barrier.* $\Delta E = 3\times10^{-10}(eV)$. *Red and green colour curves correspond to the wave function and the probability amplitude, respectively.*

We calculate the life time directly from the solution of Schrödinger equation with open boundary. We integrate the Schrödinger equation, providing a zero boundary condition in the deep bulk of the Si substrate, and letting the other boundary to be open. Instead of the closed boundary at the oxide side we force the wave function to satisfy the following conditions:

(i)Absolute value of the wave function at the $Si-SiO_2$ interface has to be larger than that in the interface of SiO_2/polysilicon gate;

(ii) the wave function can not change sign in the oxide layer, and the derivative of the probability amplitude can not be positive in the oxide.

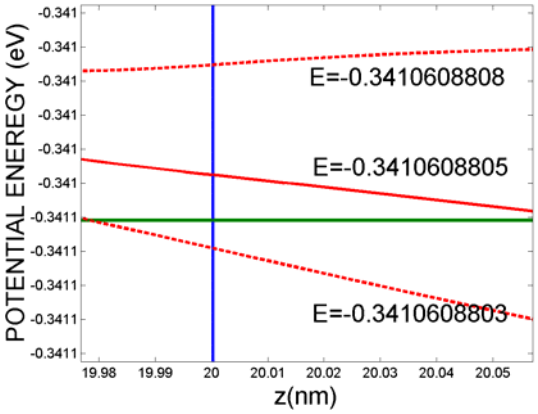

Fig. 5. *a closer shot of the figure 4 at the oxide-gate interface. The dotted wave functions fail to satisfy the conditions of an acceptable wave function.*

Under these conditions we find, that the possible energy states are placed in a close vicinity ΔE of the bound state, obtained under closed boundaries. This ΔE depends on the barrier height and thickness. Figs. 4 and 5 show the first eigenvalue with $\Delta E = 3\times10^{-10}\,eV$. Changing the barrier height from 3 eV to $2\,eV$, ΔE changes from $3\times10^{-10}\,eV$ to $1\times10^{-8}\,eV$. Shift in the thickness of the barrier from 1 nm to $0.7\,nm$, changes ΔE from $1\times10^{-8}\,eV$ to $1\times10^{-7}\,eV$.

The life time of an electron in the quasi- bound state can be calculated by using the Heisenberg uncertainty relation $\Delta t\times\Delta E = \hbar/2$. ΔE increases with decreasing the barrier height or thickness, which consequently decreases Δt leading to high leakage current.

4. Conclusion

As the oxide layers in MOS transistors becomes ultrathin the bound-state approximation is not a reasonable approximation. The states should be characterized as quasi bound-states by solving the Schrödinger equation with open boundaries.

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Deposition and characterization of amorphous hydrogenated diamond-like carbon films (a-C:H)

Klaus Schirmer, Josef Lutz
TU Chemnitz, Fakultät für ET/IT, Professur Leistungselektronik und elektromagnetische Verträglichkeit

1 Introduction

State of the art passivation layers (SiO_2 and its modifications) are reaching their limits at high voltage and high electric fields. DLC (diamond-like carbon) has suitable mechanical and chemical properties. Because of the high density of states in the band gap, mirror charges can be created, which avoid high electrical field peaks, and which are able to compensate disturbing interface charges. This results in high breakdown voltage and excellent long term stability and reliability [1].

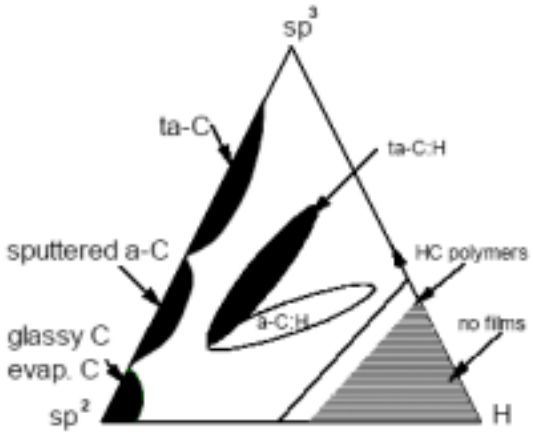

Fig. 1. Phase diagram showing composition of a-C:H, ta-C and ta-C:H [3]

2 Diamond-like carbon

Carbon forms a great variety of crystalline and disordered structures because it is able to exist in three different hybridisations, sp^3, sp^2 und sp^1 [2]. In diamond carbon's four valence electrons are each assigned to a tetrahedrally directed sp^3-orbital. The sp^2 configuration characterizes a graphitic structure. DLC is a metastable form of amorphous carbon containing a significant fraction of sp^3 bonds. The term a-C:H as an abbreviation for amorphous, hydrogenated carbon describes a system which covers a wide range of properities depending on deposition parameters. A rough classification of a-C:H films is given by the fractions of hybridisation type and hydrogen contend. Hydrogen rich films with a hydrogen contend of 40% or more , commonly deposited with low ion energies, are often so called polymerlike a-C:H films, whereas dense, sp^3 rich a-C:H films with a hydrogen fraction lower than 30% are called diamond-like carbon (DLC). This notation should not mislead. There is no 3D network of tetrahedrally bonded sp^3 carbon incorporated in these films but an amorphous network of graphitic clusters interconnected by sp^3bonds.

	sp^3 (%)	H (%)	Density (g cm^{-3})	Band Gap (eV)	Hardness (GPa)
Diamond	100	0	3.515	5.5	100
Graphite	0	0	2.267	0	
C_{60}		0		1.6	
Glassy C	0	0	1.3-1.55	0.01	3
Evaporated C	0	0	1.9	0.4-0.7	3
Sputtered C	5	0	2.2	0.5	
ta-C	80-88	0	3.1	2.5	80
a-C:H hard	40	30-40	1.6-2.2	1.1-1.7	10-20
a-C:H soft	60	40-50	1.2-1.6	1.7-4	<10
ta-C:H	70	30	2.4	2.0-2.5	50
Polyethylene	100	67	0.92	6	0.01

Table 1: Comparison of properties of amorphous carbon with reference materials diamond, graphite, C_{60} and polyethylene

3. Deposition

It is possible to produce DLCs with various deposition methods such as mass selected ion beam deposition (MSIB), sputtering of a graphite electrode by Ar plasma, filtered cathodic vacuum arc (FCVA) or plasma enhanced chemical vapour deposition (PECVD).
At the TU-Chemnitz DLC films will be deposited with a Roth&Rau MicroSys 500 PECVD system. It consists in a adjustable parallel plate arrangement within a chamber of 500 mm in diameter, a water cooled substrate electrode for deposition dimensions up to 300 mm in diameter, a 5 kW rf generator and a gas supply system for 4 gas lines. To control the plasma energy the generator runs either on fixed rf power or on fixed dc bias voltage. The system is suitable for deposition and for structuring of DLC-films. The DLC etching process development has been scope of former investigations.
Different forms of the PECVD technique constitute the main methods for depositing hydrogenated DLC films. Any hydrocarbon with sufficient vapour pressure can in principle be used as source material for the PECVD of DLC films. Among these are acetylene, benzene, butane, cyclohexane, ethane, ethylene, hexane, isopropane, methane, pentane, propane and propylene.

4 Characterization

A variety of techniques have been used to estimate sp^3/sp^2 ratio. Transmission electron microscopy (TEM) is suitable to investigate the interface between substrate and a-C:H. Fig. 2 shows a TEM picture of the Si/DLC interface.
The material properties of amorphous hydrogenated carbon films deposited by plasma chemical vapor deposition from seven different saturated and unsaturated hydrocarbon source gases were investigated in [4]. It was shown that the precursor gas substantially influences the film properties. The unsaturated hydrocarbons acetylene and ethylene lead to films with higher density, lower hydrogen content, and higher refractive index than saturated hydrocarbons. This holds for low and high ion energies.
Fig. 3 shows the influence of different hydrocarbons to the optical transmission of DLC film. Deposition has been performed at the same pressure, gas flux and self bias voltage. To retain self bias at 750 V, only 73 % of the rf generator power level was necessary for acetylene compared to methane. The methane (CH_4) based film shows a slightly darker surface than acetylene (C_2H_2) based, this can be explained by its more graphitic like film composition. Acetylene's deposition rate was five times as much as the one of methane due to acetylene's two carbon atoms and due to less sputter effect of the Ar carrier gas.

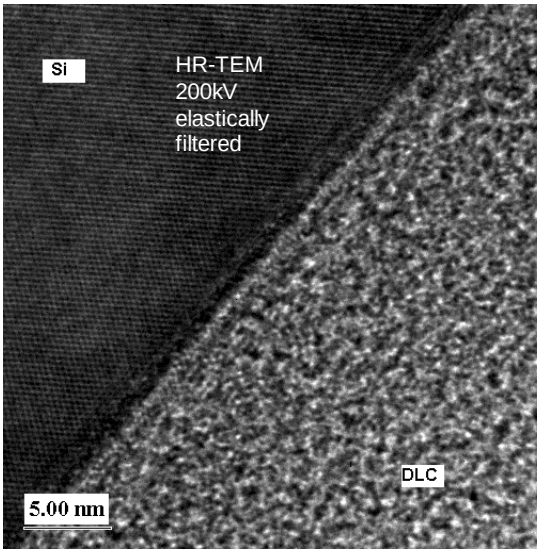

Fig 2: TEM-Picture of the interface Si/DLC

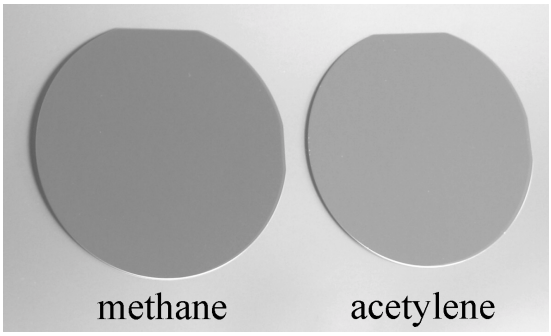

Fig. 3. Influence of hydrocarbons

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Results of Active Power Cycling with High Temperature Swing

R. Amro[1], J. Lutz[1], A. Lindemann[2]
[1]TU Chemnitz, Fakultät für ET/IT, Professur Leistungselektronik und elektromagnetische Verträglichkeit
[2] Otto-von-Guericke-Universität, Magdeburg

1 Introduction

The environmental conditions of power devices, especially with respect to the maximum specified temperature, are getting harsher. In automotive applications e.g. some parts of the electronic will move under the hood where the modules are subjected to an environmental temperature higher than 100 °C. The automotive standard AEC-Q101 stipulates that power components must withstand 5000 power cycles at temperature swings higher than 100K. To fulfil the requirements in reliability the demand for module lifetime prediction of given packaging concepts at high temperature increases.

2 Investigated Packaging Technologies

In the transfer molded, DCB based technology the power semiconductor chips are soldered onto a DCB ceramic substrate together with a lead frame with up to five pins. Subsequently chips and DCB are covered by molding compound. Figure 1a shows the cross section of a DCB based transfer molded package.

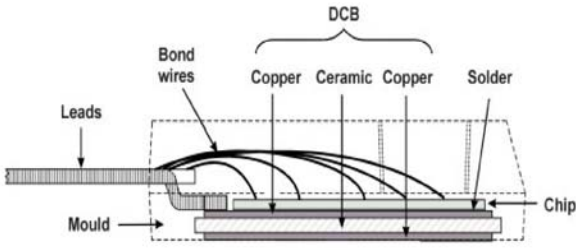

Fig.1a: cross section of transfer molded DCB based component

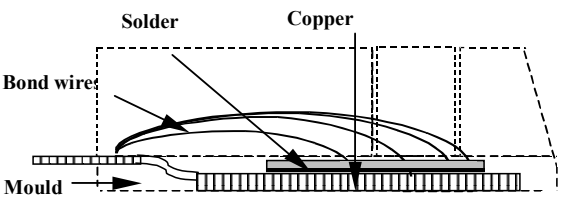

Fig.1b: cross section of transfer molded copper based component

In the transfer molded copper based technology the top side of the power semiconductor chip is wire bonded while the bottom side is soldered on copper lead frame. The package is typically moulded plastic to fix the leads for external electric connections (Fig.1b). However, the reliability of this technology is restricted by mismatch of thermal expansions coefficients of silicon chip and copper lead frame.

3 Test Results

3.1 DCB based, transfer molded diodes

Three power cycling tests with ΔT_j=105K (PC1), ΔT_j=130K(PC2), ΔT_j=155K(PC3) were performed. The minimal junction temperature ($T_{j,min}$) was 40 °C. Failure criteria, which decide that a device has reached its end-of-life, were:

- An increase of the forward voltage V_F at 50A and room temperature of 20% with respect to the initial value.
- An increase the thermal resistance between junction and heat sink ($R_{thj\text{-}h}$) of 20% with respect to the initial value, or
- Leakage current I_R exceeds 1mA.

The executed tests and achieved results are published in details in [1]. Figure 2a shows a photograph of a component of PC1 taken with the electron microscope after test stop. One can observe the trace of a completely lifted of wire and the heel cracking of the adjacent wires.

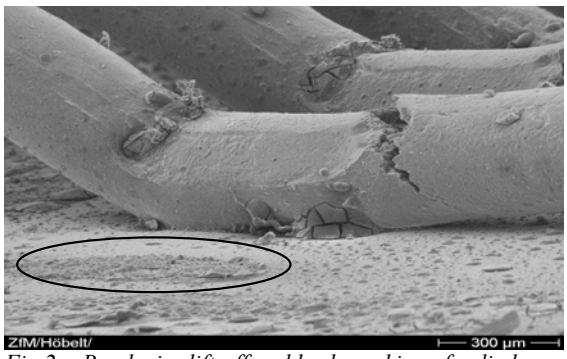

Fig.2a: Bond wire lift-off and heel cracking of a diode power cycled at ΔT_j=105 K

In PC2 (ΔT_j=130K) the majority of the tested diodes shows no significant increase of V_F, however a clear increase of T_j was obvious. Exceeding the maximum allowed increase of the thermal resistance from junction to heat sink ($R_{th,j-h}$) was the dominant failure mode. However, analysis of the diodes after test has shown that bond wires of some diodes have aged too. The failure mechanisms of bond wires and the solder fatigue seem to occur at virtually the same time.
Diodes power cycled in PC3 (ΔT_j=155K) showed a similar thermal and electrical behaviour to the diodes in PC2. However, increase of thermal resistance by solder fatigue could be clearly identified as the main failure mechanism in this test.

3.2 Copper based, transfer molded diodes.

A group of six diodes have been power cycled at ΔT_j =110K. After ca. 3800 cycles, investigations of the failure parameters have shown that two diodes exhibit no blocking capability. The crack of the chip observed in the analysis of a failed diode after test (Figure 3) clarifies this effect.
Till ca. 22000 power cycles, no further failures were registered and test was stopped because no reasonable accurate failure forecast is possible with the achieved failure data.

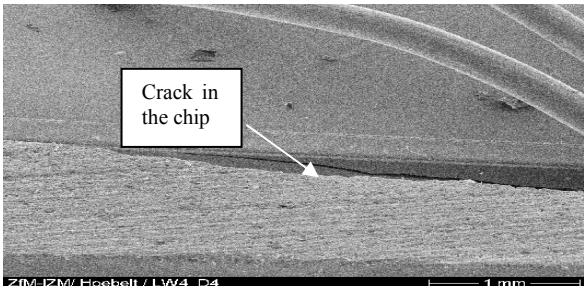

Fig.3: Chip crack of copper based, transfer molded diode power cycled at ΔT_j=110K

4 Evaluation of Results

The following diagram presents a comparison between the results achieved in the test of the DCB based components at end-of-life failure probability for 50% from the Weibull analysis (solid line) and an extrapolation of the results achieved during the evaluation of standard modules with base plate in the LESIT programme [2] with the fit given in [3] (broken line). All test results are compared for test condition $T_{j,min}$=const=40°C.

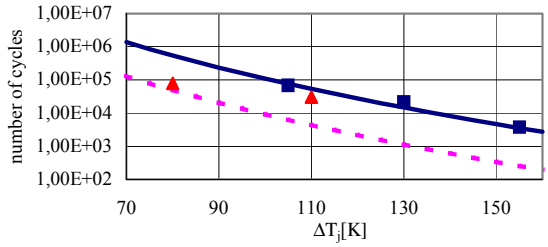

Fig.4: Comparison between transfer molded DCB based components, and extrapolated LESIT results

The DCB based transfer molded components show a clearly increased power cycling capability compared to the extrapolation of the results for standard modules.
Mechanical stress originating from mismatch of thermal expansion coefficients of silicon and copper lead frame can be identified as failure cause in the test of copper based, transfer molded devices.

5 Conclusion

The DCB based transfer molded devices show at high temperature swings a higher power cycling capability than standard modules with base plate. They promise to fulfil the automobile standard AEC-Q101 at ΔT_j>130 K Regarding the analysis of the components after test, supported by the end-of-life failure mode of PC2 and PC3, one can assume that the compound material decelerates the bond wire lift off. This clarifies the high power cycling capability of this assembly technology.
The result of testing copper based, transfer molded diodes led to the assumption that this packaging technology is unsuited for applications with temperature swings in the range of 110K, if chips large chips, e.g. with area of 63 mm^2 or more, are used.

ACKNOLEDGEMENT: IXYS Semiconductors AG is acknowledged for providing the DCB based transfer molded devices.

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Using of High-end Design Tools in Education

Kay Hammer, Steffen Heinz, Hendrik Zeun, Gunter Ebest
Chemnitz University of Technology, Faculty of Electrical Engineering and Information Technology,
Chair Electronic Devices

1 Introduction

Analogue circuits are essential components of integrated circuits. Nowadays, most integrated circuits are prepared in CMOS technology. Advantages of CMOS circuits are lower power loss and favourable manufacturing costs according to bipolar circuits. For this reason, the later introduced practical training is based on a CMOS process.
Simultaneous to the growing scale of integration a lot of new applications are opened. At the same time, the desire for short development times and savings in sophisticated test circuits is growing. For integrated analogue circuits the selection of an appropriate production process is very important also. Statements about the efficiency of a designed circuit are only possible with the help of prototypes produced in the same process scheduled for serial production.
The design of these circuits is performed with the help of design tools like MENTOR and CADENCE. For students, who are working as an integrated circuit designer later, it is important to understand the context between theoretical knowledge of circuit design, production process and the influence of specific layouts. The knowledge about working with a design software is means for the purpose only.

2 Integrated Analogue Design Flow

During a design flow, many decisions influence characteristics of the design. One aim of the practical training is the understanding of these coherences. Fig. 1 shows a typical design flow for integrated circuits. In the practical training, students are responsible for all design steps.
The first task in the integrated circuit design is a draft of the circuit (design specification). Hereby, function and performance of the circuit are defined. After this step, the calculated transistor dimensions and the chosen design process form the design specifications. These include restrictions like the allowed power loss, the supply voltages and other technology parameters.

Afterwards, the draft has to be feed into the design tool as a netlist (schematic entry). In general, netlists are created with the help of the design tool through a graphical editor. The resulting netlist is used in the next step of the design flow. With a first simulation of the circuit, the properties and functionality of the designed circuit can be confirmed. Dependent on the circuit, different simulators for analogue, digital or mixed signal applications are available. After the first simulation, one can change some circuit parameters like transistor dimensions to improve the circuit parameters. Understanding and testing the circuit with suitable test circuits is an important part of the practical training too.

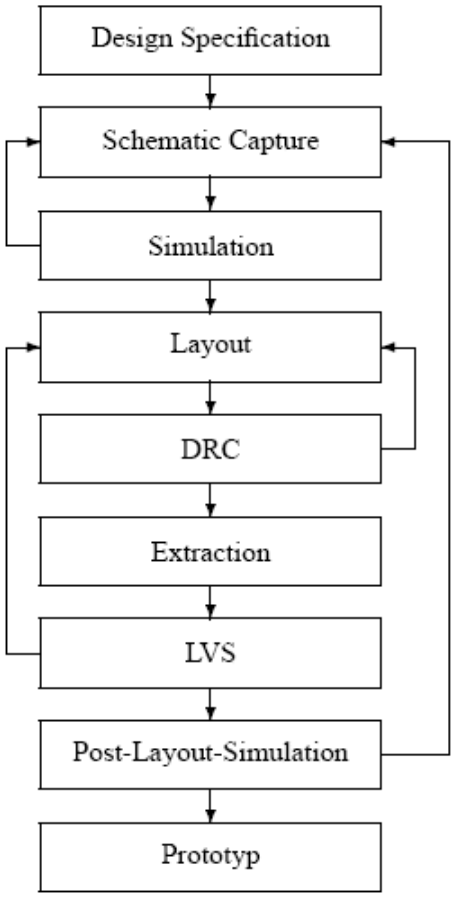

Fig. 1: Integrated Circuit Design Flow

Using a layout editor, one feeds the positions and dimensions of each circuit element into the design tool. For integrated analogue circuits, the

layout, determining the circuit's efficiency, is a very important step during the design flow.
The layouts of circuits have to fulfil many restrictions. Their number depends on the process. The design rule checker (DRC) checks the layout whether the rules are fulfilled or not. If there are any rule violations, they are listed.
Afterwards, one has to compare the layout with the netlist of the schematic capture. For this reason, the design tool extracts a netlist from the layout. Additional information about parasitic elements like parasitic capacities is extracted also.
Now, the layout versus schematic checker (LVS) checks whether the two netlists represent the same circuit or not. Anyway, this tool allows no statement about the performance of the circuit.
Afterwards, the electrical characteristics of the layout are simulated during the post layout simulation. Because of the more detailed netlist with included parasitic elements, the results of this simulation allow a good prediction about the real circuit. Restrictions in the performance of the simulator are the used non ideal models.
After a satisfying simulation result, the designed circuit can be produced as a prototype.

3 High end design tools in a practical training

Nowadays, it is very important for students to be trained with the same design tools used in industry. For a prospective employee as an analogue designer, the relation between layout and performance of a circuit has to be trained. For this reason, an early practical training with a high-end design tool like CADENCE is advisable.
During the practical training, the students have to be responsible for the complete design flow. It is important to demand and support an autonomous work of the student. A possible task is the design an operational amplifier with a specific performance. The demands for a good slew rate or a rail to rail output stage are possible optimising criteria.
The first step will be the design specification. Beginning with a simple two stage amplifier, students have to get into the operation of the design tool.
During the design flow, students will improve the first circuit to fulfil the given requirements. By adding a nulling resistor and an AB output stage like shown in Fig. 2, the simulation results will improve (Fig. 3). It is important that the students have the ability to try things out on their own to get a sense how to get the best design results.

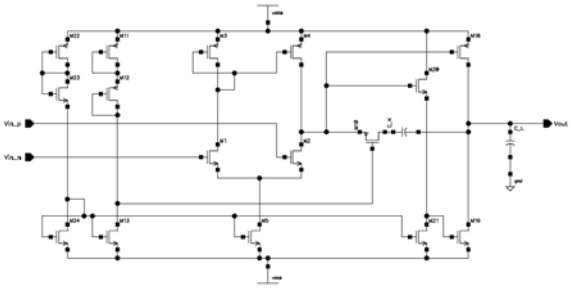

Fig. 2: Two Stage Amplifier with AB Output Stage

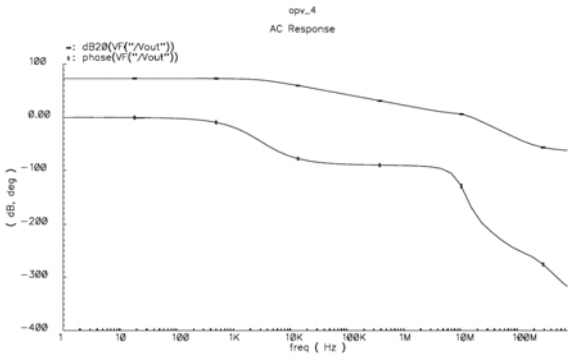

Fig. 3: AC Response of the Circuit from Fig. 2

The most important part of the practical training should be the layout. For good results, the students need an experienced instructor and a good knowledge about mask layout. The practical training can help to understand the effects of reducing serial resistance of the circuit elements, the importance of dummy elements and the design of protective circuits.

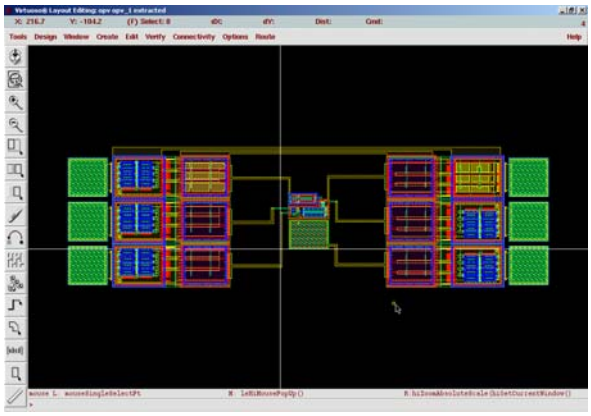

Fig. 4: Complete Layout with Protection Circuits

After the complete design flow, including many iteration steps to get the best design results, the students have designed their first own circuits (Fig. 4). A post layout simulation now gives a

good prediction of the performance of the designed circuit.
Now, the possible production of a prototype enlarges the possibilities of a practical training. The students have already designed test circuits to prove the performance of their designs. With real hardware, the students can compare simulation results with measurement results.

4 Conclusion

A practical training with a design tool like CADENCE is very attractive for students. Beside the necessary licence for the design software, it is important to have an up-to-date design kit (high performance interface tool kit) from a semiconductor manufacturer. The higher expenditure in preparation and realisation the practical training results in a better understanding of analogue circuit design by students.

5 References

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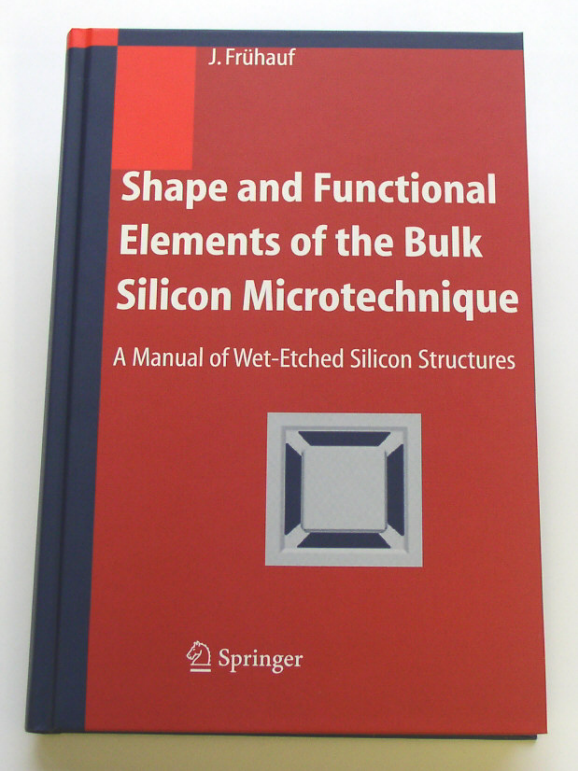
Shape and Functional Elements of the Bulk Silicon Microtechnique

Frühauf, Joachim; Gärtner, Eva; Krönert, Steffi
TU Chemnitz, Fakultät für Elektrotechnik und Informationstechnik,
Fachgruppe Werkstoffe

As a result of activities and experiences for many years in the field of wet chemical etching of silicon a systematic compilation of etched microelements is given. The possibility for writing the manual with the title "Shape and Functional Elements of the Bulk Silicon Microtechnique" was enabled by the Stiftung Industrieforschung, Germany. This includes an extensive literature research in different papers and the design and fabrication of new microstructures.
The methodic manual presents a survey of the shape related and functional elements of the bulk silicon microtechnique. It gives a systematic description of simple shape elements and of elements for mechanical, optical and fluidical applications. It includes practical instructions for the use of the relevant techniques and an extensive collection of examples for the support of the search for applications via photographs, drawings and references. It serves as a valuable guide to the design of etch masks and processes while summarizing the important properties of silicon.

After an introduction the 2nd chapter summarizes the technological basis of the bulk silicon microtechnique. Chapter 3 deals with the basics of orientation dependent etching of silicon. In chapter 5 the simple shape elements are described including one- and two step etch processes. The content of chapter 6 are the elements for a mechanical application among them spring elements, levers and bearings. Chapter 7 contains the elements for fluidic application including channels, elbows, branchings, caverns and nozzles. The optical elements mentioned in chapter 8 are fibre grooves, micro mirrors, beam splitters and gratings. The book is finished with a summary of the properties of silicon compared with other materials.
The manual is aimed at producers of sensors and microtechnical components as well as producers of components of precision engineering and optical applications.



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5 Cooperations with industry and universities

Partnerships with the following institutes and companies were continued and / or established in 2004:

- Advanced Micro Devices (AMD), Sunnyvale & Austin, USA and Dresden, Germany
- Aktiv Sensor GmbH, Stahnsdorf, Germany
- Alpha Microelectronics GmbH, Frankfurt (Oder), Germany
- AMTEC GmbH, Chemnitz, Germany
- Applied Materials, Santa Clara, USA and Dresden, Germany
- Atmel Design Center, Dresden, Germany
- BASF AG, Ludwigshafen, Germany
- BMW AG München, Germany
- Robert Bosch GmbH, Reutlingen & Stuttgart, Germany
- CAD-FEM GmbH Grafing, Germany
- CiS Institut für Mikrosensorik gGmbH, Erfurt, Germany
- Colour Control Farbmeßtechnik GmbH, Chemnitz, Germany
- DaimlerCrysler Research Lab Ulm, Germany
- Danfoss Silicon Power, Schleswig, Germany
- Digital Instruments – Veeco Instruments, Mannheim, Germany
- DILAS Diodenlaser GmbH
- Endress und Hauser Conducta GmbH & Co. KG, Germany
- Eupec GmbH Warstein, Germany
- FACRI , Research Institute, Xi´an, China
- Fahrzeugelektrik Pirna GmbH, Pirna, Germany
- FHR Anlagenbau GmbH, Ottendorf-Okrilla, Germany
- First Sensor Technology GmbH, Berlin, Germany
- FLEXIVA automation & robotics, Amtsberg, Germany
- Forschungszentrum Rossendorf, Germany
- Fujitsu Microelectronic GmbH, Dreieich-Buchschlag, Germany
- GEMAC mbH Chemnitz, Germany
- GF Messtechnik Teltow, Germany
- Gesellschaft für Prozeßrechnerprogrammierung mbH (GPP) Chemnitz, Germany
- GHF IWM Halle
- Heinrich-Hertz-Institut Berlin, Germany
- Hitachi Ltd., Japan
- Institut für Festkörper- und Werkstoffforschung e.V. IFW Dresden, Germany
- IMEC, Leuven, Belgium
- Infineon Technologies AG, Munich and Dresden, Germany
- InfraTec GmbH, Dresden
- ITIM International Training Center for Material Science, Vietnam
- IXYS Semiconductor GmbH, Lampertheim, Germany
- Jenoptik-LDT GmbH, Gera , Germany
- Kyocera Fineceramics GmbH
- L.A.A.S-C.N.R.S Toulouse, Prof. Dr. D. Esteve, France
- LETI, Grenoble, France
- LG Thermo Technologies GmbH
- Lionix, Enschede, Netherlands
- LITEF GmbH, Freiburg, Germany
- Massachusetts Institute of Technology, Cambridge / Boston, Mass., USA
- Max-Planck-Institut (MPI) für Mikrostrukturphysik Halle, Germany

- Mechanical Engineering Laboratory AIST, MITI, Dr. Mitsuro Hattori and Chisato Tsutsumi, Tsukuba, Ibaraki, Japan
- memsfab GmbH, Chemnitz, Germany
- Merck KGaA, Darmstadt, Germany
- Mesa Research Institute, Prof. J. Fluitman, Twente, The Netherlands
- Microtech GmbH, Gefell, Germany
- Mitsui Engineering and Shipbuilding Co. Ltd., Japan
- Motorola, Phoenix, Arizona ,USA / Munich, Germany
- Nex Systems, Wilmington, MA. , USA and Berlin, Germany
- NICO Pyrotechnik, Trittau, Germany
- OEC GmbH, Germany
- PANALYTIK GmbH, Dresden, Germany
- Physikalisch-Technische Bundesanstalt Braunschweig (PTB), Germany
- PLASMACO Inc. Highland, New York, USA
- Raytek GmbH Berlin, Germany
- Rohm and Haas Electronic Materials, Marlborough, USA
- Roth & Rau Oberflächentechnik GmbH, Wüstenbrand, Germany
- RWE Schott Solar GmbH, Alzenau, Germany
- Schott Mainz & Schott Glas Landshut, Germany
- Seiko Epson, Japan
- Sentech Instruments GmbH, Berlin, Germany
- SICK AG, Waldkirch & Ottendorf-Okrilla, Germany
- SF Automotive GmbH, Freiberg, Germany
- Siegert TFT GmbH, Hermsdorf, Germany
- Siemens A&D ATS2 Nürnberg und AT Regensburg, Germany
- Institut für Solarenergieforschung Hameln-Emmerthal, Germany
- Solid State Measurements, Pittsburgh, PA., USA
- ST Microelectronics, Crolles, France
- Suss Microtec AG Vaihingen, Munich and Sacka, Germany
- Dr. Teschauer AG, Chemnitz, Germany
- Thales-Avionics, Valence and Orsay, France
- Trikon Technologies, UK
- TRW Airbag Systems GmbH & Co. KG, Aschau/Inn, Germany
- X-Fab Gesellschaft zur Fertigung von Wafern mbH, Erfurt, Germany
- Yole Developpement, Lyon, France
- ZMD Dresden, Germany
- 3D-Micromac AG, Chemnitz, Germany

Universities:

- Johannes Kepler Universität Linz, Austria
- Atominstitut Universität Wien, Austria
- Chongqing University, Chongqing, China
- Fudan University, Shanghai, China
- TSINGHUA University, Beijing, China
- Xiamen University, Xiamen, China
- University of West Bohemia, Pilsen , Czech Republic
- Technische Universität Braunschweig, Germany
- Universität Bremen, Germany
- HTW Mittweida, Laserapplikationszentrum, Germany
- TU Dresden, Germany
- Universität Erlangen, Germany
- Universität Essen, Institut für anorganische Chemie, Germany

- Universität Hannover, Germany
- Westsächsische Hochschule Zwickau (FH), Zwickau, Germany
- TU Budapest, Hungary
- University of Tokyo, Res. Ctr. for Adv. Science & Technology (RCAST), Japan
- University of Delft, Netherlands
- University of Twente – MESA, Netherlands
- Warsaw University of Technology (WUT), Warsaw, Poland
- Nowosibirsk State University, Russia
- Technological University Singapore, Singapore
- Royal Institute of Technology, Stockholm, Sweden
- University of Hertfordshire, UK
- State University of New York at Binghamton, USA
- Portland State University, Portland, Oregon, USA
- Rensselaer Polytechnic Institute (RPI), Troy, N.Y., USA
- University of Nevada, Reno, USA
- University of California at Berkeley, Berkeley Sensor and Actuator Center, USA
- Case Western Reserve University, Cleveland, Ohio, USA
- University of Colorado at Boulder, USA
- University of Delaware, Newark, USA
- Hanoi University of Technology, Vietnam

6 Equipment and service offer

The ZfM facilities include 1000m² of clean rooms (about 30% of them class 10 to 100). Modern equipments were installed for processing of 100 mm and 150 mm wafers as well as design and testing laboratories providing the basis for the following processes, partly in cooperation with the Fraunhofer Institute IZM, branchlab Chemnitz:

- Design (Workstations)
- Mask fabrication 3" ... 7" / Electron beam lithography / Proximity and contact double-side lithography
- High temperature processes: Diffusion / Thermal oxidation / Annealing / RTP
- Etching (dry: Plasma- and RIE-mode & wet: isotropic / anisotropic)
  (Alcatel MCM, SECON XPL 251, STS Multiplex ICP-ASE, Metal Etch DPS Centura)
- Chemical vapor deposition MOCVD (Precision 5000 [Cu, WN, TiN])
- Chemical vapor deposition PECVD (Precision 5000 [SiO_2, Si_3N_4, CF-Polymer, SiCH, SiCOH, SiCNH])
- Physical vapor deposition PVD (MRC 643, FHR 150x4, CLC 9000, ...)
- Chemical mechanical polishing CMP
- Wafer bonding: silicon direct, anodic, eutectic, glass frit
- Testing (SEM, AFM, electrical, mechanical …)

The ZfM provides the following services :

R & D

(e.g. Si processes, technology, development of sensors and actuators, metallization)

- Thermal oxidation of silicon wafers
- PVD (Cr, Au, TiN, Cu , Pt, Al, W, TiW, $AlSi_x$,CrNi, Pyrex)
- CVD: PECVD / LPCVD (600° C ... 900° C)
  (SiO_2 , Si_3N_4 , Polysilicon, $Si_xO_yN_z$, Cu-MOCVD, TiN-MOCVD, SiCOH, SiCH)
- PECVD (diamond-like Carbon films, a-C:H)
- Dry etching (Si, SiO_2 , Si_3N_4 , Polysilicon, Silicides, Al, Cu, refr. metals, TiN, Cr, DLC)
- Wet etching (SiO_2 , Si_3N_4 , Si, Polysilicon, Al, Cr, Au, Pt, Cu, Ti, W)

- Wafer lithography / Electron beam lithography / Mask fabrication (3“ ...7“ Cr mask)
- Design & simulation (technology, process....)
  Software: ANSYS, SIMODE, PHOENICS, SIMBAD, EVOLVE ,
  Etch mask design tool EMADE
- Parametric testing: Waferprober, HP Testsystem

and in **analytical fields** such as

- Scanning electron microscopy SEM / EDX
- Atomic force microscopy AFM (D 3000)
- Ellipsometry / Nanospec
- Laser profilometry (UBM, TENCOR FLX-2900)
- Surface profilometer (TENCOR alpha step 200, Dektak 3)
- US-Microscope
- Zug-/Druckprüfmaschine Zwick 4660 universal
- Perkin-Elmer DMA 7e dynamic mechanical analyser
- Micromechanical testing instrument (Sartorius and PI)
- Lifetime scanner SEMILAB WT-85

In cooperation with the Fraunhofer Institute IZM, branchlab Chemnitz:

- STS „Multiplex ICP“ etch tool for deep silicon etching
- Wafer bonding (silicon fusion bonding, anodic bonding, eutectic bonding, Seal-glass-bonding, adhesive bonding)
- CMP MIRRA & ONTREK-cleaner (Copper, Silicon, SiO_2)
- Test measurements for MEMS

7 Education

7.1 Lectures

Electronic Devices and Circuits
Elektronische Bauelemente und Schaltungen
Lecturer: Prof. Dr. G. Ebest

Electrical Engineering / Electronics
Elektronik
Lecturer: Prof. Dr. C. Radehaus

Design Technology and Production Engineering
Konstruktions- und Fertigungstechnik
Lecturer: Prof. Dr. W. Dötzel

Materials Science in Electrical Engineering
Werkstoffe der Elektrotechnik / Elektronik
Lecturer: Prof. J. Frühauf

Fundamentals of Electronic
Grundlagen der Elektronik
Lecturer: Prof. Dr. G. Ebest

Electronic Devices
Elektronische Bauelemente
Lecturer: Prof. Dr. G. Ebest

Optoelectronics
Optoelektronik
Lecturer: Prof. Dr. C. Radehaus

Semiconductor Device Technology
Technologien der Mikroelektronik
Lecturer: Prof. Dr. T. Gessner

Solid State Electronics and Photonics
Festkörperelektronik und - photonik
Lecturer: Prof. Dr. C. Radehaus

Electrophysics
Elektrophysik
Lecturers: Prof. Dr. C. Radehaus

Fundamentals, Analysis and Design of Integrated Circuits
Integrierte Schaltungstechnik
Lecturer: Prof. Dr. G. Ebest

Physical and Electrical Design
Physikalischer und elektrischer Entwurf
Lecturer: Prof. Dr. G. Ebest

Analog Integrated Circuit Design
Analoge integrierte Schaltungstechnik
Lecturer: Prof. Dr. G. Ebest

Microtechnologies / Materials and Technologies of Microsystems and Devices
Mikrotechnologien / Werkstoffe und Technologien der Mikrosystem- und Gerätetechnik
Lecturers: Prof. J. Frühauf, Prof. Dr. T. Gessner

Basics and Application of Solar Power Engineering
Grundlagen und Anwendung der solaren Energietechnik
Lecturers: Prof. Dr. G. Ebest, Prof. Dr. W. Hiller, Prof. Dr. U. Rindelhardt

Optocommunication
Optokommunikation
Lecturer: Prof. Dr. C. Radehaus

Electrooptics
Elektrooptische Bilderzeugung
Lecturer: Prof. Dr. C. Radehaus

Device Technology
Gerätekonstruktion
Lecturer: Prof. Dr. W. Dötzel

Microsystems
Mikrosystemtechnik
Lecturer: Prof. Dr. W. Dötzel

Reliability and Quality Assurance
Technische Zuverlässigkeit / Qualitätssicherung
Lecturer: Prof. Dr. W. Dötzel

Control Engineering (Microsystem Technology)
***Prüftechnik* (*Mikrosystemtechnik*)**
Lecturers: Dr. J. Markert, Dr. S. Kurth

Technical Optics
Technische Optik
Lecturer: Dr. B. Küttner

Computer Aided Design
CAD
Lecturer: Dr. J. Mehner

Semiconductor Measurement Techniques
Halbleitermeßtechnik
Lecturers: Prof. Dr. C. Radehaus, Prof. Dr. M. Hietschold

Electrical Drives
Elektrische Antriebe / Gerätetechnische Antriebe
Lecturers: Prof. Dr. W. Hofmann, Dr. R. Kiehnscherf

Integrated Circuit Design
Schaltkreisentwurf
Lecturer: Prof. Dr. D. Müller

System Design
Systementwurf
Lecturer: Prof. Dr. D. Müller

EDA-Tools
EDA-Tools
Lecturer: Prof. Dr. D. Müller

Rapid Prototyping
Rapid Prototyping
Lecturer: Prof. Dr. D. Müller

Components and Architectures
Components and Architectures
Lecturer: Prof. Dr. D. Müller

Design and Calculation of Power Electronic Systems
Entwurf und Berechnung leistungselektronischer Systeme
Lecturer: Prof. Dr. J. Lutz

Industrial Electronics
Industrielle Elektronik
Lecturer: Prof. Dr. J. Lutz

Power Electronics
Leistungselektronik
Lecturer: Prof. Dr. J. Lutz

Semiconductor Devices in Power Electronics
Bauelemente der Leistungselektronik
Lecturer: Prof. Dr. J. Lutz

Process and Equipment simulation
Prozesssimulation / Equipmentmodellierung
Lecturers: Prof. Dr. T. Gessner, Dr. R. Streiter

7.2 Student exchange programmes

SOCRATES / ERASMUS

I.S.M.R.A. – Ecole Nationale Supérieure d`Ingénieurs Caen, France
Technical University of Cluj-Napoca, Romania
Katholieke Universiteit Leuven / IMEC, Belgium
Danmarks Tekniske Universitet, Lyngby, Denmark
Ecole des Mines de Nancy, Nancy, France
University of Oulu, Finland
Universite de Rennes I, France
Technical University of Lodz, Poland
Royal Institute of Technology Stockholm, Sweden
University of West Bohemia, Pilsen , Czech Republic

IAS/ ISAP Programme (DAAD)

University of Delaware, Newark, USA
University of Nevada, Reno, USA
Portland State University, Portland, USA

DAAD

University of Hanoi, Vietnam

7.3 Project reports/ Diploma theses / PhD

Project reports

Ahner, N.:	Entwicklung und Optimierung einer Technologie zur Herstellung dünner Kobaltsilizidschichten für neuartige Substratmaterialien der Hochfrequenztechnik
Bonitz, J.:	Untersuchungen zur Kompatibilität von dünnen TiN-Diffusionsbarrieren und porösen low-k-Materialien
Bonitz, J.:	Abscheidung ternärer TiSiN-Barriereschichten
Carstens, J.:	Zuverlässigkeitsuntersuchungen an Neigungssensoren nach DIN 60068-2-27
Gebauer, S.:	Ansteuerelektronik für einen Vakuumsensor unter Nutzung eines Digitalen Signalprozessors
Hammer, K.:	Integrierter analoger Schaltungsentwurf mit CADENCE
Herrmann, M.:	Untersuchungen zur hermetischen Kapselung von Beschleunigungssensoren in Volumentechnologie

Herrmann, M.:	Messtechnische Charakterisierung von Drehratensensoren in BDRIE Technologie
Hillert, A.:	Erstellung eines Praktikumsversuches „Simulation CMOS-Differenz-verstärker“
Jandt, U.:	Erstellung einer Software zur Spektrometereffizienzbewertung
Koch, T.:	Voruntersuchungen zur Realisierung einer Messeinrichtung zur scannenden Detektion von Wärmestrahlung an Oberflächen mittels Mikrospiegel
Leidich, S.:	RF-Phase Shifter in Bulk Micro Mechanic Technology
Leistner, T.:	Untersuchungen zum Dämpfungsverhalten mikromechanischer Vibrationssensoren
Meichsner, G.:	Charakterisierung von chemisch und galvanisch abgeschiedenen Goldschichten auf Glas und Silizium
Richter, G.:	Laserprojektion mit resonanten Scannern
Srihari Prakash:	Fabry-Perot-Filter with improved performance
Stürmer, M.:	Evaluierung von Beugungsgittern hinsichtlich deren Einsatzes in Miniaturspektrometern
Voigt, S.:	Einsatz von variablen MEMS-Kapazitäten in der Hochfrequenztechnik

Diploma works

Grumann, R.:	Optimierung eines 100µm – DRIE-Prozesses für die Anwendung in hochgenauen MEMS-Kreiseln Advisors: Dr. K. Hiller, DI U. Breng, LITEF GmbH
Günther, M.:	Entwicklung eines Verfahrens zum Fügen von Halbleitersubstraten mittels Epoxid- und Polyimid-Klebstoffen Advisors: Dr. M. Wiemer, DI J. Frömel
Hensel, R.:	RF-MEMS: Wirtschaftlich-technische Bewertung der Marktchancen, des F&E-Potenzials sowie der Realisierbarkeit auf Basis der Silizium-Technologie Advisors: Prof. Käschel, Dr. A. Bertz
Homilius, J.	Prozessetablierung spin-on-low k Dielektrika und Schichtcharakterisierung Advisors: Dr. S. Frühauf, Dr. S. E. Schulz
Kuschel, B.:	Entwicklung eines Messplatzes zur isothermalen Kennlinienaufnahme von Bauelementen Advisor: DI Korndörfer
Lahner, F.:	Konzeption, Entwicklung, Aufbau und Test eines Kommunikationskanals für ein autarkes Mikrosystem Advisor: DI Dienel
Lorenz, A.:	Realisierung von MSM Dioden in AlGaN / GaN für sonnenblinde UV Sensoren Advisors: Prof. Gessner, Dr. John (IMEC Leuven / Belgien)
Rank, H.:	Entwicklung eines Drucksensor-Katheters für klinische Untersuchungen Advisor: Dr. Billep
Sachse, H.:	Erarbeitung, Realisierung und Testung einer Bedienoberfläche für einen Gasmessplatz mittels Visual Basic unter Windows NT Advisors: DI R. Hoffmann, Dr. C. Kaufmann
Schneider, J.:	Entwicklung eines feldtauglichen inertialen Messsystems zur Anwendung in biometrischen Analysen Advisors: Dr. Billep, DI Seibt Fa. ErgoVitaGmbH & Co. KG
Sodan, L.:	Messtechnische Charakterisierung mikromechanischer Schrittschaltwerke Advisor: DI Schröter
Stahl, Ch.:	Kapzitätsberechnung mittels Boundary Element Methoden Advisor: Dr. J. Mehner

Sternberger, A.:	Ansteuerung eines durchstimmbaren Infrarot-Filters mit digitalem Signalprozessor Advisors: Prof. W. Dötzel, Dr. S. Kurth
Strobel, J.:	Lasernevillier mit 2D-Mikrospiegel Advisor: Dr. J. Markert
Tenholte, D.:	Einsatz eines Mikroresonators für ein Reibungsvakuummeter Advisors: Prof. W. Dötzel, Dr. S. Kurth
Uhle, J.:	Entwurf eines RF-Systems mit birektionalem Datenaustausch Advisor: DI Zeun
Völkel, U.:	Optische Lithografie vs. Direct Write – Eine technische und ökonomische Evaluation Advisors: Dr. A. Bertz & AMTC Dresden
Wächtler, T.:	Bewertung neuartiger metallorganischer Precursoren für die chemische Gasphasenabscheidung von Kupfer für Metallisierungssysteme der Mikroelektronik Advisor: Dr. S. E. Schulz

PhD / Habilitation

Dr.-Ing. habil. Karla Hiller
„Technologieentwicklung für kapazitive Sensoren mit bewegten Komponenten“, Habilitation
TU Chemnitz, Fakultät ET/IT, January 20, 2004

Dr.-Ing. habil. Nam-Trung Nguyen
„Entwurf, Herstellung und Charakterisierung von polymeren mikrofluidischen Systemen“,
Habilitation, TU Chemnitz, Fakultät ET/IT, June 21, 2004

Dr.-Ing. habil. Göran Herrmann
“ASICs: Entwurf und Applikation mikroelektronischer Systeme”, Habilitation
TU Chemnitz, Fakultät ET/IT, July 7, 2004

Dr.-Ing. Uwe Weiß
„Einsatz neuer Materialsysteme für Niedrig-Energie Anzündelemente in Airbagsystemen“
TU Chemnitz, Fakultät Maschinenbau, July 20, 2004

Dr.-Ing. Knut Gottfried
“Metallisierungssysteme für temperaturbelastete Bauelemente der Mikrosystemtechnik”
TU Chemnitz, Fakultät ET/IT, September 6, 2004

Dr.-Ing. Stephan Buschnakowski
„Alternatives Antriebs- und Auswerteverfahren für die Mikrosystemtechnik“
TU Chemnitz, Fakultät ET/IT, October 8, 2004

8 Colloquia / Workshops at the Institute

January 8, 2004
Dr. Heinz Mitlehner, SiCED
SiC - auf dem Weg zu neuartigen hochsperrenden Bauelementen

February 26, 2004
DI Sven Zimmermann, TU Chemnitz
„Derzeitiger Stand der Mikroelektroniktechnologie gemessen an der AMC 2003“

April 22, 2004
Prof. Dr. Cornelia Zanger, TU Chemnitz
"Marketing für technische Innovationen"

May 6, 2004
Dr. Franz-Josef Niedernostheide, Infineon Technologies
Siliziumbauelemente sehr hoher Leistung

May 10, 2004
Prof. James Morris, Department of Electr. & Computer Engn., Portland State University, Portland USA
„Nanoparticles for Nanoelectronics"

June 2, 2004
Dr. Egbert Vetter, Infineon technologies , Dresden
„Entwicklungstendenzen in der Mikroelektronik“

Prof. Ekkehard Meusel, Dr. J. Uhlemann, TU Dresden
„Prüfverfahren, Prüftechniken und Prüfaufwand zum Nachweis der Bioverträglichkeit in der Aufbau- und Verbindungstechnik“

June 22, 2004
Thomas Werner, AMD Saxony, Dresden
„Anwendung von Cu Verdrahtungstechnologien bei der Herstellung von Mikroprozessoren“

July 13, 2004
Dr. Claus Ascheron, SpringerVerlag
"Elektronisches Publizieren"

August 10, 2004
Colloquium “Centre of Competence for Micro- & Nanosystems”: 5 Years Fraunhofer IZM, Dept. Micro Devices and Equipment, Chemnitz

Prof. K.-J. Matthes	Rector of TU Chemnitz
Prof. K. M. Einhäupl	President of “Scientific Advisory Board of the Federal Republic of Germany” “Excellence at Universities”
Prof. W. Dötzel	Vice President for Research of TU Chemnitz “Microsystems and Microelectronics”
Prof. H. Reichl	Director Fraunhofer IZM, Berlin “Competence of Branchlab Chemnitz”
Dr. M. Rößler	SMWK Dresden
Dr. P. Seifert	Lord mayor of Chemnitz
Meng Shuguang	Ambassador of China, Berlin
Dipl.-Phys. W.Hentsch	FHR Anlagenbau GmbH, Ottendorf-Okrilla „Microsystem Technology“
Dr. E. Vetter	Vice President „Unit Process Development“, Infineon Dresden “Chemnitz Support for Microelectronics“

November 29, 2004
Dipl.-Ing. Erik Markert & Dipl.-Ing. Michael Schlegel
„Modellierung heterogener Systeme“

November 30, 2004
Dr. Eberhard Waffenschmidt, Philips GmbH
Systemintegration passiver Komponenten der Leistungselektronik

9 Scientific publications 2004

Amro, R.; J.Lutz, A.Lindemann: "Evaluation of a DCB based Transfer Molded Component for Application with High Temperature Swings" PCIM Europe 2004, Nuremberg, Germany

Amro, R.; J.Lutz, A.Lindemann: "Power Cycling with High Temperature Swing of Discrete Components based on Different Technologies" Proceedings of the 35th IEEE Power Electronics Specialists Conference, S. 2593 - 2598, Aachen (2004)

Bagdahn, J.; Wiemer, M.; Bernach, M.; Petzold, M.: "Characterisation of mechanical properties of directly bonded silicon after low and high temperature annealing", 1st workshop on wafer bonding for MEMS technologies, 10th to 12th October 2004, Halle, Germany

Baum, M.: Optical devices and biomedical application, A*Star IZM Workshop, Singapore, 8.11.04

Belsky, P.; Streiter, R.; Wolf, H.; Gessner, T.: „Application of Molecular Dynamics to the Simulation of IPVD", presented at AMC 2004, San Diego, USA, Oct. 19-21, 2004

Blaschta,F.; Schulze,K.; Schulz,S.; Gessner,T.: SiO_2 aerogel ultra low k dielectric patterning using different hard mask concepts and stripping processes. Microelectronic Eng., 76 (2004) pp 8-15

Bonitz, J.; Schulz, S.E.; Gessner, T.: Ultra thin CVD TiN layers as diffusion barrier films on porous low-k materials, Microelectronic Eng. 76, (2004)1-4, pp 82-88

Diefenbach, K.-H.; Erler, K.; Mrwa, A.; Denissov, S.; Ebest, G.; Rindelhardt, U.: Emitter Formation at RIE textured Surfaces, 10th PVSEC, Paris, June 7-11, 2004

Ecke, R.; Schulz; S.E.; Hecker, M.[1]; Engelmann, H.-J.[2]; Gessner, T.: *W*(Si)N Diffusion Barriers for Cu Metallization deposited by PECVD, Advanced Metallization Conference AMC 2004, San Diego, USA, Oct. 19-21, 2004.
[1] Institute for Solid State and Materials Research, 01069 Dresden, Germany
[2] AMD Saxony LLC &Co KG, 01330 Dresden, Germany

Frömel,J.; Billep,D.; Wiemer,M.: Application of micromechanical resonant structures for measuring the sealing of bonded sensor systems. Workshop on Wafer Bonding for MEMS Technologies, 10th to 12th October 2004, FhG-IWM Halle, Germany

Frühauf, J.; Krönert, S.: Linear Silicon Gratings with Different Profiles: Trapezoidal, Triangular, Rectangular, Arched. Proc. Of the XI. International Colloquium on Surfaces, Chemnitz, Germany 2.-3. February 2004, Proceedings Part II 75-83, Shaker-Verlag Aachen 2004

Frühauf, J.; Krönert, S.; Brand, U.; Krüger-Sehm, R.: Reachable precision of silicon dimensional standards. Proceedings of the EUSPEN, p. 217, Glasgow 2004

Frühauf, J.; Gärtner, E.; Brand, U.; Doering, L.: Silicon springs for the calibration of the force of hardness testing instruments and tactile profilometers. Proceedings of the EUSPEN, p. 362, Glasgow 2004

Frühauf, J.: Ätzmasken-Entwurf und Simulation des kristallorientierungsabhängigen Silizium-Ätzens. Tagungsband 10. GMM-Workshop Methoden und Werkzeuge zum Entwurf von Mikrosystemen (Herausg. B. Falter; W. John), Cottbus 2004, S. 19-23

Frühauf,S.; Schulz,S.E.; Gessner,T.: Integrationspotential mesoporöser SiO2-Schichten als ultra-low-k Dielektrikum. Vakuum in Forschung und Praxis, 16 (2004) pp. 194-198

Geiger, W., Breng, U., Deppe-Reibold, O., Fuchs, W., Gutmann, W., Hafen, M., Handrich, E., Huber, M., Kunz, J., Leinfelder, P., Newzella, A., Ohmberger, R., Ruf, M., Schröder, W., Spahlinger, G., Rasch A. LITEF GmbH, Freiburg ; Hiller, K., Billep, D. Chemnitz University of Technology: Test Results of the Micromechanical Coriolis Rate Sensor µCORS II, DGON 2004 Symposium Gyro Technology, Stuttgart 2004

Gessner, T.: "Advanced Silicon Micromachining Technologies", MEMS Workshop, Industrial Technology Research Institute ITRI, March 1, 2004, Taiwan

Gessner, T.: "MEMS Metallization", Invited Talk, MRS Spring Meeting 2004, April 12-16, San Francisco, USA

Gessner, T.; Schulz, S.E.: "Selected Challenges for Advanced Interconnect Systems", Invited Talk, E-MRS 2004, May 24-28, Strasbourg, France

Gessner, T.; Hiller, K.; Hübler, A.; Kurth, S.: „Micro Scanners for Spectrum Analysis Systems", Invited Talk, Actuator 2004, June 14, Bremen, Germany

Gessner, T.: "Microsystems Technologies", Leipziger Messe Z 2004, 23.Juni 04, Leipzig, Germany

Gessner, T.: „Copper Metallization systems and low k dielectrics", Joint Workshop on Materials for Advanced Interconnects, Fudan University Shanghai, July 13-14, 2004, Shanghai, China

Gessner, T.: "Mikroelektronik- und Mikrosystemtechnik-Forschung am Zentrum für Mikrotechnologien der Technischen Universität Chemnitz in Kooperation mit dem Fraunhofer IZM", Kolloquium am ZMN Ilmenau, 30. Juli 2004, Ilmenau, Germany

Gessner, T.: "Microelectronics and MEMS: Challenges for the Technology Transfer into the Industry within the Fraunhofer Organization", MINAPIM 2004, September 15-18, Manaus, Amazonas, Brazil

Gessner, T.: "The Scientific System in Germany – Universities, Max-Planck-Institutes, Fraunhofer Organization, Leibniz-Foundation and Helmholtz-Foundation", Workshop at Chongqing University, October 12, 2004, Chongqing, China

Gessner, T.; Otto, T.; Wiemer, M.; Frömel, J.: Wafer Bonding in Micro Mechanics and Microelectronics – An Overview, pp. 307-313, Anniversary book for Prof. Dr. H. Reichl´s 60th birthday, ed. B. Michel & R. Aschenbrenner, 2004

Gessner, T.: "Technology Approaches for Inertial Sensors", Invited Talk, ISINTIT 2004, October 15-16, 2004, Nanjing, China

Gessner, T.: „Mikrosysteme im Automobil", Chemnitzer Automobiltagung, TU Chemnitz, Oct. 21, 2004, Chemnitz, Germany

Gessner, T.: „ Systems Integration – A Challenge for Micro- and Nanotechnologies", Kolloquium „caesarianum", October 26, 2004, Stiftung caesar, Bonn, Germany

Gessner, T.: Challenges and trends for advanced interconnect systems – contribution and experiences of TU Chemnitz / ZfM and FhG-IZM Chemnitz, AMD-Silicon Saxony, Dresden, November 3, 2004

Gessner, T.: „Microelectronics and MEMS: Overview about FhG-IZM and the Fraunhofer Organization", A*Star IZM Workshop, IME Singapore, 8.11.04

Gessner, T., Bertz, A.; Lohmann, C.; Wiemer, M.; Kurth, St.; Hiller, K.:
„Advanced Silicon Micromachining Technologies", Suss MEMS Seminar ; Institute of Microsystem and Information Technology, Chinese Academy of Science, Shanghai, China, November 12, 2004

Gessner, T.; Hiller, K.; Bertz, A.: MEMS for automotive applications, Nanofair 2004, VDI-Berichte 1839, pp. 77-82

Hammer,K.; Heinz,S.; Zeun,H.; Ebest,G.: Using of High-end Design Tools in Education. Proceedings Conference Applied Electronics 2004, Pilsen (Tschechien), 2004 Sep 8-9 pp 64-67

Hanf, M., Dötzel, W.: Characterization of charges in MEMS devices, Actuator 2004, Bremen, Germany, pp. 498-501

Hanf, M., Kurth, S., Billep, D., Hahn, R., Faust, W., Heinz, S., Dötzel, W., Gessner, T.: A Dynamically Driven Micro Mirror Array as Light Modulator in a Hadamard Transform Spectrometer (HTS), Eurosensors XVIII, Roma, Italy, 09/2004,

Hanf, M., Dötzel, W.: „Micromechanical electrostatic field sensor for the detection of surface charges“, Proc. of the EUROSENSORS XVII, pp.374-375, Guimaraes, Portugal 2004, Sensors and Actuators 10/2004

Hanf, M., Markert, J., Dötzel, W.: „Measurement and evaluation of surface of micro mechanical mirror structures“, XI. Internationales Colloquium on Surfaces, 2. & 3. Febr. 2004 Chemnitz

Herrmann, G.; Müller, D.: ASIC – Entwurf und Test. Fachbuchverlag Leipzig,Carl Hanser Verlag, Januar 2004

Herrmann, G.; Dost, G.: Entwurf und Technologie von Mikroprozessoren. in: Beierlein, T.; Hagenbruch, O. (Hrsg.): Taschenbuch Mikroprozessortechnik. Fachbuchverlag Leipzig im Carl Hanser Verlag München Wien, Mai 2004

Himcinschi,C.; Friedrich,M.; Frühauf,S.; Schulz,S.E.; Gessner,T.; Zahn,D.R.T.: Contributions to the static dielectric constant of low-k xerogel films derived from ellipsometry and IR spectroscopy. Thin Solid Films, 455-456 (2004) pp 433-437

Jerinic, V.; Müller, D.: Safe integration of parameterized IP. in: Integration, the VLSI journal, 37 (2004), ELSEVIER B. V., pp. 193-221

Jia, Ch.; Wiemer, M.; Gessner, T.: “Low temperature direct bonding with on wafer metal interconnections“ , 1st workshop on wafer bonding for MEMS technologies, 10th to 12th October 2004, Halle, Germany

Knechtel, R.; Wiemer, M.; Knaup, M.; Bagdahn, J.: „An non-destructive test structure for bond strength evaluation in silicon-glass bonds“, 1st workshop on wafer bonding for MEMS technologies, 10th to 12th October 2004, Halle, Germany

Knechtel, R.; Wiemer, M.; Frömel, J.: “Wafer level encapsulation of microsystems using glass frit bonding“, 1st workshop on wafer bonding for MEMS technologies, 10th to 12th October 2004, Halle, Germany

Körner, H.[1]; Büyüktas, K.[1]; Eisener, B.[1]; Liebmann, R.[1]; Schulz, S.E.; Seidel, U.[1]; Gessner, T.: Impact of Ultra Low k dielectrics on RF-Performance of Inductors, Talk at the Advanced Metallization Conference AMC 2004, San Diego, USA, Oct. 19-21, 2004.
[1] Infineon Technologies AG, Otto-Hahn-Ring 6, 81739 Munich, Germany

Kretzschmar, C.; Siegmund, R.; Müller, D.: Adaptive Bus Line Grouping for Power Efficient Data Transfer over Wide System Buses. GI/ITG/GMM Workshop: Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Kaiserslautern (D), 23.-25. Februar 2004

Kretzschmar, C.; Nieuwland, A. K.; Müller, D.: Why Transition Coding for Power Minimization of on-Chip Buses does not work. Design Automation and Test in Europe (DATE), Paris (France), 16.-20. Februar 2004

Kretzschmar, C.; Bitterlich, T.; Müller, D.: A High-Level DSM Bus Model for Accurate Exploration of Transmission Behaviour and Power Estimation of Global System Buses. Integrated Circuit and System Design, Power and Timing Modeling, Optimization and Simulation,14th International Workshop, PATMOS, Santorini (Greece), 15.-17. September 2004

Kretzschmar, C.; Scheithauer, M.; Müller, D.: Adaptive Bus Encoding Schemes for Power-efficient Data Transfer in DSM Environments. IFIP Working Conference on Distributed and Parallel Embedded Systems (DIPES), Toulouse (France), 23.-26. August 2004, Kluwer Academic Publishers, Boston, USA

Krüger-Sehm, R.; Häßler-Grohne, W.; Frühauf, J.: Traceable calibration standard for the lateral axis of contact stylus instruments. Wear, Vol. 257 Nr. 12 (2004), pp.1241-1245

Kurth, S.: Meßtechnische Parameterbestimmung an MEMS-Baulementen, Materialsweek 2004, München, 21-23.Sept. 2004

Kurth, S.: Test, Charakterisierung und Zuverlässigkeit mikromechanischer Komponenten, MEMUNITY Workshop, Waldbronn, März 2004

Leidich, S.; S. Voigt, S. Kurth, B. Rawat, Gessner, T.: Microwave Phase Shifter in Bulk Micro Mechanic Technology, Proc. of Int. Conference Applied Electronics 2004, Plzen

Lohmann, C.; Gottfried, K.; Bertz, A.; Reuter, D.; Hiller, K.; Kuhn, M.; Gessner, T.: MEMS Metallization. Materials, Technology and Reliability for Advanced Interconnects and low-k Dielectrics, 2004 (Eds. R.J.Carter, C.S.Hau-Riege, G.M.Kloster, T.-M. Lu, S.E.Schulz), MRS Symp. Proc. 812 (2004), pp 233-242

Lohmann, C.; Reuter, D.; Bertz, A.; Gessner, T.: High Aspect Ratio Micromachining using the AIM Technology, Anniversary book for Prof. Dr. H. Reichl´s 60th birthday, pp. 544-548, ed. B. Michel & R. Aschenbrenner, 2004

Markert, E.; Schlegel, M.; Herrmann, G.; Müller, D.: Beschreibung von mechatronischen Systemen mit SystemC-AMS. 10. GMM-Workshop „Methoden und Werkzeuge für den Entwurf von Mikrosystemen“, Cottbus, 20.-22. Oktober 2004, p. 59 ff.

Mehner, J.: MEMS design, simulation and modelling,, A*Star IZM Workshop, Singapore, 8.11.04

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10 Guests & special international relations

Guests from:

January 13	Prof. R. Bruch, University of Nevada, Reno
February & March	Prof. Zhuyi Wen, Chongqing University, China
February 19	Dr. Koichi Ohtaka, Takahito Uga, Ikuo Katoh, Ricoh Comp. Ltd., Japan
March 22	Mr. Natsuki Yokoyama, Hitachi Ltd., Tokyo, Japan
March 30	Valentin Kahl, ibidi GmbH, München
March 31	Mrs. Annie Roulleau, Fa. Sagem, St. Etienne , Frankreich
	Mr. Philiepe Pougnet, Johnson Controls, Cerey-Pontoise, Frankreich
May 8	Prof. R. Bruch, University of Nevada, Reno, USA
May 10	Prof. J.Morris, Portland State University, Portland, USA

May 28	Dr. Joost Grillaert (Technical Marketing Manager Europe), Martin Kranz (Account Manager Central Europe); Cabot Microelectronics
June 17&18	Dr. Masao Arakawa, Mr. Tomoo Otsuka, Mr. Yutaka Kinugasa, Matsushita Electric Works, Osaka, Japan
June 20	Prof. Zhuyi Wen, Prof. Yansun Wu, Chongqing University, China
	Doz. Dr.-Ing. Jan Mühlbacher, Dozentenaustausch, TU Pilsen, Tschechien Doz. Dr.-Ing. Vaclav Kus, Dozentenaustausch, TU Pilsen, Tschechien Doz. Dr.-Ing. Eva Kucerova, Dozentenaustausch, TU Pilsen, Tschechien
June 30	K. Sukondhasingha (Chairman of MTEC Board), C. Thanachayanont National Science & Technology Development Agency, Pathumthani, Thailand
July	Zhou Yi, Wei Fanglin, Ji Yinhu, FACRI Xián, China
July 9	Dr. Christof Krautschik, Intel Corp., Santa Clara, USA
July 9	Dr. A.R. Baker (Vice President Technology), P. van der Velden, M. Hauck; Rohm and Haas Electronic Materials
July 26 - August 2	Prof. A. Kazemzadeh, Dr. M.A. Bahrevar, Materials & Energy Research Center, Teheran, Iran
August 24	Dr. Curtis R. Carlson, President and CEO, SRI International
September	Chris Cooke, John Ziegler, Dr. Thomas Lechtenberg – Vice President, General Atomics, San Diego, USA
September 10	Mrs. H. Weber, Sumitomo Deutschland, Düsseldorf und Dr. T. Yamamoto, Asahi Kasei, Kawasaki, Japan
October 4	Mr. Min Shi, FhG Office Shanghai, China
October 27	Mr. Hernan Valenzuela, Brazilian Ministry of Development, Industry and Foreign Trade (SUFRAMA), Coordination of Institutional Relations for Technological Affairs
October	Yang Min, Li Wenhong, Han Kejian, FACRI Xián, China
November 3	Dr. J. Kade, Dr. A. Hürrich, DP M. Müller, FhG Photonische Mikrosysteme Dresden
November 11	Mr. Takahito Uga, Mr. Ikuo Katoh, Mr. Daiki Ninegishi, Ricoh, Yokohama, Japan
November	Prof. Zhuyi Wen, Prof. Yansun Wu, Chongqing University, China
December 12-17	Prof. Boris M. Sinelnikov, President of North-Caucasus State Technical University, Stavropol, Russia and Prof. Nikolay I. Kargin, Vice-President and Dr. Alieva L. Ruslanovna, Head of Internatl. Relation Dept.

and

Dietrich Mund	Schott Glas Electronic Packaging
Kunihiko Ueki	Kyocera
Dieter Stolze	Endress und Hauser GmbH+Co. KG
Holger Reinecke	Steag microparts
Bernhard Trui	Atmel Germany GmbH
Jürgen Graf	Robert Bosch GmbH

Scientific coworkers / PhD:

DI Alexej Schaporin Novosibirsk Technical University, Russia
November 2002 – December 2004
DI Wladimir Kolchuzhin Novosibirsk Technical University, Russia
November 2002 – December 2004
Shohei Hata Hitachi, PERL, Yokohama / Japan
March 2003 – February 2004
Chenping Jia University of Xian, China,
January 2003 – December 2004
Julia Yukecheva Novosibirsk Technical University, Russ. Präsidentenstipendium
August 2003 – July 2004
Junjun Wang China, FUDAN University, Shanghai
October 2003 – August 2004
Dr. Huseyn Orujov Azerbaijan Technical University, Baku, Aserbaijan
September 2004 – December 2004
Yukito Sato Ricoh Company Ltd., Japan
October 2004 – February 2005

Students:

Ebermann, Gustavo	Universidad Catolica del Peru, Lima	09/2003 – 03/2004
Leinveber, Rostislav	TU Pilsen	04/2004 - 08/2004
Kuchar, Milan	TU Pilsen	04/2004 - 08/2004
Mitas, Jan	TU Pilsen	04/2004 - 08/2004
Hendrichova, Jarmila	TU Pilsen	04/2004 - 08/2004
Stefanski, Marek	TU Lodz	10/2003 - 02/2004
Suchodolski, Marcin	TU Lodz	10/2003 - 02/2004
Stacia, Michael	TU Lodz	10/2003 - 02/2004
Greisel, Andreas	Portland State Univ., USA	06/2004 – 08/2004
Lantz, Vanessa	Portland State Univ., USA	06/2004 – 08/2004
Lotz, Josef	Portland State Univ., USA	06/2004 – 08/2004
Sankisa, Srihari	University of Nevada, Reno	08/2004 – 12/2004
Vasudeva, Vikas	University of Nevada, Reno	08/2004 – 11/2004