Annual Report 2005

Center for Microtechnologies (ZfM)

Editors:
Prof. Thomas Gessner
Dr. Wolfgang Seckel

Postal address: **Reichenhainer Str. 70**
D – 09107 Chemnitz

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1 Preface

As in preceding years, the Center for Microtechnologies in close cooperation with the "Micro Devices and Equipment" Department Chemnitz of the Fraunhofer Institute for Micro-integration and Reliability (FhG IZM) in Berlin has further consolidated its position as a Center of Excellence in the fields of microelectronics back end technologies and microsystem technologies.

The key to our success was an interdisciplinary cooperation of several chairs within the ZfM. Based on this idea, ZfM's primary mission is to provide an intellectual and working environment that makes possible student education and research in areas that require or may benefit from advanced ULSI-interconnect technologies, Si-nanotechnology and new developments and ideas in the field of MEMS by using microfabrication technologies. ZfM's technology laboratories provide a complex of modern microelectronics laboratories, clean rooms and microfabrication facilities.

It is a pleasure to announce that the cooperation of the ZfM with the Fraunhofer IZM was promoted in a new quality within the year 2005. The location Chemnitz was selected for a new institute part of the Fraunhofer IZM having sole responsibility. We plan to involve Prof. Bernd Michel (expert in Nano and Microreliability) and Prof. Arved Hübler (expert in printed electronics) as new members within the Fraunhofer IZM (Chemnitz branch of the Fraunhofer IZM). Furthermore Prof. Thomas Gessner was appointed as a Vice Director of the Fraunhofer IZM by the Fraunhofer Board in October 2005.

We are very pleased that Prof. Dr. Ulrich Heinkel was elected as a new member of the board of directors of the ZfM at the end of 2005. He has replaced Prof. Dietmar Müller, who retired 2005. We would like to thank Prof. Müller for his long term contribution within the ZfM, especially for his very successful participation in the Collaborative Research Center "Arrays of micromechanical sensors and actuators".

The international relationship to China and Japan has been intensified in the year 2005. In April 2006 we will start an International Research Training Group with the FUDAN University, Jiao Tong University (Shanghai) and the TU Berlin as well as TU Chemnitz. The Fraunhofer IZM was invited to participate in a MEMS-Workshop in Sendai (Japan) in October 2005. Prof. Esashi, Tohoku University in Sendai, will be an active consultant of the Fraunhofer IZM in the field of MEMS. Another highlight was a joint workshop entitled "MEMS for Automotive Applications" in Chongqing, organized by the Fraunhofer IZM and ZfM together with Chongqing University in June 2005.

The 2005 Annual Report of the Center for Microtechnologies provides an overview of the facilities, staff, faculty and students associated with the ZfM, as well as a description of many of the ongoing research projects which make use of the ZfM facilities.

These developments, which are based on close links with industry and cooperation with German as well as international institutes, contribute to an advanced education for our students. We kindly acknowledge the support of the Federal Ministry of Research, the German Research Foundation, the Saxon Ministry of Science and the European Commission.

As always, we are driven by our triple aims of excellence in education, scientific and technological research and by providing a comprehensive range of research and development services to industry.

I would like to thank all my colleagues, the scientific fellows and technicians for all their dedicated work.

I look forward to participating in the promising development of new devices and concepts through the use of silicon technology.

Thomas Gessner
President of the Center for Microtechnologies

The Ninth European Workshop on Materials for Advanced Metallization 2005 (MAM) Dresden March 6-9th 2005 was organised by the ZfM.

International Program Committee and 2005 co-chairs
H. Körner (Infineon),T. Marangon & J. Torres (both ST Microelectronics), T. Gessner (TU Chemnitz), S. Petersson (KTH Stockholm), K. Maex (IMEC), I. Suni (VTT Finland), R. Madar (INPG France), S. E. Schulz (TU Chemnitz)

170 scientists from 15 countries attended the 38 lectures on latest research in metallization covering both micro- and nanodimensions.

Workshop atmosphere at the poster session: Discussion of research results at 58 posters

International cooperations

Prof. Thomas Gessner on Fraunhofer – Symposium, Sendai / Japan, October 19, 2005

Prof. Thomas Gessner together with the Lord mayor of Sendai, Mr. Katsuhiko Umehara (left) and Prof. Masayoshi Esashi , Tohoku University, Sendai (right)

International Student Exchange programs (ISAP)

Prof. Reinhard Bruch (left) and Prof. James Morris (right) met the students who were studying at the University of Nevada and the Portland State University, together with Prof. Christian Radehaus, Prof. Michael Hietschold and Dr. Wolfgang Seckel.

** ISAP: Internationale Studien- und Ausbildungspartnerschaften, DAAD Bonn*

2 Organization

Center for Microtechnologies

Prof. Dr. Wolfram Dötzel
Prof. Dr. Gunter Ebest
Prof. Dr. Joachim Frühauf
Prof. Dr. Thomas Gessner
Prof. Dr. Josef Lutz
Prof. Dr. Dietmar Müller
Prof. Dr. Christian Radehaus

Our scientific research focuses on microsystem technology, microelectronics, as well as opto-electronics and integrated optics. In these fields, the Chemnitz University of Technology has had a tradition and experience for more than 30 years.
The research comprises ULSI metallization technologies, fabrication and application of micromechanical components, modeling, simulation and design of processes, devices, components, circuits and test structures down to the nanometer range, as well as single electron tunneling technologies, nonlinear photonic materials and fiber optics.
In education, the specified and related topics are taught in the basic and main courses. The institute offers the specializations Electronics/Microelectronics, Microsystem/Device Technology and Mechatronics.
The equipment is provided for the institute in combination with the Center for Microtechnologies and comprises a complete silicon wafer line, mask making equipment, commercial software and hardware for simulation and design, as well as extensive analysis and semiconductor measurement technology.
The Center for Microtechnologies facilities include 1000 m² of clean rooms (about 30 % of it class 10 to 100) with equipment for mask and wafer processes.

Visit our homepage: http://www.zfm.tu-chemnitz.de

Chair Microsystems and Precision Engineering
Professur Mikrosystem- und Gerätetechnik
Prof. Dr.-Ing. Wolfram Dötzel
phone (+49 371) 531 3264
fax (+49 371) 531 3259
e-mail: doetzel@etit.tu-chemnitz.de
www.infotech.tu-chemnitz.de/ ~microsys/index.html

Chair Electronic Devices
Professur Elektronische Bauelemente
Prof. Dr.-Ing. Gunter Ebest
phone (+49 371) 531 3125
fax (+49 371) 531 3004
e-mail: ebest@etit.tu-chemnitz.de
www.tu-chemnitz.de/etit/leb/

Chair Microtechnology
Professur Mikrotechnologie
Prof. Dr. Dr. Prof. h.c. mult. Thomas Gessner
phone (+49 371) 531 3130
fax (+49 371) 531 3131
e-mail: Thomas.Gessner@zfm.tu-chemnitz.de
www.zfm.tu-chemnitz.de

Chair Power Electronics and Electromagnetic Compatibility
Professur für Leistungselektronik und elektromagnetische Verträglichkeit
Prof. Dr.-Ing. Josef Lutz
phone (+49 371) 531 3342
fax (+49 371) 531 3327
e-mail: Josef.Lutz@etit.tu-chemnitz.de
www.tu-chemnitz.de/etit/le

Chair Circuit and System Design
Professur Schaltungs- und Systementwurf
Prof. Dr.-Ing. habil. Dietmar Müller
phone (+49 371) 531 3195
fax (+49 371) 531 3193
e-mail: mueller@infotech.tu-chemnitz.de
www.tu-chemnitz.de/etit/sse/

Chair Opto- and Solid-State Electronics
Professur Opto- und Festkörperelektronik
Prof. Dr. rer. nat. Christian Radehaus
phone (+49 371) 531 3086
fax (+49 371) 531 3004
e-mail: cvr@zfm.tu-chemnitz.de
www.tu-chemnitz.de/etit/opto/

Group for Material Science
Arbeitsgruppe „Werkstoffe der Elektrotechnik / Elektronik“
Prof. Dr. rer. nat. habil. Joachim Frühauf
phone (+49 371) 531 3178
fax (+49 371) 531 3202
e-mail: joachim.fruehauf@e-technik.tu-chemnitz.de
www.infotech.tu-chemnitz.de/~wetel/wetel-home.html

Center for Microtechnologies (Scientific Institution)
Zentrum für Mikrotechnologien (ZfM)
President: Prof. Dr. Dr. Prof. h.c. mult. Thomas Gessner
phone (+49 371) 531 3130
fax (+49 371) 531 3131
e-mail: Thomas.Gessner@zfm.tu-chemnitz.de
www.zfm.tu-chemnitz.de

3 Memberships

Prof. Wolfram Dötzel

Vice President for Research of Chemnitz University of Technology, since October 2003
Member of the Academy of Science of Saxony, Leipzig / Germany
Member of acatech (Council of Technical Sciences of the Union of German Academies of Sciences and Humanities)
Gesellschaft für Mikroelektronik und Mikrotechnik (VDI/VDE-GMM)
ESPRIT III – Network „NEXUS“

Prof. Gunter Ebest

Vertrauensdozent „Studienstiftung des Deutschen Volkes“

Prof. Thomas Gessner

Member of the Academy of Science of Saxony, Leipzig / Germany
Member of acatech (Council of Technical Sciences of the Union of German Academies of Sciences and Humanities)
Member of "Senatsausschuss Evaluierung der Wissenschaftsgemeinschaft Gottfried Wilhelm Leibnitz" (WGL)
Member of the Board of „KoWi“, Service Partner for European R&D funding, Bruessel
The Institute of Electrical and Electronics Engineers, Inc. (IEEE) , USA
The Electrochemical Society, USA
„Advisory Professor“ of FUDAN University: honorary professor, 1st June 1999
„Advisory Professor“ of Chongqing University: honorary professor, 1st July 2003
Referee of the German Science Foundation (DFG-Fachgutachter) „Systemtechnik“

Prof. Josef Lutz

International Steering Committee of the European Power Electronics and Drives Association (EPE), Brussels
Member of the Advisory Board of the Power Conversion Intelligent Motion Conference (PCIM), Nuremberg
International programme committee of the International Seminar on Power Semiconductors (ISPS), Prague

Prof. Dietmar Müller

Member of the Academy of Science of Saxony, Leipzig / Germany
Member of acatech (Council of Technical Sciences of the Union of German Academies of Sciences and Humanities)

Prof. Christian Radehaus

Optical Society of America (OSA)
The Institute of Electrical and Electronics Engineers, Inc. (IEEE), USA
The American Physical Society (APS)
Deutsche Physikalische Gesellschaft (DPG)

Fraunhofer Institute for Reliability and Microintegration IZM
Branch Lab Chemnitz
Dept. Multi Device Integration

Fraunhofer Institut Zuverlässigkeit und Mikrointegration

Director: Prof. Thomas Gessner ***Management: Dr. Thomas Otto***

Since 1998 a strong co-operation exists between the Fraunhofer Institute for Reliability and Microintegration (Fraunhofer IZM, Berlin, Munich & Chemnitz) and the Center for Microtechnologies. Accordingly the department was founded to combine the packaging know-how of the Fraunhofer IZM with the silicon MEMS devices of the Center for Microtechnologies.

The main research activities of the department MDE are focused on the following topics:

- ***Development of MEMS***: Sensors (kinetic, pressure, force, chemical) and actuators (scanner) are transferred into the system level (e.g. micro spectrometer).

- ***Development of advanced technologies*** like CMP (chemical mechanical polishing) and 3D-patterning by deep silicon etching as well as increasing the core competence in *MEMS packaging* (chip and wafer bonding including combinations of new materials and bonding at low temperatures)

- ***Process and equipment simulation****:* The goal is the improvement of deposition and etch rates, uniformity and fill behavior of vias and trenches by optimizing process conditions and reactor design.

- ***MEMS design and simulation***:
  - New reduced order modelling features of MEMS provide efficient means for data exchange from component models to circuit and system simulation environment.
  - Novel frequency selective vibration sensor arrays have been successfully integrated into a user programmable vibration measurement unit for wear state monitoring.

In near future microsystems will be quite more intelligent and multifunctional e. g. the integration of electronics for signal and information processing with sensors and actuators in silicon and nonsilicon technologies. The so called multi device integration to smaller and smarter systems is our vision. Therefore further research fields are back-end-of-line technologies for micro and nano electronics, printed electronic systems for ubiquitous low-cost applications and investigation of micro and nano reliability for smart systems.

To derive benefits from the potential of Asian markets, the Fraunhofer IZM Chemnitz established a representative office in Shanghai (PR China) in July 2002, which is managed from Chemnitz. The aim of these activities is to evaluate the microelectronics and microsystems markets in the science and economic areas in Shanghai, Chongqing, and whole China. Furthermore we would like to use this knowledge for common R & D projects and for getting in contact with industry in China.

In general the strategic alliance between the Fraunhofer Institute for Reliability and Microintegration and the Center for Microtechnologies as described ensures strong synergies in the technology and device development.

Nanotechnology Center of Excellence "Ultrathin Functional Films"

The Center of Excellence "Ultrathin Functional Films" (UFF), distinguished by the Federal Ministry of Research (BMBF) as a nation-wide center, is coordinated by Fraunhofer-IWS Dresden. It joins 51 enterprises, 10 university institutes, 22 research institutes, and 6 corporations into a common network. Nanotechnology is one of the key technologies of the 21st century. In order to channel the research results already available at institutes and universities as well as the growing demand from industry, the Nanotechnology Centers of Excellence (CE) had been established in 1998. The Center for Microtechnologies is an active member within this center, especially in the field of microelectronics related topics.

Contact: Office of Center of Excellence "Ultrathin Functional Films"
at Fraunhofer-IWS Dresden
Dr. Ralf Jaeckel
Phone +49 (0) 351 / 25 83 444, Fax +49 (0) 351 / 25 83 300

Activities within the frame of Nano-CE-UFF are subdivided into 6 Working Groups (WG), every one of which is administered and coordinated by one member:

WG 1: Advanced CMOS
WG 2: Novel components
WG 3: Biomolecular films for medical and technological purposes
WG 4: Mechanical and protective film applications
WG 5: Ultrathin films for optics and photonics
WG 6: Nano-size actorics and sensorics

The Working Groups, in which the Center for Microtechnologies is mainly involved, are described shortly in the following:

Advanced CMOS

Structural widths of about 100nm are state-of-the-art in CMOS technology. A reduction down to below 50nm within 10 years, for further miniaturization, is envisaged by the International Technology Roadmap for Semiconductors ITRS (by Semiconductor Industry Association (SIA) and SEMATECH). Along with this trend, higher frequency and reliability are required. This implies novel developments in materials and processes for both the active elements and the interconnect system, including advanced equipment for larger Si-wafer production. High k dielectrics will be applied to ensure further scaling of effective gate oxide thickness. Most present-day interconnect systems are made of contacts (e.g. titanium or cobalt silicide), barrier layers (TiN, TiW), isolating interlayers (SiO_2 and low-k dielectrics like FSG, OSG), interlayer connections and conducting paths (Al-alloys and Copper). Copper with its high conductivity and stability with respect to electromigration has been introduced as conductor material leading to higher frequency and reliability. This requires the availability of suitable barrier layers suppressing interdiffusion and reactions. The barrier layers must not affect the conductivity of the paths remarkably, which requires ultra-thin films. Interfaces and nanometer scale effects become increasingly important.

Head of the Working Group: Prof. Dr. Thomas Gessner
Chemnitz University of Technology

Novel components

The continuing trend towards miniaturization of integrated circuits has given rise to increasing efforts to supplement and gradually replace conventional CMOS-technologies by nanotechnologies and nanoelectronics in near future. The latter include magneto-electronics, and single electron devices, nanocluster storage elements, and resonant tunneling elements, among others.

Head of the Working Group: Prof. Dr. Christian Radehaus
Chemnitz University of Technology

4 Research activities of ZfM in cooperation with the FhG-IZM, Branch Lab Chemnitz

Fields of research

- Design and fabrication of microelectronic and micromechanical elements and arrays
- ULSI metallization
- High temperature stable metallization
- Analysis of micromechanical systems
- Development and application of design tools and methods for micromechanical components and systems & coupled field analysis
- Coupling of microsystems and instrumentation (mechanical, electrical, thermal and substantial interfaces)
- Function, principles and modelling of electronic devices (test structures, parameter extraction, model building)
- Microelectronic circuit design (read out- and controlling circuits for sensors and actuators)
- MIS – solar cells (manufacturing, analysis, measuring and modelling) & multicristalline solar cells
- Electronics for micro-electromechanical systems (MEMS)
- Development of infrared measurement systems
- Nanoelectronics
- Integrated Optics
- Colour measurement

Subjects of research

- Microfabricated scanner arrays
- Acceleration sensors
- Electostatically driven torsion actuators with one or two DOF
- Air gap insulated microstructures (AIM) technology
- High temperature applications of MEMS, e.g. gas sensor for exhaust measurement
- Vibration monitoring based on Si-sensor arrays
- Sensor / actuator systems for high precision scanning with a large vertical range
- Gyroscopes
- Wafer bond techniques / SOI – substrat fabrication / MEMS wafer level packaging
- Simulation of micromechanical and microelectronical components, materials databases
- Design tools for microsystems and microelectronics
- Macromodels for simulation of micromechanical components using PSpice
- Design and fabrication of integrated optical waveguides on silicon
- Fiber-optical communication systems
- Single Electron Tunnelling Technologies
- Infrared measurement and sensors
- Orientation dependent etching of silicon: Development of etchants and determination of etch rates, design of etch masks and simulation of etch process, development of new structures by multi-step etch processes
- Geometrical measurement on microstructures
- Plastic deformation of silicon-microstructures
- Copper metallization / Diffusion barriers / CMP
- Low k dielectrics / Air gap structures for ultra low-k values
- Equipment and process simulation for microelectronics
- Development of probing equipment for 1/f measurements
- Microwave Device and Circuit Design and Simulation
- Reliability analyses

4.1 Current research projects

BMBF Project "InnoRegio – InnoSachs: Joint Project – Formation of a regional network for the fabrication of silicon MEMS (MIKROFE); Part: Sensor development and fabrication"

Project leader:	Dr. T. Otto, FhG IZM Chemnitz
Partners:	GEMAC mbH Chemnitz; Turck Beierfeld GmbH
Project duration:	01. 09. 2004 - 31. 03. 2006
Project goal:	Development and integration of a *low* g sensor for a regional fabricated system

BMBF Project "Active Smart ID-Label for transportation monitoring (ASIL)"

Project leader:	Dr. F. Kriebel, KSW Microtec AG, Dresden
Partners:	KSW Microtec AG Dresden, ELMOS Semiconductor AG Dortmund, Schenker Deutschland AG Dresden, ZfM TU Chemnitz
Project duration:	01. 09. 2005 - 31. 08. 2008
Project goal:	Development, adaptation and integration of sensors for shock and tilt sensing within an active rf ID label

BMBF Project „Modular Optical Analyser System (MOPAL)"

Project manager:	Prof. T. Gessner
Partners:	Endress+Hauser Conducta GmbH & Co. KG, COLOUR CONTROL Farbmesstechnik GmbH, SENTECH GmbH, Micro System Research Center of Chongqing University (VR China)
Project duration:	01. 08. 2004 - 31. 07. 2007
Project goal:	Development and realization of an economical, efficient and universally applicable modular optical miniature analysis system for the spectral range from 300 nm – 10 µm.

BMBF Project "Visualisierung mit halbleiter-basierten RGB Lasern im Automobil- und Consumerbereich - VISULASE"

Project leader:	OSRAM Opto Semiconcuctors GmbH
Partners:	FhG IZM Chemnitz, ZfM TU Chemnitz, FhG-IOF Jena, Robert Bosch GmbH, ELOVIS GmbH
Project duration:	01. 10. 2004 - 30. 09. 2007
Project goal:	The goal of the project is the development of a complex micromechanical system for a head-up display in a car.

BMBF Project „Isolation schemes for ultra high RF-circuits" (Isosurf)

Project manager:	Dr. H. Höhnemann, Atmel Germany GmbH
Partners:	Atmel Germany GmbH, IMS chips Stuttgart, FZ ISG Jülich, FhG IZM Department Chemnitz, TU Ilmenau, TU Ulm
Project duration:	04/2003 – 04/2006
Project goal:	Fabrication of new transistor structures based on SOI-substrates with buried silicides layers

BMBF Project „Design und Technologie für SOI-CMOS Bauelemente mit Gatelängen kleiner 50nm (MOSTEDE)"

Project manager:	Prof. C. Radehaus
Partners:	AMD Saxony, HTW Dresden
Project duration:	01. 04. 2004 – 31. 03. 2007
Project goal:	Atomic scale modelling of new dielectrics for CMOS technologies

BMBF-Project : "Advanced Supercaps based on nanostructured materials (Nanocap®II)"

Project Manager:	Mr. P. Malcher, Brandenburgische Kondensatoren GmbH
Partners:	FhG ISC Würzburg, Bosch Group, BMW Group, TU Chemnitz – Prof. Lutz
Project duration:	01.09.2005 – 31.08.2008

Project goal:	Development of a new generation of supercaps with improved technical features

SMWA Project „Mikroelektronisches Zündelement für Insassen - Sicherheitssysteme“

Project manager:	Prof. T. Gessner
Partners:	Flexiva automation & Anlagenbau GmbH, Amtsberg; Fahrzeugelektrik Pirna GmbH
Project duration:	01.10. 2003 – 28.02. 2005
Project goal:	Development of a new airbag igniter

DFG Project „Polymere als low-k Dielektrika für Metallisierungssysteme in der Mikroelektronik“ – Polymers as low-k dielectrics for microelectronic metallization schemes

Project manager:	Prof. T. Gessner
Partners:	Prof. M. Bauer, BTU Cottbus
Project duration:	01.02.2002 – 31.01.2004 01.12.2004 – 30.11.2006
Project goal:	Development and characterization of organic ultra low k material with reduced density; Patterning process development and compatibility with copper interconnect processing.

DFG Project „Bestimmung und Optimierung des mechanischen Verhaltens von Schichtstapeln mit porösen low-k-Dielektrika“ – Evaluation and Optimization of mechanical behavior of film stacks containing porous low-k dielectrics

Project manager:	Prof. T. Gessner
Partners:	Prof. F. Richter, Chair Solid-State Physics, Chemnitz University of Technology
Project duration:	01.11.2004 - 31.10.2006
Project goal:	Development of fundamental models and software for mechanical characterization technique based on nanoindentation of porous low-k dielectrics. Correlation with CMP loads on porous materials.

Integrated Project (IST) “NANOCMOS”: CMOS backbone for 2010 e- Europe. From the 45 nm node down to the limits

Project leader:	ST Microelectronics SA (F)
Project manager:	Prof. T. Gessner / Dr. S. E. Schulz
Partners:	Infineon Technologies AG (D), Philips Electronics Nederland B.V. (NL), Philips Semiconductors R&D France (F), Philips Innovative Technology Solutions NV (B), IMEC Leuven (B), ST Microelectronics Srl. (I), CNRS (F), CEA-LETI Grenoble (F), Fraunhofer (D), isiltec GmbH (D), Ion Beam Services (F), Magwell (B), ACIES Europe (F)
Project duration:	01.03.2004 – 31.05.2006
Project goal:	NANOCMOS is a project integrating in a coherent structure, activities that in the past have been the object of ESPRIT/IST, JESSI/MEDEA projects in the field of CMOS technologies. It focuses on the RTD activities necessary to develop the 45nm, 32nm and below CMOS technologies. From these technology nodes it will be mandatory to introduce revolutionary changes in the materials, process modules, device and metallization architectures and all related characterization, test, modelling and simulation technologies, to keep the scaling trends viable and make all future IST applications possible. NANOCMOS covers all these aspects. The first objective of the project is the demonstration of feasibility of Front-End and Back-End process modules of the 45nm node CMOS logic technology. The project intents to process as demonstrator a very aggressive SRAM chip displaying worldwide best characteristics. The second objective of the project is to realize exploratory research on critical issues of the materials, devices, interconnect and related characterization and modelling to start preparing the 32/22 nodes considered

	to be within the limits of the CMOS technologies. The third objective of the project is to prepare the take up of results described in the Objective I and implement a 45nm Full Logic CMOS Process Integration in 300 mm wafers by the end of 2007. This integration will be part of a separate MEDEA+ project.
Website:	www.nanocmos-eu.com

SMWA Project „Modular measurement system consisting of a tunable FPI and IR sensor - MODUL“

Project manager:	Prof. T. Gessner
Partners:	InfraTec GmbH Dresden, GEMAC mbH Chemnitz
Project duration:	01.04.2003 – 31.09.2005
Project goal:	Development of layout and technology for a micromachined Fabry-Perot-Interferometer; Fabrication of prototypes

SMWA Project "Development of an IC-cluster-tool for high aspect ratio dry etching of silicon dioxide (C2T/SiO2)“

Project leader:	Dr. R. Fendler, Mr. W. Hentsch, FHR Anlagenbau GmbH
Partner:	FHR Anlagenbau GmbH
Project duration:	01. 06. 2004 - 30. 11. 2006
Project goal:	Development of process and system for deep dry etching of silicon oxide and silicon oxide based glasses.

Stiftung Industrieforschung: Project “Calibration of instruments of the hardness testing by standards produced by use of the silicon microtechnologies“

Project Manager:	Prof. J. Frühauf
Project duration:	01.10.2003 – 30.06.2005
Project goal:	Development of a silicon spring system suitable as standard for the calibration of indentation depths and forces

DFG-Project ”Hotpressing of multifunctional standards for image processing microscopes for measurements on microsystems and nanostructures" (SPP 1159/1)

Project Manager:	Prof. J. Frühauf
Partner:	Prof. E. Reithmeier, University of Hannover
Project duration:	06.09.2004 - 05.09.2006
Project goal:	Development of pressing tools made out of silicon

EU Project “Surface Enhanced Micro Optical Fluidic Systems – SEMOFS”

Project manager:	Dr. K. Hiller
Partners:	CSEM (Switzerland), CEA (France), Cardiff University (UK), Bayer (Schweiz) AG (Switzerland), Eurogentec (Belgium), CHR Citadelle (Belgium), ALMA Consulting (France)
Project duration:	01.09.2005 – 31.08.2008
Project goal:	Development of polymer based integrated probecards (including microfluidic and micro optical parts) for health diagnoses

SAB compound project GEMO, part “Silicon basic components for instruments for the measurement of mechanical surface properties in the micro-nano region“

Project Manager:	Prof. J. Frühauf
Partners:	Institut für Physik, Prof. F. Richter, TU Chemnitz ASMEC Advanced Surface Mechanics GmbH Radeberg Anfatec Instruments Oelsnitz IMA Materialforschung und Anwendungstechnik GmbH
Project duration:	01.08.2005 - 31.07.2007
Project goal:	Development of systems of springs and tips made by the silicon microtechnologies

EFRE Project „NMR-Mikroresonatoren zur Erstellung von Metabolit-Profilen hämatopoetischer Stammzellen“

Project manager:	Dr. T. Riemer, Interdisziplinäres Zentrum für Klinische Forschung Leipzig
Partners:	Zentrum für Mikrotechnologien Chemnitz, Universität Leipzig
Project duration:	01. 07. 2005 - 31. 06. 2007
Project goal:	The goal of the project is the development of a nuclear magnetic resonance detector with very high sensitivity, suitable for analyzing small amounts of biological sample material.

AIF Projekt "Entwicklung von Siliziumaktoren mit lasertrimmbaren Feder-Masse-Strukturen"

Project manager:	Prof. T. Gessner
Partners:	3D-Micromac AG
Projekt duration:	01.05.2004 - 31.10.2006
Projekt goal:	Aim of the collaboration is to investigate achievable accuracy and efficiency as well as developing new laser systems and equipment for in-line laser treatment of MEMS.

Industrial Research Contract „Development of precursors for copper deposition “

Project managers:	Prof. T. Gessner, Dr. S. E. Schulz
Partners:	BASF Ludwigshafen; Prof. Lang, TU Chemnitz , Chair Inorg. Chemistry
Projekt duration:	01.04.2003 - 31.03.2005
Project goal:	Development of precursors and deposition processes for copper.

Industrial Research Contract „Wafer level packaging for micro scanners“

Project managers:	Prof. T. Gessner
Partners:	Ricoh Company, Ltd., Japan
Projekt duration:	01.10.2004 – 30.06.2006
Project goal:	Development of a new packaging technology for micro scanners on wafer level by wafer bonding.

Industrial Research Contract „Fabrication of multi-use acceleration sensors“

Project manager:	Prof. T. Gessner
Partners:	Fara New Technologies, Xi´an, China, GEMAC mbH Chemnitz
Project goal:	Development of an high precision acceleration sensor system and its fabrication technology; Fabrication of prototypes

DFG Project „VIVA – Low Power System Bus Encoding“

Project manager:	Prof. D. Müller
Project duration:	01.07.1999 - 31.03.2005
Project goal:	Development and implementation of coder-decoder systems for SOC system busses which minimize under a set of constraints the total power dissipation on a system bus with its coder and decoder implementation through reduction of switching activity on this bus.

Project: „Prüf- und Qualitätssicherungssystem für die industrielle Fertigung von wafer-gebondeten Mikrosystemen“ (Mikroprüf)

Project manager:	Dr. K. Kadel, Steag microParts GmbH
Partners:	FhG IWM Halle, ZfM - TU Chemnitz, X-Fab GmbH, Robert Bosch GmbH, Hegewald & Peschke Mess- und Prüftechnik GmbH
Project duration:	11/2002 – 10/2005
Project goal:	Evaluation of different wafer bond techniques and optimization of wafer bond processes.

4.2 Collaborative Research Center No. 379 : (Sonderforschungsbereich SFB Nr. 379) 01. 01. 1995 – 31. 12. 2006

„Arrays of micromechanical sensors and actuators“

The MEMS research field covers several provinces using different microtechnology methods for the fabrication.
The subject of the SFB deals with the well-defined part of the microsystems research:
“The realization of sensor and actuator arrays consisting of a number of single components”.
Thus, results concerning the behaviour and new application fields of the devices would be expected.
As a vision of the future it is aimed toward a system which combines the arrays with the electronics by microtechnology integration.

Within the focus of interest are the following topics:

- Micromechanical scanning devices (actuators fabricated in bulk and surface micromachining)
- Use of micromechanical basic components, e.g. for ultrasonic arrays and positioning systems, including the application of new materials
- Optimization of the AIM process flow

The following institutions are working together

Faculty of Electrical Engineering and Information Technology
Chair Microsystems and Precision Engineering, Prof. Dr. Wolfram Dötzel
Chair Electronic Devices, Prof. Dr. Gunter Ebest
Group Material Science, Prof. Dr. Joachim Frühauf
Chair Microtechnology, Prof. Dr. Thomas Gessner
Chair Measurement and Sensor Technology, Prof. Dr. Wolfgang Manthey
Chair Circuit and System Design, Prof. Dr. Dietmar Müller
Chair Opto- & Solid-State Electronics, Prof. Dr. Christian Radehaus

Faculty of Natural Science
Chair Semiconductor Physics, Prof. Dr. Dietrich R. T. Zahn
Chair Solid Surfaces Analysis, Prof. Dr. Michael Hietschold

Faculty of Mechanical Engineering
Institute for Print and Media Technology, Prof. Dr. Arved C. Hübler

Fraunhofer Institute for Reliability and Microintegration, Branch Lab Chemnitz
Micro Materials Center Chemnitz, Prof. Dr. Bernd Michel

Institut für Mechatronik e.V. Chemnitz, Prof. Dr. Peter Maißer

Subproject A1: Design of Micromechanical Components
Development of accelerometer arrays for drift compensation

M. Dienel[1], W. Dötzel[1]
[1]Chemnitz University of Technology, Faculty of Electrical Engineering and Information Technology

1 Introduction

This article describes the development and the measurements that were made with a new accelerometer. The developed acceleration sensor array will be used in an inertial measurement system. The approach fuses the information of redundant sensors. In this application, the redundancy provides validity check and the possibility to correct dynamically the offset caused by temperature and ageing drift.
Ideally, two noncollinear acceleration sensors fulfil the requirements to measuring motion in plane. The magnitude and the angle of the acting acceleration can be calculated. Practically, the measured sensor signal is superimposed by the real acceleration and a term caused by drift. Equation (1) illustrates this issue.

$$a_{measure} = a + a_{offset}(t,T) + a_{offset,\,fixed} \qquad (1)$$

If the temperature dependency is similar for a given sensor array design, the variable term in the equation could be eliminated using the difference of the measured signals (2) [1].

$$\begin{pmatrix} a_x \\ a_y \end{pmatrix} = (W^T W)^{-1} W^T \left(\vec{a}_{diff} - \vec{a}_{offset,\,fixed} \right) \qquad (2)$$

Where W is a difference angle matrix depending on the alignment of the sensors in the array. The elimination of the temperature dependant terms requires a similar behaviour. Consequently, the design of the array must consider the equal influence on every sensor in the array.

2 Principle

The six sensors of one array shown in Figure 1 have a similar basic structure [2]. The seismic mass is attached to a ring segment. The ring is supported by bending beams and they are fixed at a centred anchor. The bending beams are similarly aligned in the chip. Hence, the spring constant for all bending beams is equal in the (100)-silicon chip. To change the axis of detection the seismic mass has three different positions at the ring segment [upper part of Figure 1]. So the centre of gravity is displaced and the axis of detection is rotated in the sensor design. The mass part covers a sector of 36°.

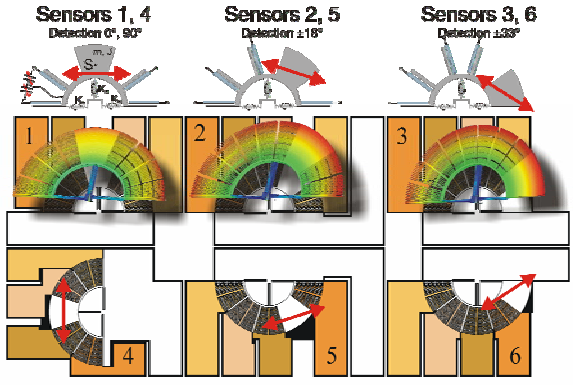

Figure 1: Sensor chip and schematics of principle

Basically, the sensor can be described as a rotational mechanical spring mass damping system. Therefore, the differential equation (3) has to be solved. At first, all terms must be determined.

$$J\ddot{\varphi} + D_R\dot{\varphi} + K_R\varphi = M_{mech} + M_{elec} \qquad (3)$$

So, a FE-model was created for structural and modal analysis. The sensors were designed for an Eigenfrequency of 2 kHz, the seismic mass is about 49 µg. For a reduced model, which is described in [3], the moment of inertia and the spring constants were extracted from the FE-model. The damping behaviour was estimated using analytic formulas [4]. The reduced model

was implemented in PSpice and a dynamic and static simulation was done [Figure 4].

3 Measurements

The sensors were fabricated using the BDRIE silicon technology [5]. The active sensor elements have a height of 50 µm.

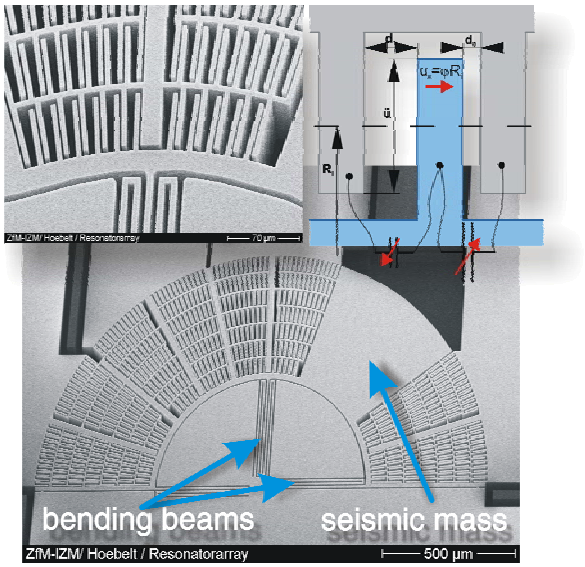

Figure 2: SEM of a sensor element and the capacitive combs

The smallest structure detail is the gap (2 µm) of the capacitors. Figure 2 shows a part of the fabricated sensor chip. A detail of the comb cells and the modelling parameters are highlighted. The capacitors are used for detecting the deflection of the seismic mass. The capacitance varies, if a acceleration is applied depending on magnitude and direction. To enhance the linearity and to reduce the cross sensitivity the capacitors form a three plate (differential) capacitance. Every sensor consists of four such capacitance arrangements, so, the measurement and the electrostatic feedback force is separated.

At first the capacitance distribution was measured [Figure 3]. For comparison a second sensor design consisting of linear accelerometers (SBS) was fabricated on the same chip, the results are also shown in the figure. The results show differences in the capacitance of the segments across the wafer. The variance increases on the level of view, the lowest values are reached on single chip level. The measurements in the field of gravity are shown in Figure 4, which are compared to simulation results. The differences are explained by irregularities in the fabricated sensors, which are not considered in the simulation model.

4 References

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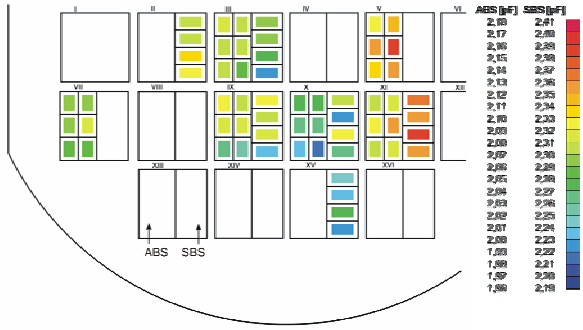

Figure 3: Measured capacitance distribution [6]

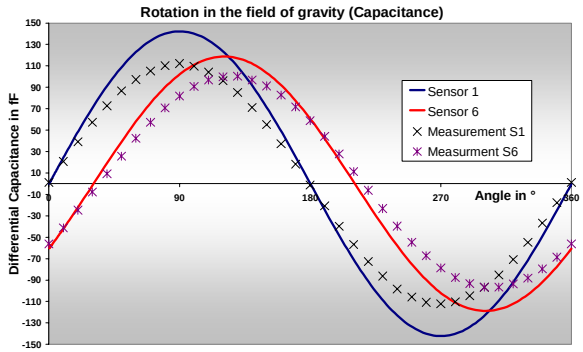

Figure 4: Simulated and measured capacitance during rotation of the sensors in the field of gravity [6]

Subproject A2: Acceleration sensor modelling using SystemC-AMS

Markert, Erik; Müller, Dietmar; Heinkel, Ulrich
TU Chemnitz, Faculty of Electrical Engineering and Information Technology,
Professorship Circuit and System Design

1 Introduction

The complexity of today's systems increases rapidly. So simulation of the whole system using low abstraction level simulators (e.g. Spice for analog, VHDL-Modelsim for digital) takes too much time. This problem is currently solved using high-level descriptions such as Matlab/Simulink and SystemC. But most systems contain both digital and analog parts. For this reason SystemC is extended by a C++-library to SystemC-AMS [1]. This language allows modelling of analog and digital hardware as well as software. The applicability of SystemC-AMS for MEMS modelling was checked in [2].
A new acceleration sensor is currently developed in the project A1 "Component Development" of the collaborative research center 379. This sensor will be part of an inertial navigation system which additionally consists of FPGA-based digital hardware and PC-based software. To start development of digital parts before availability of the new sensor a high level model of that sensor has to be created. This model shall be described briefly in the following article.

2 Sensor model

The sensor [3] consists of one seismic mass and four comb segments for capacitive acceleration detection. Figure 1 shows the structure of the sensor.

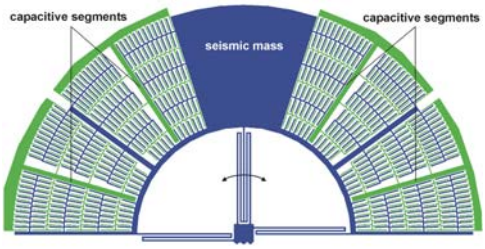

Figure 1: Structure of the sensor

An acceleration causes a linear displacement of the seismic mass. The three springs force the segments on a circular path. This rotational movement leads to capacity changes in the comb segments and therewith to a current flow which could be analysed.

The sensor is divided into a mechanical (displacement) and an electrical (capacity calculation, feedback) part. The derivation of modeling equations is described in an early work [4]. In this article only the resulting equations should be epitomized.

Mechanical part

The tangential acceleration a_s of a segment depends on the translational accelerations a_x and a_y, the current displacement angle α and the segment's position angle β_s:

$$a_S = a_X \times \sin(\alpha + \beta_S) + a_Y \times \cos(\alpha + \beta_S)$$

Therefore the segment's torque can be calculated in dependence of the segment's mass m_s and the coordinates of the center of gravity x_s and y_s related to the center of rotation:

$$M_S = m_S \times a_S \times \sqrt{x_S^2 + y_S^2}$$

The motion equation for rotation can be refined to:

$$\sum M_S - \sum M_R = \sum J_S \frac{d^2\alpha}{dt^2} + k\frac{d\alpha}{dt} + \sum c\alpha$$

Thereby M_R specifies the reset torque caused by applied voltages. The moment of inertia J_s and the spring constant c_{rot} are calculated from geometry data and material constants. The rotational displacement α is determined by solving the differential equation.

Electrical part

The rotational displacement α causes a change of the segment's capacity C_s. This leads to a current flow I_s depending on the measurement voltage U_s:

$$I_S = U_S \times \frac{dC_S}{dt} + C_S \times \frac{dU_S}{dt}$$

In addition the mechanical reset torque results on voltage and capacity changes:

$$M_R = \frac{1}{2} U_S^2 \times \sqrt{x_S^2 + y_S^2} \times \left(\frac{dC_{S1}}{ds} + \frac{dC_{S2}}{ds} \right)$$

The dependence of the reset torque M_R and therewith the sensor's displacement α on the applied voltage U_S is utilized to compensate the sensor movement. For this reason the voltages of the segments are pulse width modulated.

Sensor model

The current version of SystemC-AMS (0.14) offers two possibilities for the description of analog behavior: linear electrical nets solved by Modified Nodal Analysis (MNA) and Static DataFlow networks (SDF).
The usage of SDF networks speeds up simulation significantly. So this network type is preferred for sensor modeling. The behavior of the mechanical and the electrical subsystem is described using Laplace transfer functions representing the differential equations. The analysis and feedback module additionally consists of an electrical network representing op-amp circuits. Figure 2 gives an overview of the structure of the sensor model.

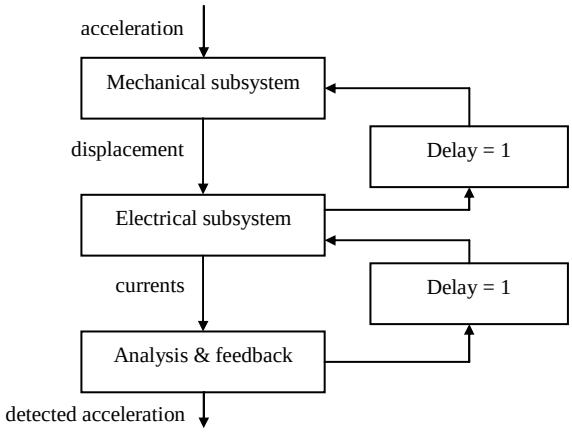

Figure 2: Structure of the sensor model

3 Simulation Results

At the moment parameters for analysis and PWM are still under research. The SystemC-AMS model helps the designers to evaluate new parameter settings quickly. The sensor output voltage with activated PWM feedback is plotted in figure 3. It represents the measured acceleration in multiples of gravitation constant.

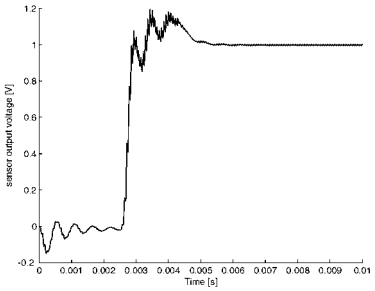

Figure 3: Simulation output on a 1g step

4 Conclusion and Outlook

The article presents the modeling of a capacitive acceleration sensor with feedback. The sensor will be part of an inertial navigation system which also consists of digital and software parts. For system modelling SystemC-AMS is used which allows simulation of all three subsystems in one tool. The sensor model is verified using a VHDL-AMS and an FEM model.
After completion of all system components it is planned to use a walking robot (figure 4) as carrier for the inertial navigation system

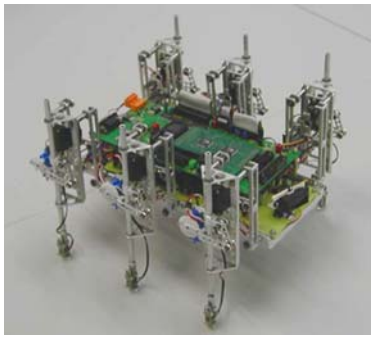

Figure 4: Walking robot

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Subproject A4: Micromachined Force Coupled Sensor System for Frequency Selective Vibration Monitoring

Forke, Roman[1]; Mehner, Jan[2]; Dötzel, Wolfram[3]; Gessner, Thomas[1]
[1]Chemnitz University of Technology, Center for Microtechnologies
[2]Fraunhofer-IZM Chemnitz, Department MDE
[3]Chemnitz University of Technology, Faculty for Electrical Engineering and Information Technology

1 Introduction

Vibration monitoring has become an important means for wear state recognition of industrial machinery such as cutting tools, bearings, gears, pumps or engines. The majority of mechanical vibration used to identify the wear state is found in the frequency range from a few Hertz to 10 kHz. Currently, piezoelectric wide band transducers combined with signal analysers are widely used to obtain the spectrum. Due to high costs permanent monitoring is limited to expensive machinery or safety related applications.
Generally, it is sufficient to analyze only a few spectral lines in order to get the relevant information about the wear state and process conditions. Thus, micromechanical frequency selective vibration sensors are powerful means for this type of application and were investigated earlier [1]. The main drawback of resonant sensors is that monitoring of the low frequencies requires excessively large chip areas or weak suspensions to lower the stiffness to mass ratio for applications well below 1 kHz.

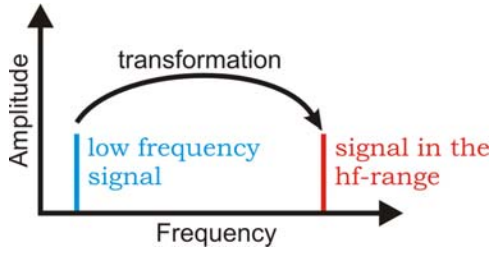

Fig. 1: Basic principle

To extend the frequency range down to a few Hertz, we developed a novel sensor principle based on frequency transformation. With the help of a micromechanical coupling structure, the mechanical signal of low frequency is transformed to a higher frequency where it can be detected selectively (Fig. 1). Thus, the spectral information is read out directly without subsequent Fast Fourier Transformation (FFT) leading to fewer costs for permanent wear state monitoring.

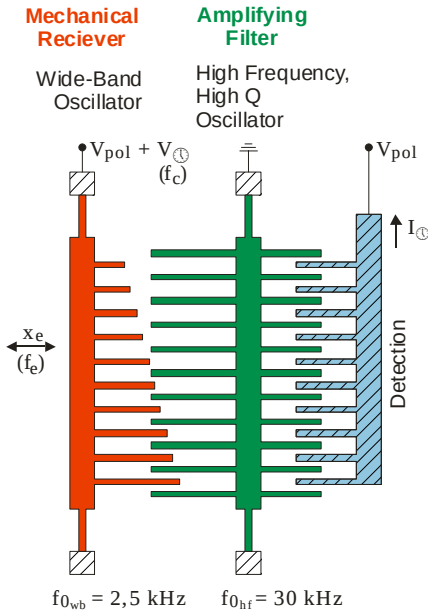

Fig. 2: Simplified structure of the sensor system

2 Principle of Operation

The force coupled sensor system consists of two separated but electrostatically coupled mechanical spring-mass-damping systems (Fig. 2). The first oscillator operates as a wideband, optimally damped vibration sensor and detects the mechanical vibrations. With its eigenfrequency set to 2.5 kHz, it detects vibration signals up to 1 kHz proportional to the acceleration. The second oscillator is a high Q resonator with its eigenfrequency set to approximately one decade above the latter.
Due to mechanical vibration, the wide-band sensor couples electrostatic forces to the high Q resonator, which is additionally stimulated by a carrier signal. Amplitude modulation occurs in the same way as known from communications engineering in radio receivers. Consequently we get the lower and upper sidebands with the information of the vibration signal as shown in Fig. 3.
By variation of the carrier frequency, it is possible to adjust the lower sideband exactly to the resonance frequency of the second oscillator.

Thanks to the high Q-Factor of the MEMS, the signal is amplified in a very small band with a high signal-to-noise ratio. Hence, the sense frequency can be tuned by variation of the carrier frequency. The motion signals are detected by capacitive pick-up.

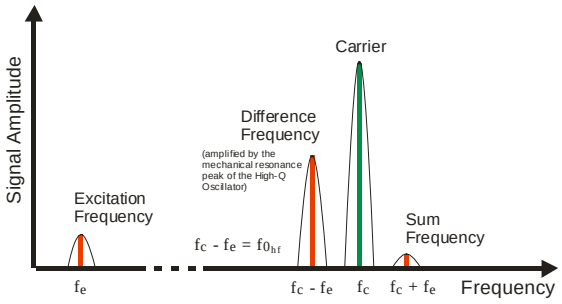

Fig. 3: Principle of operation

2.1 Electrostatic force coupling

For the presented principle of operation, the electrostatic coupling force has to be amplitude dependant as shown in equation (1). To comply with this condition, the capacity function of the coupling electrode needs to be a square function. This can be achieved by variation of the electrode form as reported in [2]. The comb electrodes of linear varied finger length lead to the required function.

$$F_{el} = \frac{V^2}{2} \cdot \frac{dC}{dx} \quad with \quad \frac{dC}{dx} = const. \cdot x \qquad (1)$$

2.2 Fabricated sensor structure

Figure 4 shows a 3D model of the developed sensor system. The two separated oscillators are coloured differently. To meet the electrical requirements and contact both of the oscillators electrically, the wide-band oscillator encloses the high Q resonator in a “C” shape.

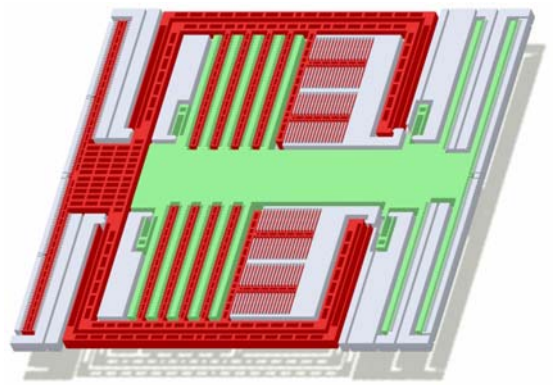

Fig. 4: 3D model of the sensor system

The sensor is fabricated in the BDRIE (Bonding and Deep Reactive Ion Etching) silicon technology [3]. In Fig. 5 a light microscope photo of the fabricated sensor is displayed.

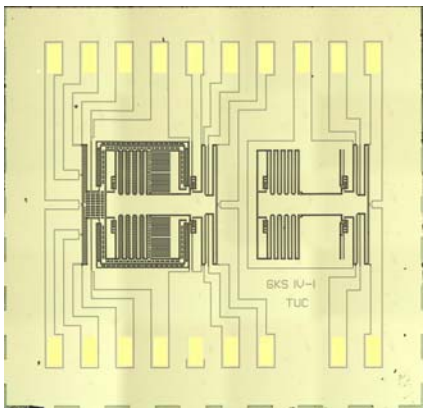

Fig. 5: Light microscope photo of the fabricated sensor

3 Summary

With the presented micromachined force coupled sensor system the frequency range for permanent wear state monitoring could be extended down to a few Hertz. The sense frequency is acquired by a simple frequency tuning mechanism. Further work includes a characterization of the fabricated structures in which important aspects are eigenfrequencies as well as bandwidth and damping effects.

Acknowledgements

The work is done within the Collaborative Research Center SFB 379 which is funded by the German Research Association (DFG).

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Subproject B2: Experimental characterization, model adaption – reliability
Characterization of MEMS on the base of Eigenfrequencies

Dötzel, Wolfram[1], Michel, Bernd[2]
[1]TU Chemnitz, Fakultät für Elektrotechnik und Informationstechnik, Professur für Mikrosystem- und Gerätetechnik
[2] FhG-IZM Berlin, Abteilung MR & MM

1 Introduction

During development as well as in the manufacturing process of micro electro mechanical systems (MEMS) it often is essential to perform a comprehensive characterization of the realized structures. The major part of MEMS can be assign to spring-mass-damping-systems. Well known examples are gyroscopes, acceleration and vibration sensors and micro mirrors. Beside electrical properties, like capacitance of sensors or surface properties, like warp and roughness for optical applications MEMS's are characterized by their geometry and material properties as density, Young's modulus and mechanical intrinsic stress.

At the Chemnitz University of Technology a micro mirror array was developed that consists of 48 electrostatically driven mirrors (Fig. 1). It is implemented in a Hadamard transform spectrometer as encoding mask [1]. The expected benefit of the array is equality of its micro mirrors. While the optical properties fulfill this expectation, the first resonant frequencies of the micro mirrors show strong deviations within the arrays. This can be caused by differences of the flexures cross section ($5 \times 5\ \mu m^2$) and intrinsic stress within the flexures.

In order to improve the mirror design and the fabrication technology it is necessary to determine those properties that are responsible for the change of resonant frequency. Therefore a method was developed that enables determination of thickness and width of the flexures as well as the intrinsic stress based on theoretically predicted and experimentally obtained Eigenfrequencies.

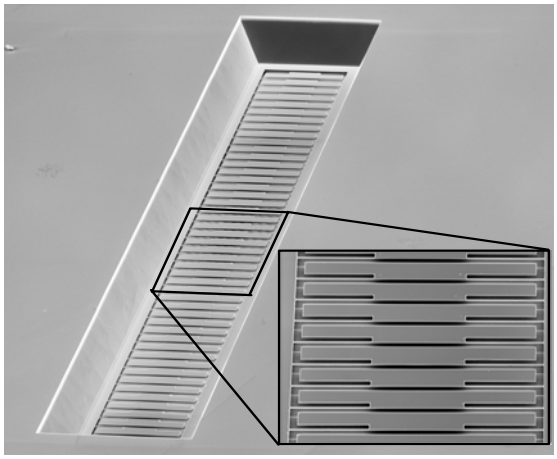

Fig. 1: SEM view of the micro mirror array

2 Parameter identification method

Commonly every development of a new MEMS starts with design and simulation of its behavior. This is where the presented method begins too. As to be seen from fig. 2 the simulation is performed in terms of a variational analysis. In case of the micro mirror array, this means the flexure's width and thickness as well as the stress are set to be parameters which are iteratively changed. A prestressed modal analysis is used to calculate the first 6 Eigenfrequencies depending on the three parameters. A three dimensional polynomial interpolation is applied to the obtained data that yields an analytical description of dependence of each Eigenfrequency on the three parameters. After manufacturing the MEMS the structure is investigated regarding its Eigenfrequency. A measurement setup consisting of an arbitrary waveform generator, a Laser Doppler interferometer [2] and a signal analyzer enables acquisition of frequency response functions (FRF).

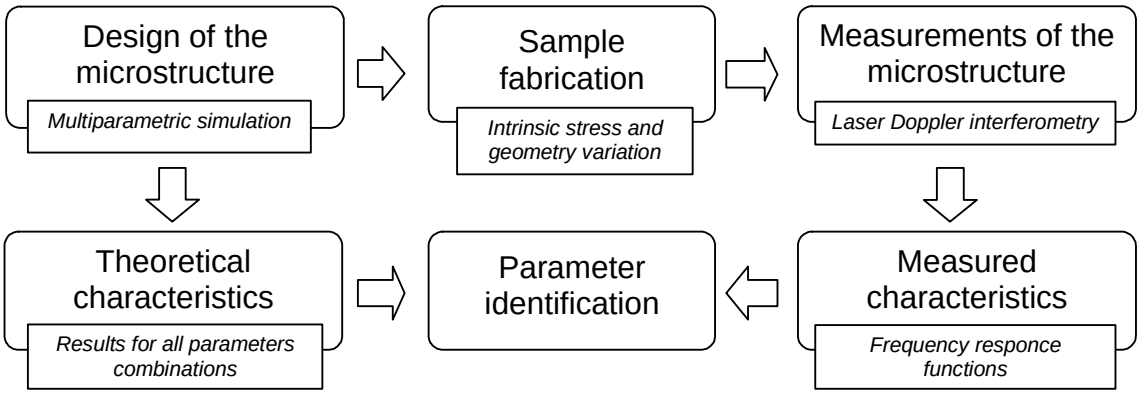

Fig. 2: Flow chart of the parameter identification method

The FRF imply the Eigenfrequencies which are extracted. These frequencies and the equation of the polynomial interpolation of the simulation data are used to calculate the three unknown parameters in terms of a least square method. Table 1 shows the first four out-off plane Eigenfrequencies, thickness (th_s), width (w_f), and stress (σ) of two micro mirrors.

Table 1: Measured Eigenfrequencies and micro mirror parameters

	Mirror 1	**Mirror 2**
fo_1 [Hz]	8172.25	8411.31
fo_2 [Hz]	14977.11	15662.23
fo_3 [Hz]	34113.90	34951.71
fo_4 [Hz]	53852.06	54059.29
th_s [µm]	4.336	4.343
w_f [µm]	4.363	4.296
σ [MPa]	0.350	4.275

The diagram in fig. 3 shows the obtained flexures width and thickness for 48 mirrors in one array. The thickness shows an increasing tendency towards higher mirror numbers. The diagram in fig. 4 shows the calculated stress in flexures for 48 mirrors in one array. As to be seen, it changes from 4 to -9 MPa, that strongly influences the first resonant frequencies. As a conclusion it is to be said that thickness and stress variation are the major reasons for the inhomogeneities of the first resonant frequency. The developed parameter identification method enabled determination of three parameters very time efficient and with a sufficient accuracy.

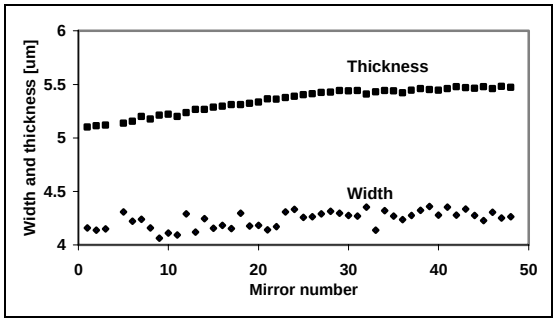

Fig. 3: Flexure's width and thickness in one array

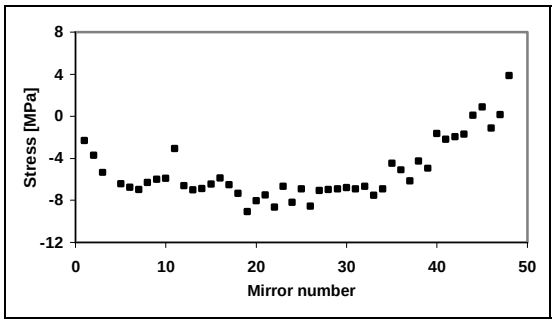

Fig. 4: Stress in flexures in one array

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Subproject B5: A new microactuator with transmission grating for a spectral imaging technology

J. Bonitz[1]; M. Flaspöhler[2]; C. Kaufmann[1]; R. Hahn[1]; T. Gessner[1]; Hübler, Arved Carl[2]
[1] Chemnitz University for Technology, Centre for Microtechnologies
[2] Chemnitz University of Technology, Faculty of Mechanical Engineering, Institute for Print and Media Technology

1 Introduction

The accurate colour reproduction of an arbitrary original image is a common problem of image capturing and printing processes. There, spectral methods of image capturing offer a better colour accuracy as the state-of-the-art RGB technique, because more than three colour channels are used.
In this project, a spectral imaging system with an oscillating micro mirror with diffraction grating is developed [1,2]. Because of light absorbing and subsequent heating of the mirror plate, a change from a reflection grating to a transmission grating was realized. Because of this fact a new designed actuator was fabricated and characterized optically in the last project phase.

2 Fabrication of the microactuator

The main actuator fabrication steps are shown in Fig. 1. The basis material was a double sided polished 200 µm wafer. The first step was the deposition and patterning of the optical layers SiN and SiO_2. Afterwards the grating with lattice constants of 1.6 and 2.0 was structured in the silicon oxide layer. Figure 2 shows a SEM micrograph of the grating.

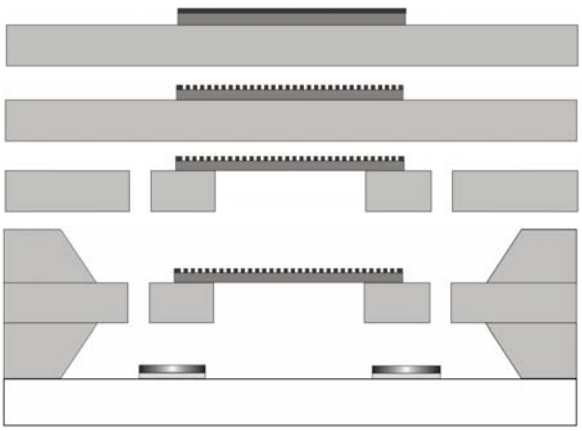

Fig. 1: Process steps of microactuator fabrication

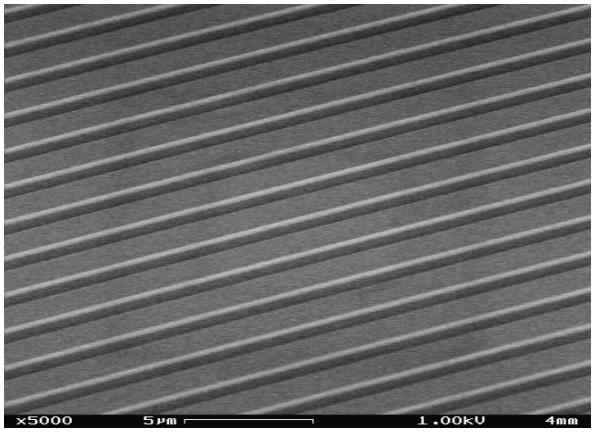

Fig. 2: SEM micrograph of the SiO_2 grating

The next step was the creation of the actuator by Silicon DRIE from the backside. With this process step a round hole with 4.2 mm of diameter was etched in the actuator plate which led to a transparent SiN membrane with a SiO_2 diffraction grating. The last step was the fabrication of the whole wafer system by different bonding processes. Figure 3 shows a photograph of a ready fabricated microactuator on conductor board.

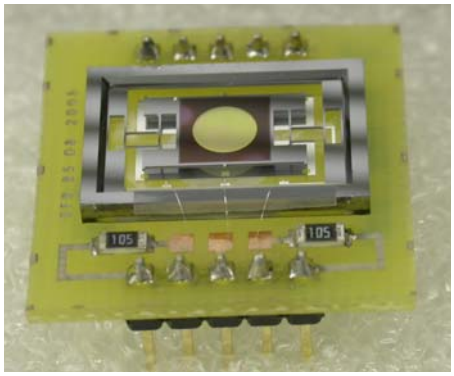

Fig. 3: Actuator on conductor board

3 Colorimetric and optical characterisation

The realised optical gratings have to be studied regarding their optical and the resulting colorimetric properties. Important optical

parameters are the spectral resolving power and the diffraction efficiency of the gratings. The realised microactuators have a transmission grating with a grating period of 1.6 or 2.0 µm. The results of the optical characterisation of these gratings are presented below.

3.1 Spectral resolving power and the resulting possible colour space

The diffraction properties of a grating are measured using a xenon lamp and various narrowband interference filters that are placed successively in the optical path in front of the grating. The distribution of the transmission characteristics against the wavelength of each filter forms a sharp Gaussian distribution with a full width at half maximum of about 15 nm. The diffracted intensity distributions are measured by a CCD-line and the spectral resolving power can be determined for the two gratings. The resolving power of the 1.6 µm grating is about 25 % higher as the 2.0 µm grating. Considering these results the possible colour space can be calculated for each grating. Figure 4 shows the resulting colour spaces for both gratings, which are both greater than the standard RGB colour space.

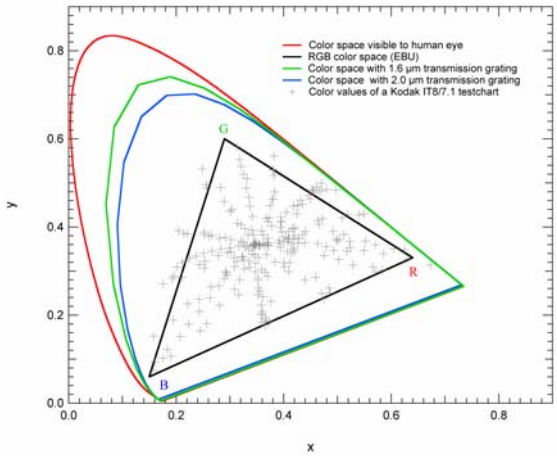

Fig. 4: Calculated possible colour spaces for the transmission gratings considering the measured spectral resolving power. The limitations are calculated in respect to the CIE light source D65. The RGB values are based on the standard of the European Broadcasting Union for television phosphors. The crosses represent the colour values of a standardised colour test chart.

3.2 Diffraction efficiency

Another important optical parameter is the diffraction efficiency of the gratings. To measure the diffraction efficiency the luminous flux passing through the transmission grating is measured in dependency on the wavelength. A photometer is positioned directly behind the grating insuring that the detector collects all of the transmitted light. Afterwards the photometer is positioned in the first diffraction order. Again the diffracted luminous flux is measured in dependency on the wavelength. The quotient between the diffracted and incident light is the relative diffraction efficiency. The measurement results are shown in Figure 5.

The measured diffraction efficiencies of the gratings are in a range between 12 % and 26 % depending on the wavelength. Compared to the previous reflection rectangular gratings [3] and the theoretical maximum diffraction efficiency of a rectangular phase grating of 42 % [4], these are good values.

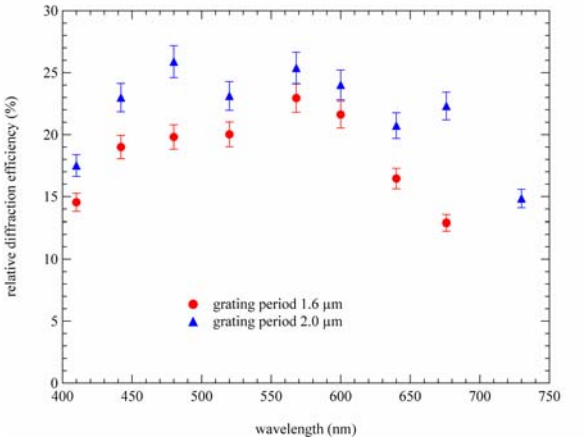

Fig. 5: Relative diffraction efficiency of the transmission gratings depending on the wavelength.

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Subproject B6: Nonoptical distance detection with Force Sensor Arrays for Dynamic Atomic Force Microscopy

Müller, Anne-Dorothea; Müller, Falk; Hietschold, Michael
TU Chemnitz, Fakultät für Naturwissenschaften, Institut für Physik, Professur Analytik an Festkörperoberflächen, 09107 Chemnitz

1 Introduction

In the project B6 of the SFB 379, cantilever arrays for Atomic Force Microscopy (AFM) are developed. Over the past 5 years, a specialized AFM system has been built which is able to work with the cantilever arrays and to evaluate signals from two or more cantilevers simultaneously. It was demonstrated that temporary devices on semiconductive substrates can be created. Their electrical characteristics can be understood with circuit simulations of adapted MESFET models [1].
Besides the multi-functional use of cantilever arrays in multiple tip applications, the worldwide cantilever developments also pursue the aim to simplify the adjustment procedures by new detection mechanisms. Here, the developments done in the project B6 have brought a significant impact to the scientific community by a non-optical detection method, the displacement current detection of the cantilever vibration.

2 General cantilever parameters

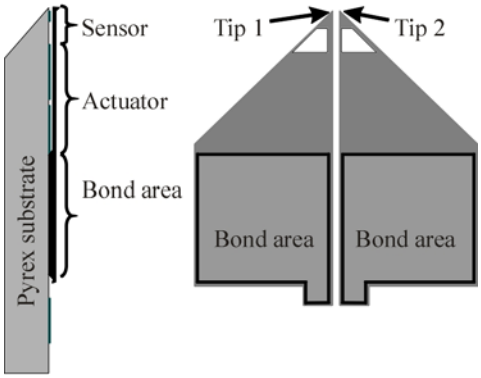

Fig. 1: Schematical drawing of double-cantilever device in side view and top view.

The cantilever arrays consist of a planar silicon membrane bonded to the glass in a certain region, where the membrane is 20 µm thick (Fig. 1). The free-standing part of the cantilever membranes is 10 µm thick and provides a 0.5 mm² large electrode in 10 µm distance to metal electrodes on the underlaying glass substrate. This area is devided into a sensor part and an actuator part. The total capacitance of the actuator is 0.44 pF per cantilever. The relative change in the total capacitance C caused by an electrode displacement of 1 nm is only 44 aF.

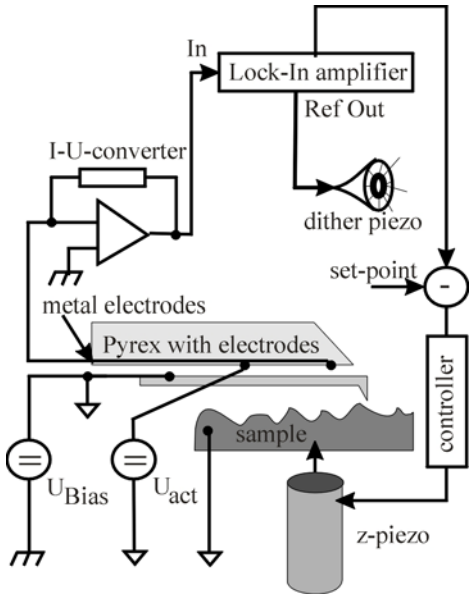

Fig. 2: Experimental setup for capacitive AFM in dynamic mode operation.

The first eigenmode of the device is found at 20 kHz, while the eigenmode of the sensors is found at approximately 140 kHz.

3 Displacement current detection

Displacement currents can be generated after the following equation:

$$I_c = \frac{dQ}{dt} = C\frac{dU}{dt} + U_{Bias}\frac{dC}{dt} \qquad (1)$$

When the applied voltage is kept constant, and one plate is oscillating vs. the other with an amplitude z_1 at a frequency f_R, Equ. 1 can be rewritten as

$$I_c = \frac{\epsilon_0 A}{d_0^2} z_1 2\pi f_R U_{bias} \qquad (2)$$

Based on the geometrical properties of the cantilever arrays follows that the displacement current caused by a 1 nm vibration amplitude z_1 at the first eigenmode at 21.3 kHz and a bias

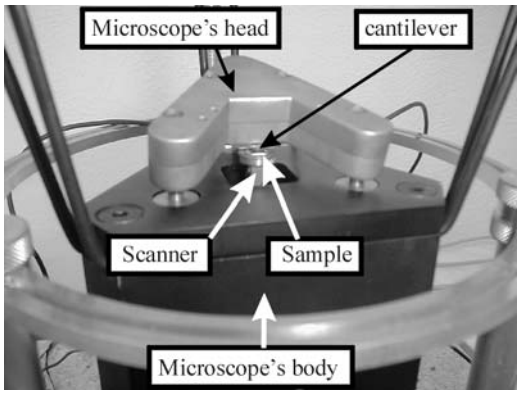

Fig. 3: Photograph of AFM head holding double-cantilever device. The low-noise, large-bandwidth current-voltage converter is implemented inside the head.

voltage of 30 V is 175 pA. Vibrations in the third eigenmode at 160 kHz should produce currents in the order of 1.3 nA/nm. The designed current-to-voltage converter for displacement current detection has an input noise of 200 fA, so the achievable signal-to-noise ratio is better than 100:1. at a reasonable bandwidth with a 1 nm vibration amplitude.

With the experimental set-up in Figs. 2 and 3, distance characteristics of displacement currents shown in Fig. 4 can be measured.

The imaging in dynamic mode with this detection mechanism has been shown and a simultaneous detection of electrical signals was applied to dopant patterns as test samples [2].

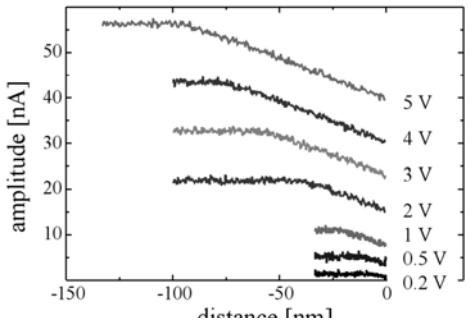

Fig. 4: Amplitude-distance curves obtained with displacement current detection for different acoustic excitation amplitudes.

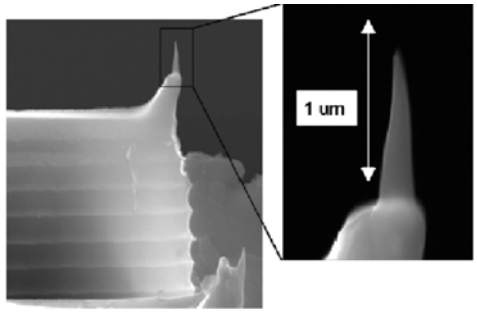

Fig. 5: W-tip deposited by electron-beam induced deposition in a $W(CO)_6$-enriched high vacuum environment.

4 Tip functionalization

Besides this instrumental work, a diploma thesis has evaluated the experimental conditions for an electron-beam induced deposition of metallic and/ or magnetic tips on the cantilever arrays.

The up to 8 µm long tips can be used to narrow the 10 µm large lateral gap between neighbored tips. Their conductance has been proven with I(U)-curves in contact AFM [3].

5 Conclusion

In 2005, the work at the cantilever arrays proceeded in physics, instrumentation and technology. Besides the non-optical detection method, geometrical improvements have reduced the cross-talk between neighbored cantilevers under ambient pressure conditions. The technology for tip sharpening has been improved and 10 nm tip radii are standard now.

6 Literature

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Subproject C2: A Novel High Aspect Ratio Technology for MEMS Fabrication Using Standard Silicon Wafers

Lohmann, Christian[1]; Bertz, Andreas[1]; Reuter, Danny[1]; Rennau, Michael[1]; Gessner, Thomas[1,2]
[1]TU Chemnitz, Fakultät für Elektrotechnik und Informationstechnik, Professur für Mikrotechnologie
[2] FhG-IZM Chemnitz, Abteilung MDE

1 Introduction

The development of a CMOS compatible technology for the fabrication of high aspect ratio microstructures (HARMs) is part of the Collaborative Research Center 379. First prototypes of *"Air gap insulated Microstructures (AIM)*" were manufactured and characterized in the third period of the project, presented elsewhere [1, 2, 3]. Beside the continuing process optimization for the fabrication of the structures, the development of the technology also includes the definition of measurement routines for wafer-level testing with a focus on process control, failure analysis and yield management.

2 A *low-g* sensor

A *low-g* inertial sensor has been chosen as one device for the evaluation of the AIM technology, because of its sensitivity and fragility. The sensor (Fig. 1) consists of a spring mass system fixed by anchors. The movement of the seismic mass, caused by inertia force or gravity, is detected by a change of the capacitance between the seismic mass and a fixed electrode. Fig. 1 shows a detailed view of a *low-g* sensor; the parameters of a fabricated sensor are listed in Tab. 1.

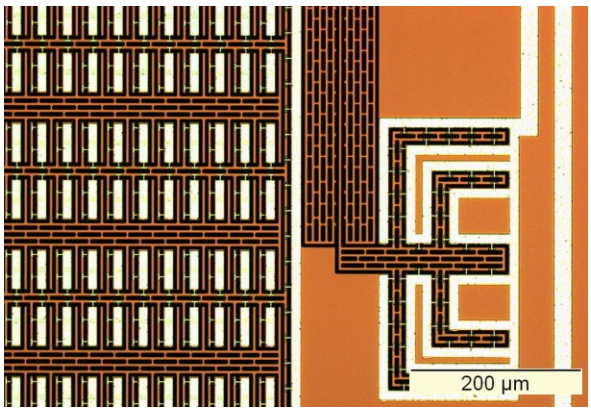

Fig. 1: Detailed view of the low-g sensor

Range	± 1 G
Sensitivity	113 fF/G
C_0	1,76 pF
Mass of the movable structure	55,7 µg
Spring constant	2,14 N/m
Eigenfrequency	986 Hz
Deflection @ 1G	256 nm

Tab. 1: Parameters of an inclination sensor

The sensors were combined and tested with different CV-converters; Fig. 2 shows the digital output signal of one of these converters depending on the rotation angle of the sensor for a 360 degree turn.

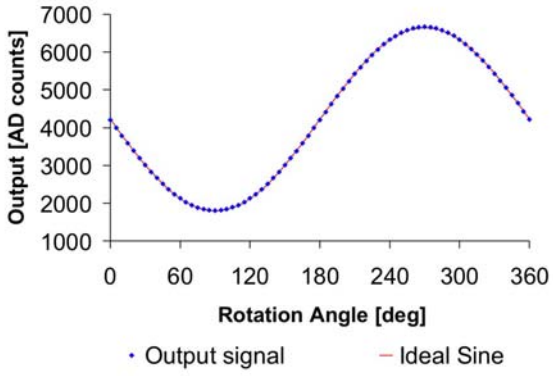

Fig. 2: Output vs. rotation of a low-g sensor in combination with a typical CV-converter

3 Wafer-level testing and failure analysis

The functional test on wafer-level of the *low-g* sensor is realized by a measurement of the leakage resistance between the electrodes and the bulk, between the seismic mass and the bulk and

between the electrodes and the seismic mass. All these measurements have been carried out by an automatic wafer prober (PA 200) in combination with a process control system (HP 4062UX).
To pass the test, the resistance between all contacts should be at least 20 MΩ. Failures can occur through particle contamination or insufficient processing.

Failure caused by particle defect

Fig. 3 shows a typical defect, caused by a particle contamination.

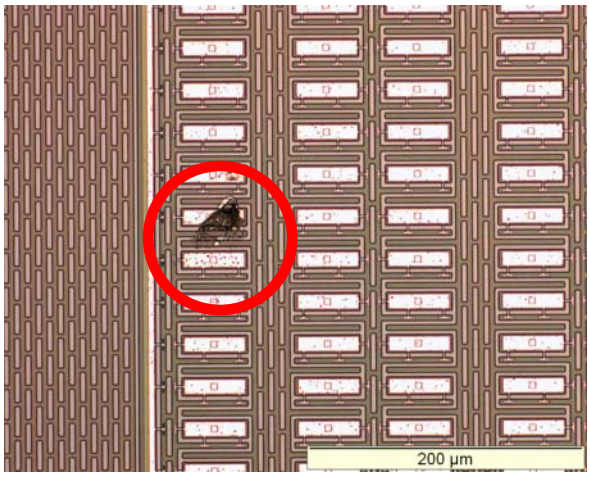

Fig. 3: Defect caused by particle contamination during processing

The particle is masking during the DRIE. Therefore, the seismic mass is not released from bulk or the electrodes are not electrically isolated with respect to bulk. Both failures can be detected by the used measurement routines. Fig. 4 is a wafer map illustrating the defects of a 100-mm-wafer used for *low-g* sensors. Green squares indicate functional sensors, orange squares sensors with one defect and red squares sensors with more than one defect. In total, there are 360 sensors with 26 orange failures and 15 red failures. This corresponds to a yield of 88.6 %.

Because the failure analysis is based on dc voltage/current measurements only, not all possible defects can be determined by this method. In the next step, active testing on wafer-level will be developed and applied to characterize the dynamic parameters of the sensors. The additional information will help to identify defect sensors. Also process parameters can be optimized by analyzing the dynamic parameters of the fabricated sensors, because they are direct related to the structure geometries and therefore corresponding to the process parameters.

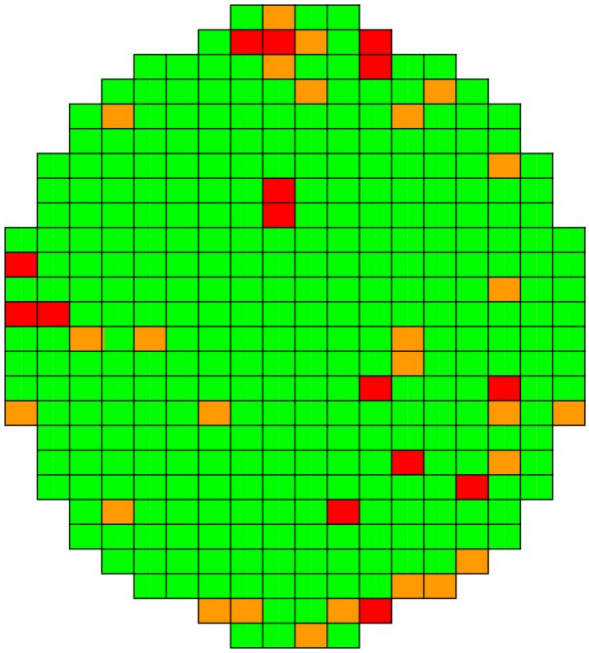

Fig. 4: Wafer map illustrating the defects of low-g sensors (green: functional sensor, orange: 1 failure per sensor, red: >1 failure per sensor)

4 References

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Subproject C4: Low temperature bonded resonator arrays with adjustable stiffness

Hiller, Karla[1]; Seifert, Mario[2] ; Shaporin, Alexej[3] ; Pohl, Robert[2] ; Frühauf, Joachim[2]; Gessner, Thomas[1]
[1]TU Chemnitz, Faculty for Electrical Engineering and Information Technology, Center for Microtechnologies, [2]Workgroup Materials in Electrical Engineering and Electronics, [3]Professorship Microsystems and Precision Engineering

1 Introduction

Resonators with tuneable vibration frequency for selective vibration measurement have already been demonstrated before[1]. Methods for tuning are either stiffening of a spring by stress or weakening by electrostatic forces. However, these resonators fabricated by near surface technologies do not provide large mass, and are therefore limited to a frequency range > 1 KHz. The approach presented here is based on a bulk technology, whereby larger masses and lower frequencies can be achieved more easily. The adjustment of spring stiffness is done by electrostatic forces, which pull together two parallel springs with a small gap between them (see Fig. 1). Hereby, the stiffness of the spring suspension is changed by a factor of 4.

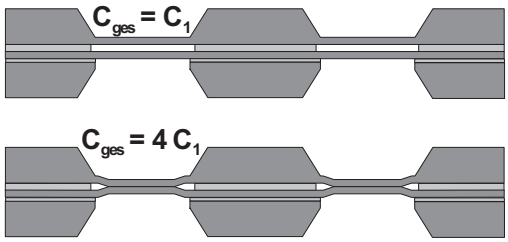

Fig. 1: Adjustment of spring stiffness by change in topology, controlled by electrostatic force

2 Concept and design

In order to realise a system with variable stiffness, a design based on an array of springs clamped on both sides has been chosen (see Fig. 2). Each pair of springs can be actuated separately, but for practical application it is helpful to use a symmetrical action (pairs 2 and pairs 3 switched in parallel). Thus, resonators with linear characteristics of stiffness or frequency (8 steps) have been designed. The main parameters which affect the switching behaviour are the stiffness of spring, the pull-in characteristics defined by the voltage, the gap and the spring dimensions, as well as the surface energy and roughness of the spring surface. For pulling the pair of springs together, the electrostatic clamping force and friction must be higher than the elastic force of the springs. On the other hand, when the voltage is switched off, the elastic force must overcome the adhesion force of the spring surface. These effects have been evaluated and calculated carefully in [2]. Fig. 3 shows the result, which has been used for definition of the dimensions for the springs.

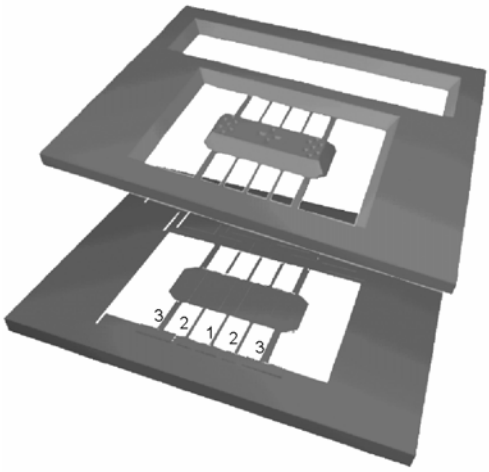

Fig. 2: Design of the resonator array as a set of 5 pairs of parallel arranged springs

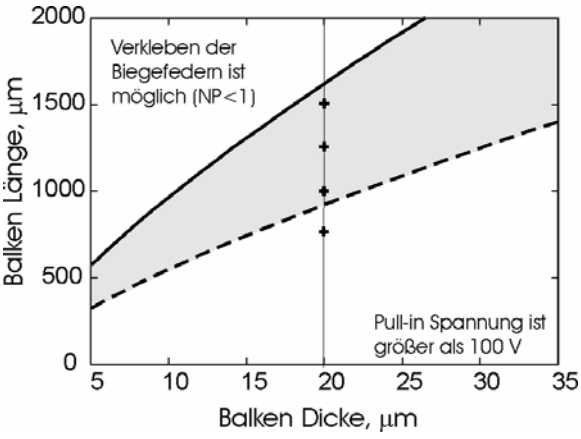

Fig. 3: Design of spring geometry (upper boundary: adhesion to high, lower boundary: pull-in voltage > 100 V

It has to be noticed that the surface energy for a hydrophilic Silicon surface (γ_s = 0,1 J/m^2) has to be reduced at least by a factor of 10 to get reasonable values for spring dimensions. Pre-investigations have shown that this is possible by a plasma etch process, which increases the surface roughness by a factor of approximately 10. However, the results are strongly influenced by humidity, too. Therefore, a set of test structures (clamped and free beams) have been designed in order to measure the actual surface energy [2].

3 Fabrication

The resonator is fabricated by bulk micromachining (using a combination of Si dry and wet etching). The process flow of the upper wafer is very simple (shown in Fig. 4). Silicon nitride serves as an etch mask for the wet etch process as well as a protective layer for the bonding oxide area. It is removed by wet etching just before direct bonding.

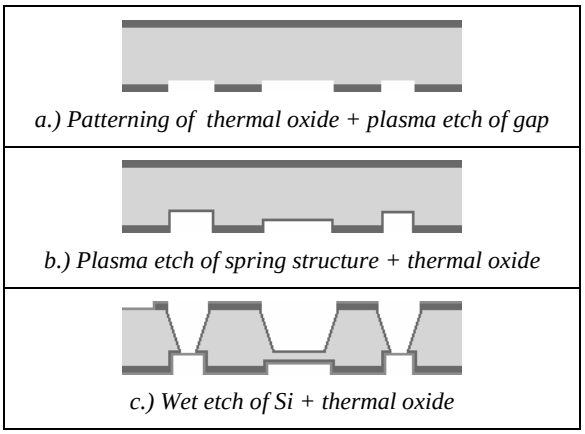

Fig. 4: Process flow of the upper wafer

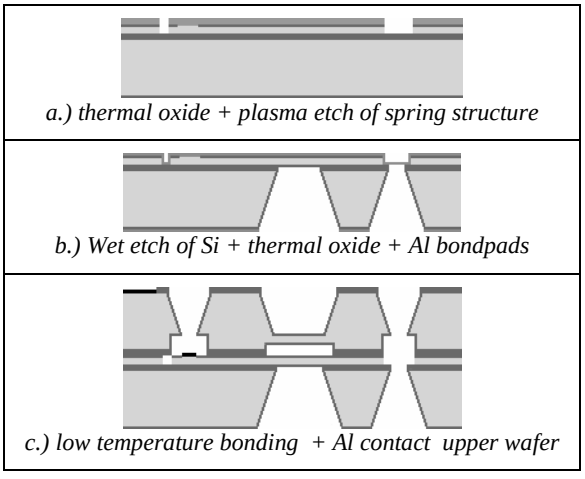

Fig. 5: Process flow of the lower SOI wafer and bonding

For the lower wafer, a similar process flow can be applied. However, in order to achieve Si springs which are separated from each other by air trenches and thermal oxide layers, a SOI wafer has been used. Metallization of the bond pads on the lower wafer must be done before bonding. Therefore, the established low temperature direct bonding process including oxygen plasma activation has been applied [3].

4 Results and future work

First demonstrators have been fabricated successfully. Fig. 6 shows the resonator and some details of springs. The spring dimensions are thickness 20 µm, width 50…100 µm and length varying from 700 µm to 1500 µm. The gap between the springs is 2 µm. As expected, this gap is not closed after bonding, whereas the chip frame and the center boss have been bonded very well by applying a selective pressure during pre-bonding. Now the demonstrators are ready for characterization, this will be aim for future work in 2006.

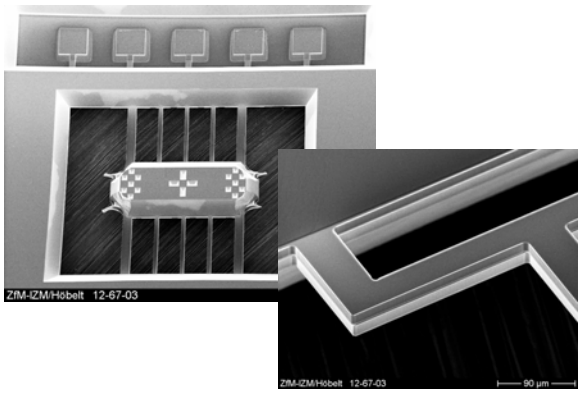

Fig. 6: SEM pictures of the resonator structure: whole bonded resonator and detail of two parallel springs with stress compensation beams (gap between them 2 µm)

4 References

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4.3 Special Reports

W(Si)N layer as Diffusion Barrier for Copper Metallization

Ecke, Ramona[1]; Schulz, Stefan E.[1]; Hecker, Michael[2]; Engelmann, Hans-Jürgen[3]
[1] TU Chemnitz, Center for Microtechnologies
[2] Institute for Solid State and Materials Research, 01069 Dresden, Germany
[3] AMD Saxony LLC &Co KG, 01330 Dresden, Germany

1 Introduction

The requirements for diffusion barriers for copper metallization are typically in conflict with each other. It is difficult to find such material that is conductive and amorphous and non-reactive in the layer thickness range of 10 nm and below. Nitrides of transition metals are promising candidates for diffusion barriers in particular WN_x that can be easily formed in amorphous microstructure. But WN_x compositions are metastable, so that barrier failure can occur at the crystallization point (600°C) or later for N lost.
A ternary WSiN composition can increase the stability of amorphous microstructure. However, increasing Si_3N_4 phase content increases both amorphization tendency and resistivity.

2 Process

To an existing PECVD process for the deposition of WN_x silane is added to obtain a ternary barrier film. The WN_x barrier is deposited by a $WF_6/Ar/N_2/H_2$ chemistry with followed process parameters: T = 380°C, p = 450 Pa, $H_2/WF_6 = N_2/WF_6 = 80$ and 50 W RF power. The electrical resistivity of WN_x is 210 µΩcm and is independent of the barrier thickness because of the amorphous microstructure. After temperature annealing at 600°C/4h in vacuum the film crystallize in 2 phases, W_2N and W. [1]
Silane is added in different flow ratios to WF_6 to this process.

3 Results

3.1 Simultaneous inlet of SiH_4 and WF_6

If SiH_4 is introduced together with WF6, the result is a two layer system. The thickness was determined by XRR. The layer structure appears inhomogeneous and an underlayer was detected. Further insight into the layer structure was gained from GDOES depth profiles and X-TEM images with EELS line scan. In Fig. 1 the double layer system is clearly visible. The first layer which was formed is a SiO_xN_y layer with incorporated W enrichments, which were identified as the dark shadows in the SiO_xN_y layer. The following layer is composed of an amorphous WN_x matrix with incorporated W grains. No significant Si amount is incorporated in the WN_x layer as proved by GDOES (detection limit ~ 0.01 at%). The thickness of the SiO_xN_y and WN_x sublayers, and the size and quantity of the W grains depend sensitively on the SiH_4/WF_6 ratio and increase with rising ratio.

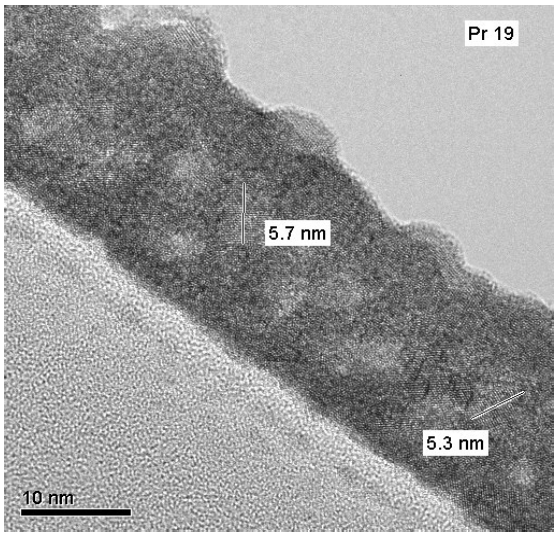

Fig. 1: Double layer system evolving from PECVD using $WF_6/Ar/N_2/H_2/SiH_4$: SiO_xN_y/WN_x with nanocrystallites in an amorphous matrix

The cause of the double layer formation is the long incubation time before the first nuclei are formed on the silicon oxide surface (Fig. 2). During this time the SiO_xN_y layer is formed, because the deposition parameters (pressure, total gas flow and gas ratios) are similar to a

SiN_x PECVD process. If silane is introduced after the incubation time, the formation of the double layer system can be prevented.

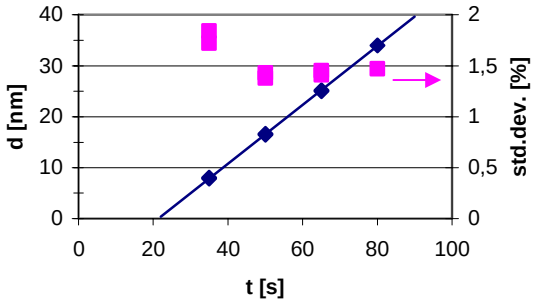

Fig. 2: PECVD WN_x film thickness vs. time showing growth incubation time for the binary process; H_2/WF_6 = 80, H_2/N_2 = 1, T = 380°C, p = 430 Pa, RF power = 50 W

3.2 SiH_4 inlet after incubation time

For obtaining a single layer system with ternary composition, silane is introduced to the process after the incubation time of 22 s (see Fig. 2). The investigated SiH_4/WF_6 flow ratios were in the range from 1 to 5.

Table 1: Sheet resistance, thickness as determined by XRR, and resistivity of W-Si-N films for different SiH_4/WF_6 ratios (silane introduced after the WN_x growth incubation of 22s)

SiH_4/WF_6	Rs [Ω/sq.]	d [nm]	ρ [μΩcm]
1	231	10	231
2	344	7	240
3	453	10	453
4	416	11.6	482
5	437	13.5	590

In Table 1 the measured sheet resistance and thickness values as well as the resulting resistivity of the deposited W-Si-N films is summarized for different SiH_4/WF_6 flow ratios. The electrical resistivity increases with rising SiH_4/WF_6 ratios, even though a further Si introduction in the barrier cannot be detected by GDOES. Only for the ratio SiH_4/WF_6 = 4, up to the middle of the layer the Si content is higher, but decreases drastically towards the film surface. Nevertheless, the barriers show a higher thermal stability compared to WN_x. Except WSiN-1 all other compositions still remain amorphous after vacuum annealing at 600°C/4h.

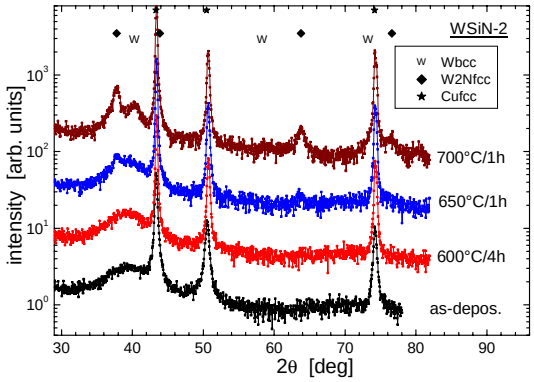

Fig. 3: GI-XRD pattern of WSiN-2 in the as-deposited state and after vacuum anneal at different T. Crystallization starts up to 650°C compared to WNx at 600°C/4h.

4 Summary

The addition of silane to a WN_x PECVD process for deposition of ultrathin films can lead to the formation of a Si stabilized W(Si)N film, but this fact depends strongly on the point in time of the silane addition. A too early addition resulted in the formation of a double layer system consisting of a SiO_xN_y layer and an amorphous WN_x layer with imbedded W grains. The lower SiO_xN_y layer is deposited during the long incubation time necessary to form the WN_x nuclei. This double layer stack is not appropriate for the application as barrier in copper metallization.
A later silane addition resulted in films with higher thermal stability compared to the binary WN_x barrier. In the as-deposited state all W-Si-N compositions have an amorphous microstructure, a favoured structure for barriers. First structural changes were observed after vacuum annealing at 650°C/1h, and the crystallization proceeded at 700°C/1h resulting in β-W_2N and α-W formation. For SiH_4/WF_6 = 2 the electrical resistivity is moderate elevated to 240 μΩcm compared 210 μΩcm of the binary process, but also the thermal stability is improved.

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Mechanical characterization of porous ultra low-k films with k~2.2

M. Herrmann[a,b]; N. Schwarzer[c]; S. Frühauf[a]; S. E. Schulz[a]; T. Gessner[a,e]; F. Richter[b]; D. Schneider[d]
[a]Centre for Microtechnologies, TU Chemnitz, Germany
[b]Solid state physics, Insitute of Physics, TU Chemnitz, Germany
[c]Saxonian Institute of Advanced Surface Mechanics, Eilenburg, Germany
[d]Fraunhofer Institute for Material and Beam Technology IWS, Dresden, Germany
[e]Fraunhofer Institute for Reliability and Microintegration, Chemnitz, Germany

1 Introduction

The sufficient mechanical stability as well as the appropriate characterization method to test it are key challenges, which have to be solved for integration of porous ULK dielectrics in Cu/ low-k interconnect systems of integrated circuits. The application of porous low-k interlayer dielectrics is planned for the 45nm technology node and below. Mechanical load on these films stems mainly from chemical mechanical polishing and packaging.
Goals of our research in this field are an evaluation of the available characterization methods for that special kind of compliant films and the determination of appropriate mechanical parameters in order to select the suitable film material. Mechanical properties like yield stress and Young's modulus of the porous material can be used in order to deal with the material behaviour as well as the failure mechanisms under typical loading conditions. Mesoporous silica as well as MSQ-based films with k=1.9…2.4, deposited with several thicknesses and different porosities on silicon wafers by spin coating, were investigated.

2 Determination of Young´s modulus and yield stress

Standard techniques like the Oliver & Pharr method, continuous stiffness measurement (CSM) and laser-generated surface acoustic wave (LSAW) measurement have been applied for the determination of the Young's modulus of porous materials. In order to investigate relevant film thicknesses for technological applications (300-500 nm), one has to prove the validity of each applied method. Generally, indentation experiments yield effective moduli which have to be corrected for the substrate influence. To achieve this, one has to adapt a fit function to measured values which are limited to a narrow range.
The film thickness limit for SAW was estimated to be 150nm, currently. Thinner films can not be analyzed by using a two-parameter fit of the dispersion curve for the elastic modulus and density (Fig.1), since straight lines were obtained [1].

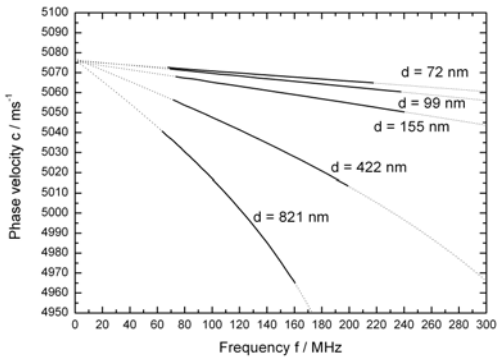

Fig. 1 Dispersion curves for mesoporous silica with different thickness from Laser acoustic test

In that case either density or elastic modulus will be obtained from the measurement, pre-conditioning the knowledge (or assumption) of the other parameter.

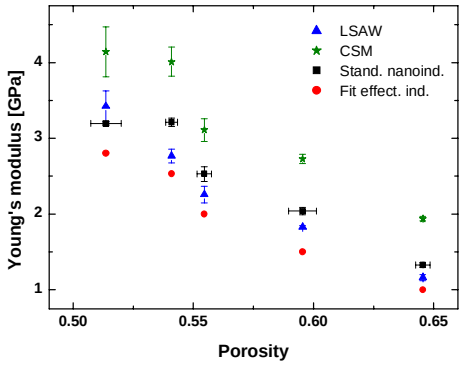

Fig. 2 Young´s modulus obtained by different characterization methods for mesoporous silica films on Si dependent on their porosity

Summarizing, the results for the Young's modulus of all applied methods are not consistent (Fig.2).
However, since those standard methods were developed for homogeneous materials it is not surprising that these methods have given different values for the same sample.
Since this dilemma has been known for about 3 years, we have developed a new concept comprising two methods for the determination of yield stress of porous materials which both are based on Pharr's concept of the effectively shaped indenter (Fig.3) [2].

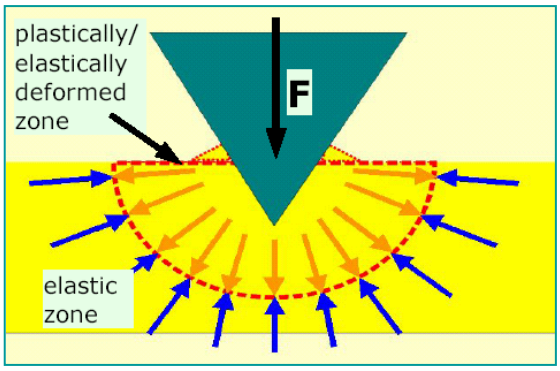

Fig. 3 Concept of the effectively shaped indenter: compressed zone acting as an effectively shaped tip onto the layer

Thus, the complete analytical solution of the elastic stress field during indentation with a body having symmetry of revolution can be obtained [3,4]. The spatial maximum of the von Mises stress is considered as yield stress (Fig.4).
The investigations showed that Pharr´s concept can be used for the analysis of thin porous films with spherical indenters only if small amounts of plastic deformation occur.

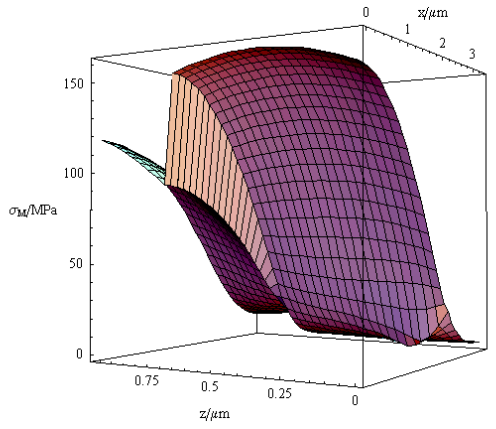

Fig. 4 von-Mises stress distribution for a MSQ-based film with porosity of 30 vol%

In the case of higher amounts of plastic deformation (i.e. when using a smaller indenter radius), the extrapolation method after [5] was applicable.
We conclude that the material behaviour of rather soft films during penetration of the indenter should be analyzed by using a pressure-dependent Young's modulus. Then a better consistency of indentation data (Young's modulus and yield stress) will be obtained. The Young's moduli which give consistent values in relation with the yield stresses are smaller than the results of all other methods, see Fig.2 ("Fit effect. ind.").

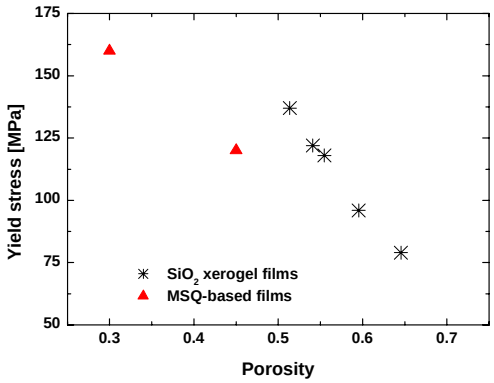

Fig. 5 Yield stress for mesoporous silica and MSQ-based dielectrics

Another interesting result applying the above mentioned model including pressure-dependent Young´s modulus was the nearly linear relation found between yield stress and porosity for mesoporous silica films (Fig.5). This is a useful input for modelling the load on porous films during chemical mechanical polishing.

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H_2-strip processes and their impact on porous low-k materials

Blaschta, Frieder; Schulz, Stefan E.; Rennau, Michael
TU Chemnitz, Center for Microtechnologies

1 Introduction

At present, H_2-strip processes are used to remove photoresists on low-k materials. Unfortunately, pure hydrogen based processes are not very promising due to low removal rates. Different admixtures like nitrogen, helium or argon are known to improve the situation. In every case the impact of stripping on low-k materials has to be examined. The pro's and con's of admixtures have to be balanced with respect to efficiency of stripping and worsening of electrical and mechanical properties.

2 Experimental

Porous MSQ (p-MSQ) with k value of ~ 2.2 was chosen as ultra low-k (ULK) material. As potential cap layer, a spin-on hard mask (SOHM; slightly porous SSQ; k~3.2) has been introduced to fulfil the demand for hardmask (HM) and CMP stop, especially for a post-CMP burnout approach. To investigate the impact of stripping on the properties of dielectric layers, investigations with non-patterned films (blankets) were done.
The plasma assisted stripping process was studied by means of an Advanced Strip Passivation Chamber (ASP) of APPLIED MATERIALS. Downstream microwave plasma of hydrogen with admixture of nitrogen or helium at a pressure of 1 Torr was used. The temperature was typically 300° or 400°C and the magnetron was adjusted to 750 or 1000W. The shrinkage was ellipsometrically measured by change of thickness. The electrical properties, i.e. k-value, leakage current and field break down (FBD) were measured by Hg-probe. FTIR spectra were used to support the investigation.

3 Results

Fig. 1a and 1b show typical SEM images for a 200s stripping with H_2/N_2 and H_2/He mixture, respectively. The admixture of nitrogen impacts the rate of stripping positively; only small residues remain, which have to be removed by a following wet clean step.

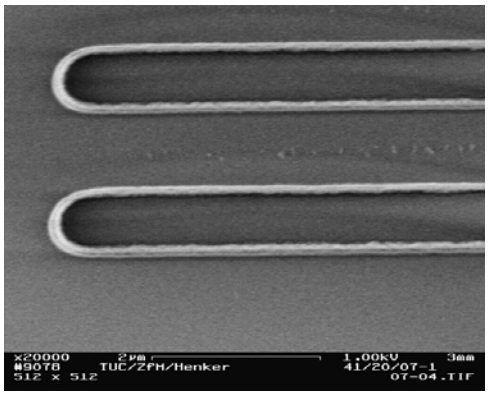

Fig. 1a: Stripping of photoresist with H_2/N_2 mixture, 200s

The admixture of helium reduces the rate of stripping and thus leads to increased stripping times.

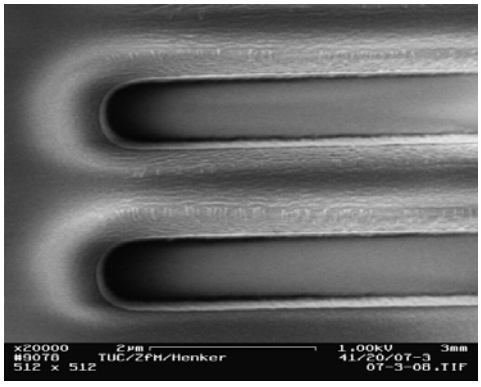

Fig. 1b: Stripping of photoresist with H_2/He mixture, 200s

The admixture of N_2 and He not only removes the resist, but it also causes a substantial shrinkage of porous hard mask and low-k material (Fig. 2a and 2b).

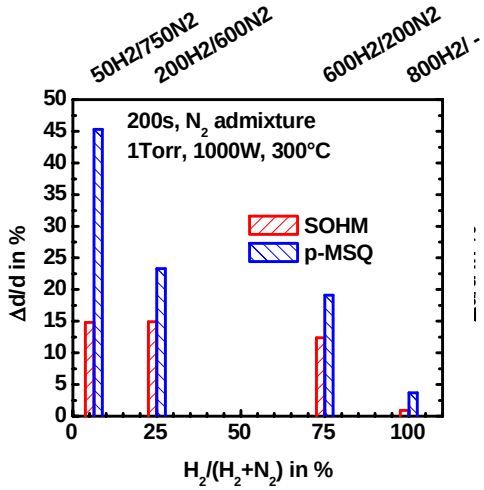

Fig. 2a: Impact of gas mixing ratio H_2/N_2 on shrinkage

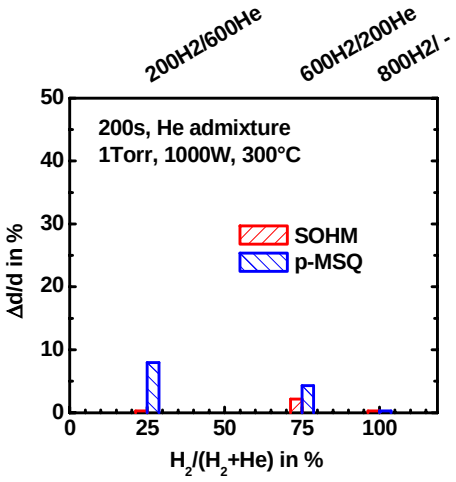

Fig. 2b: Impact of gas mixing ratio H_2/He on shrinkage

Fig. 3a and 3b show the corresponding impact on the k-value. The stronger impact of H_2/N_2 mixture on shrinkage and k-value is explained by a decrease of Si-CH_3 bonds at 1272 cm^{-1}, as seen by FTIR spectra [1].

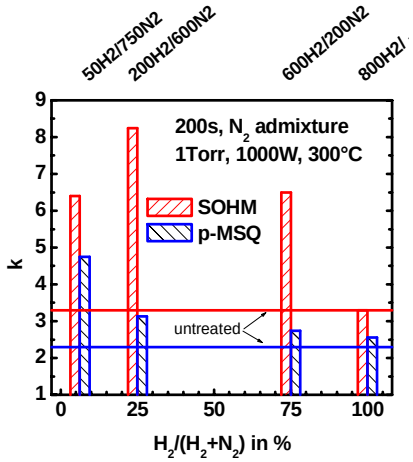

Fig. 3a: Impact of gas mixing ratio on k-value (H_2/N_2)

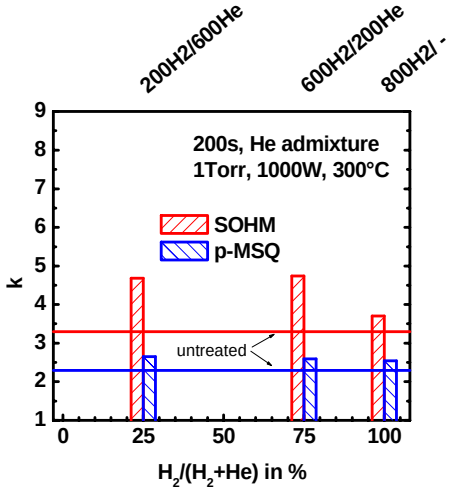

Fig. 3b: Impact of gas mixing ratio on k-value (H_2/He)

4 Summary and Outlook

Two potential admixtures to hydrogen at elevated temperatures have been studied. The N_2 admixture increases rate of stripping, but mechanical and electrical properties will be worse. He admixture presents hardly an impact, but rate of stripping is too small.
It is proposed to use a H_2/He mixture for stripping, where a small amount of N_2 increases the rate of resist stripping. A first promising result [2] is seen in Fig. 4. Further investigations, especially the impact on mechanical and electrical properties are under investigation.

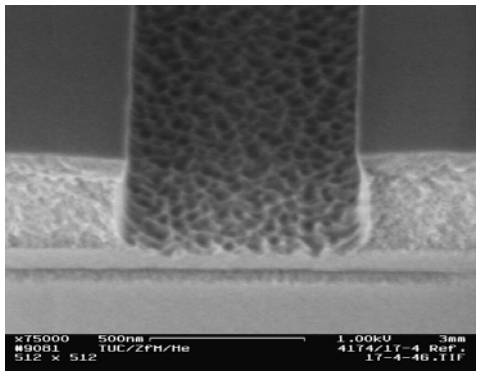

Fig. 4 : Photoresist removal with H_2/He with a small amount of N_2

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Air Gap formation using wet etch of sacrificial PECVD SiO_x

Schulze, Knut; Schulz, Stefan E.; Gessner, Thomas
Chemnitz University for Technology, Center for Microtechnologies, Chemnitz

1 Introduction

Low-k and even ultra low-k (ULK) dielectric materials have been successfully developed with respect to their electrical properties. Numerous CVD or spin-on materials are available fulfilling the required permittivities. The integration of these materials in interconnect technology caused much more problems associated to process compatibility (sidewall damage, interface to barrier materials, pore sealing), thermal properties, mechanical (CMP, packaging) and chemical stability and up to now the ITRS roadmap targets for interlevel metal insulator k-values (bulk/effective) have been softened annually [1].
Air Gaps technologies, using air (k=1), as interlevel dielectrics, seem to be increasingly potential candidates [2] for lowering the interlevel effective k-value and a simultaneous avoidance of integration issues, known especially from porous low-k materials. The different strategies for Air Gap formation, known form literature, can be allocated in two general techniques – void formation via non-conformal PE-CVD deposition and usage of sacrificial layers between metal lines [3].

2 Sacrificial wet etch Air Gap techniques and experimental results

At the Center for Microtechnologies, an Air Gap approach has been developed which uses PECVD SiO_x as a sacrificial dielectric within conventionally produced copper damascene architectures. The removal of the dielectric was done by buffered 40% HF solution.
Two integration schemes for Air Gap generation have been tested. Both approaches use a patterned hard mask on top of the structures. The initial film stacks of the prepared Cu lines embedded in SiO_x dielectric are shown in Fig. 1 (a) and Fig. 2 (a). SEM micrographs of both integration schemes types devoid of any HF treatment can be seen in Fif. 3 and Fig 4.

The “mask” approach is illustrated in Fig. 1. The surface underneath the wet-etch-mask consists of copper, diffusion barrier material and CVD SiO_x. Choosing a wet-etch-mask material, resistive against buffered HF, only the inter metal dielectric (IMD) will be the removed media, starting from the wet-etch-mask windows, depending on treatment time. In that case, the patterened hard mask defines exclusively the areas of HF impact. Etch window dimension is limited by the minimum feature size of lithography. In Fig. 2, showing the “spacer” approach, PECVD SiO_x spacer material at the side wall of all metal lines, permits self aligned HF access to PECVD SiC coated areas of the sacrificial IMD. This is additionally restricted by a patterned hard

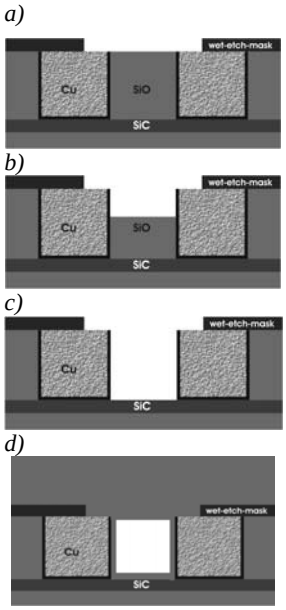

Fig. 1: “mask” approach (a) after CMP and "wet-etch-mask" patterning; (b) partially wet etched; (c) fully removed USG dielectrics (d) sealed air gap structures (using non-conformal CVD)

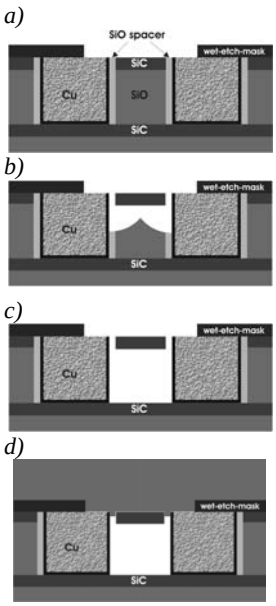

Fig. 2: “spacer” approach (a) after CMP and "wet-etch-mask" patterning; (b) partially wet etched and spacer opening; (c) fully removed USG dielectrics (d) sealed air gap structures

mask (comparable to the “mask” approach), which improves furthermore the mechanical

stability of the prepared stack. Nevertheless independent from the hard mask pattern geometry, the etch slots are defined by the spacer width, well adjustable in a sublithographical range. The applied hard mask material was PECVD SiC, because PECVD SiC or even SiCN provide an excellent etch selectivity during wet etch (no attack in buffered HF).

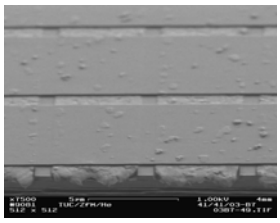

Fig. 3: 45° tilted SEM micrograph of "Air Gap via mask" preparations before wet etch

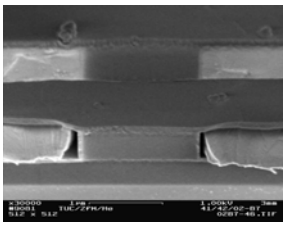

Fig. 4: : 45° tilted SEM micrograph of "Air Gap via spacer" preparations before wet etch

A sealing and encapsulation of these structures by non-conformal CVD process has still to be proven. Schematical results of this process step are presented in Fig. 1 (d) and Fig. 2 (d). Afterwards a multilevel interconnect system can be built by alternation of dense or porous dielectric for via-level and Air Gaps for metal-level.

a)

b)

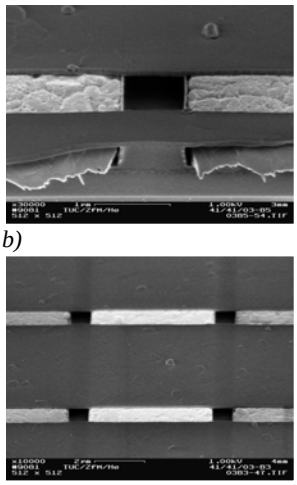

Fig. 5: 45° tilted SEM micrograph of "mask" approach; partially (a) and fully (b) removed dense dielectrics

a)

b)

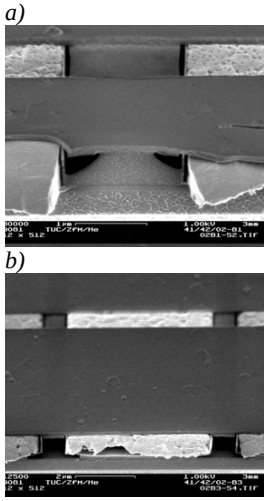

Fig. 6: 45° tilted SEM micrograph of "spacer" approach; partially (a) and fully (b) removed dense dielectrics

The application of the presented patterned hard masks offers the opportunity of well defined local etch attack. Leaving dense dielectrics in uncritical areas, ensures adequate mechanical and thermal properties. This is a good basis for an application to multilevel metallization (especially successful CMP treatment) and sufficient reliability.

Fig. 5(a) and Fig. 6(a) show the results of partially removed dense IMD of both approaches. Spacer opening mechanism and formed spacer slots can be clearly seen. Finally dense IMD material PECVD SiO_x is totally removed and air gaps are fabricated, see Fig. 5(b) Fig. 6(b).

Delaminations or other significant defects were not observed. Adhesion and stress behaviour of copper lines and hard mask materials are evaluated as the most important properties, to secure successful multi layer preparations adapted from these approaches. Concerning to the sealing of the hard mask windows and associated redeposit, we expect a higher potential of the Air Gaps via spacer approach for multilayer preparations, because of the good adjustability of the spacer slot widths (<10nm) in a sublithographical range.

Effective k-values and capacitances of both approaches including real node geometries are determined and finally compared to electrical measurements (see next report: *Electrical Characterization and Simulation of Air Gap structures*).

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4 Acknowledgement

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Electrical Characterization and Simulation of Air Gap structures

Schulze, Knut; Schulz, Stefan E.; Rennau, Michael; Gessner, Thomas
Chemnitz University for Technology, Center for Microtechnologies, Chemnitz

1 Introduction

Air gaps are very promising for a sufficient device performance of the 45 nm node CMOS technology and below. In this paper two similar sacrificial layer air gap approaches developed at TU Chemnitz, called "mask" and "spacer" approach, are electrically characterized by FEM simulations and k_{eff} is extracted for future node geometries. Furthermore, electrical measurements have been verified. Both Air Gap integration schemes, including preparation results are shown more in detail in the report before: *Air Gap formation using wet etch of sacrificial PECVD SiO.*

2 Electrical characterization and FEM simulation results

First electrical measurements at comb structures (see Fig. 1) showed a significant reduction of capacitance during cavity formation by buffered HF impact and PECVD SiO IMD removal, see Fig. 2. The introduction of air gaps caused a capacitance reduction of more than 50% in comparison to the base structures having dense

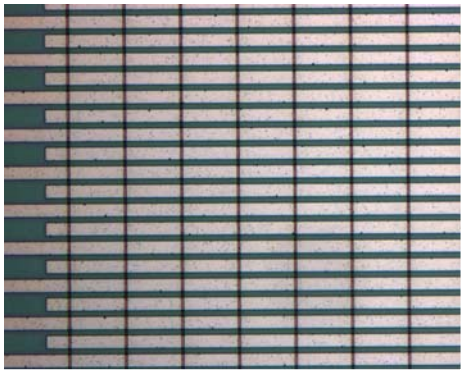

Fig. 1: Light microscopical top view of comb structures and patterned PECVD SiC wet etch hard mask

PECVD SiO_x as IMD material. Due to electrical FEM simulations referring to this, a capacitance lowering of 55% for these preparations were

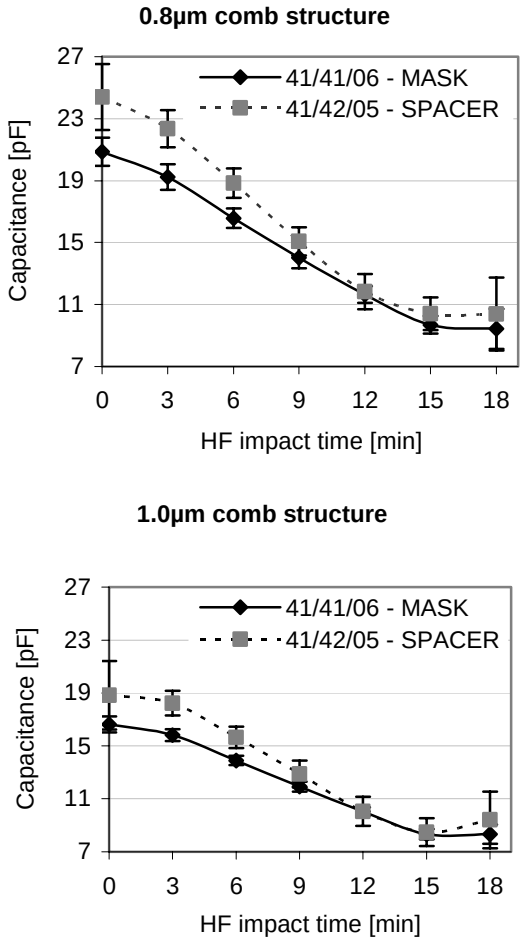

Fig. 2: Graphs of measured capacitances during time dependent cavity formation by removal of dense PECVD SiOx dielectrics for two different comb structure spacings (0.8µm, 1.0µm) and both approaches ("mask" and "spacer")

expected. Both results match sufficiently. Detailed information of measured and simulated values for two comb structure geometries is shown in Fig. 3. It is assumed, that the deviations between simulated and measured values are mainly caused by geometrical tolerances between simulation models and real prepared structures. Independent from this, the ratios of the capacitances at all preparation states (measured and simulated) between both comb structures fulfil the expected value of 0.8. This

caused by the wire spacing ratio of 1.0µm to 0.8µm. The following k_{eff} were finally extracted by FEM simulation of both approaches: $k_{eff\text{-}MASK}$~2.3 and $k_{eff\text{-}SPACER}$~2.4. Further simulations should show, what k_{eff}-values are achieved for real node geometries (65nm down to 22nm node)

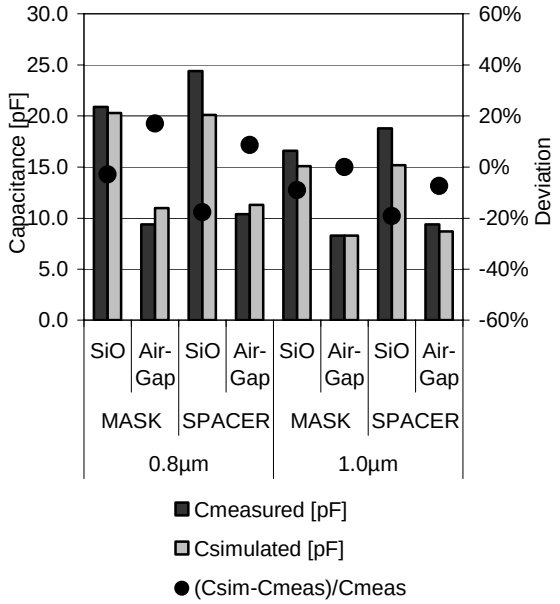

Fig. 3: Measured and simulated capacitances of two comb structures (0.8µm and 1.0µm comb spacing) including the deviation occurring between both values

of all metal levels by these two approaches. The requirements of the ITRS 2004 (International Technology Roadmap for Semiconductors) are shown in Fig. 4. The results of the FEM simulations according to this are illustrated in Fig. 5. A thickness of 10nm and a k of 5.0 were used for all PECVD SiC functional films (hard mask film, cap- and etch-stop-layer). Obviously the portion of PECVD SiC in comparison to the whole volume of the structure, particularly air, increases with proceeding node. Because of this, k_{eff} is finally degraded. If a scaling factor of 0.7 is used for thickness reduction of functional films node by node (comparable to the general node scaling factor), then k_{eff}-values are almost identical for each air gap approach and all future nodes. Otherwise air gap performance is definitely influenced by the k of the functional films. Several simulations were done with a range of k-values of 3 up to 7. The interaction of both parameters, k and thickness, are exemplarily shown for the "mask" approach and 65nm node dimensions in Fig. 6. These simulations were performed for both air gap approaches and all node geometries down to 22nm node.

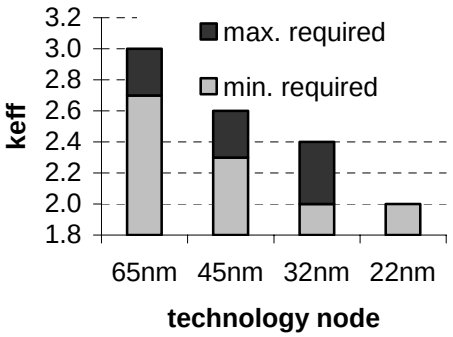

Fig. 4: Interlevel metal insulator effective dielectric constant requirements of the ITRS 2004 for future technology nodes

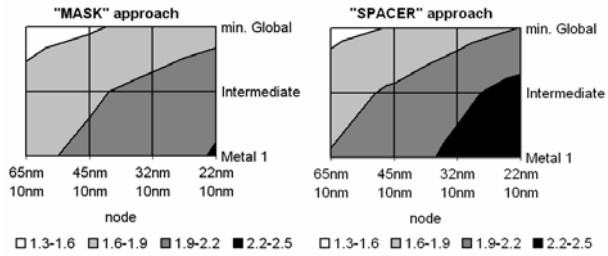

Fig. 5: FEM simulation results of k_{eff} for both air gap approaches "mask" and "spacer" using real node geometries; thickness of all functional film 10nm and a k-value of 5.0

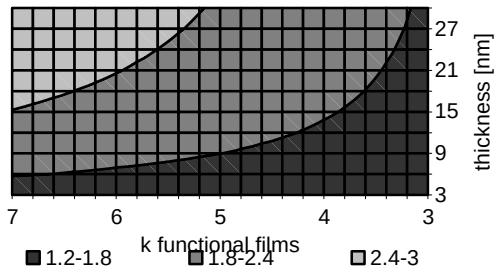

Fig. 6: FEM simulation results k_{eff} of "mask" approach with 65nm node geometries and varied k-value and thickness of the functional films

3 References

[1] K. Schulze, S.E. Schulz, M. Rennau, T. Gessner, Proceedings of the Advanced Metallization Conference (AMC) 2005, to be published

4 Acknowledgement

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“Spin on metal” – preparation of metal Cu and Ag films by spin coating of metallo-carboxylate and formiate precursors for electronic applications

S. Frühauf[a]; A. Jakob[b]; Y. Shen[b], S. E. Schulz[a]; T. Gessner[a,c]; H. Lang[b]
[a]Center for Microtechnologies, TU Chemnitz, Germany
[b]Institute of Chemistry, TU Chemnitz, Germany
[c]Fraunhofer Institute for Reliability and Microintegration, Chemnitz, Germany

1 Introduction

At present metal films for interconnect systems with Damascene architecture, especially Cu films, are mainly deposited by electroplating, PVD or CVD. Since miniaturization of electronic devices is going on, size of structures shrink and gap-fill will be more challenging. Spin on deposition has a clear benefit regarding gap-fill capability, since it is a non-structure-conformal deposition process.
The research on this field of “spin on metal” bases on the development of metallo-carboxylate and formiate compounds, mainly developed by Prof. Lang´s group at the Institute of Chemistry as well as provided by BASF AG, Ludwigshafen.

Benefits of spin coating

Radial forces on the precursor liquid during substrate spin cause flattening nearly independent of the underlying substrate structure by a plane liquid film. Trenches and holes are filled supported by capillary forces. During film drying a slightly wavy surface develops due to different shrinkage in regions with big and small structures. It can be removed by a subsequent polishing process. Holes or cracks in the filled regions can be avoided by using appropriate precursor properties and thermal treatment. This concept, which has been already successfully applied to interlayer dielectrics and shallow trench isolation in semiconductor technology with very small gaps and high aspect ratios, is investigated for deposition of metal Cu and Ag films.

2 Results for Cu and Ag metal film deposition

Several solutions of solid and liquid Cu(I)- and Ag(I)-complexes were deposited on silicon wafers (for example see Fig. 1), which had previously got a film stack isolator/barrier in order to avoid metal diffusion into the isolator material.

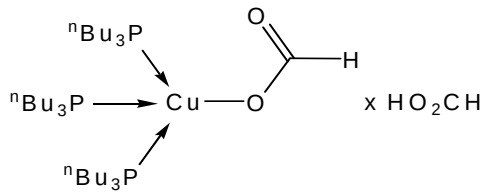

Fig. 1 Cu-complex Tris(tributylphosphan)Cu(I)-formiate

The deposition was carried out under Argon flux, since the precursors had limited stability in air. After spin coating the wafers were transferred to the furnace. Best transformation conditions were found at high heating rates and under forming gas as furnace ambient. A scheme for thermal transformation of a Cu precursor containing the main transformation steps into metallic Cu is shown in Fig. 2.

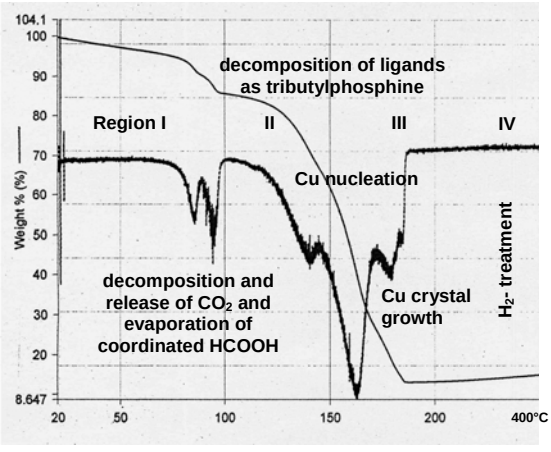

Fig. 2 Transformation steps schematically assigned to the TGA/DTA curve of a typical Cu-precursor

The obtained copper films were annealed in hydrogen stream at 400°C in order to remove traces of oxygen, detected especially on the surface of the copper grains after furnace anneal, which inhibit grain growth. The obtained blanket films with thickness between 200 and 300nm

were measured with four-point probe testing to have a film resistivity of less than 3μΩcm.

This value is higher than that for pure copper (~1.8μΩcm) and has to be improved in future, but is a competitive one compared with Cu films from other deposition processes. Fig. 3 contains the SEM image of a blanket spin coating deposited Cu film after final hydrogen anneal. Fig. 4 demonstrates the high quality of the film composition profile analysed by AES.

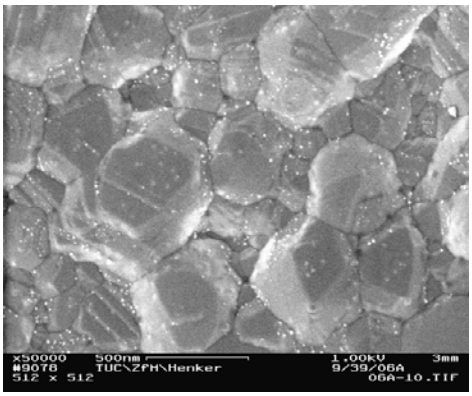

Fig. 3 Grain morphology of pure Cu film, SEM image

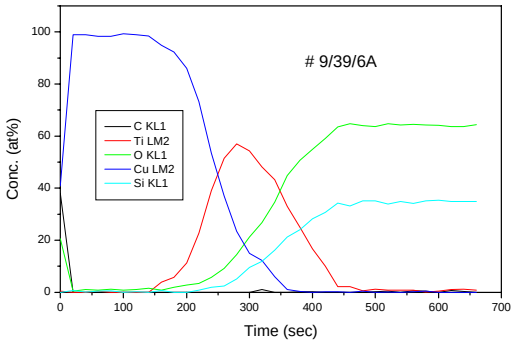

Fig. 4 AES depth profile of the film stack of Fig.3

Similar procedure for deposition was applied for Ag precursors. The best resistivity obtained for these films was ~3.4 μΩcm, which is consistent with the detected slight porosity. Nevertheless, the results are promising, since the final hydrogen anneal was not yet applied to the Ag films [1]. After achieving the milestone for blanket Cu metal films by spin coating the further research is focused on optimization of the precursor properties for gap-fill. The gap-fill capability of the precursor depends on viscosity and wetting, but most important is the Cu yield of the precursor. If Cu yield is too small, than the benefit of the spin coating method regarding non-structure-conformability has been lost and the gaps can not be filled with enough material like demonstrated in Fig. 5.

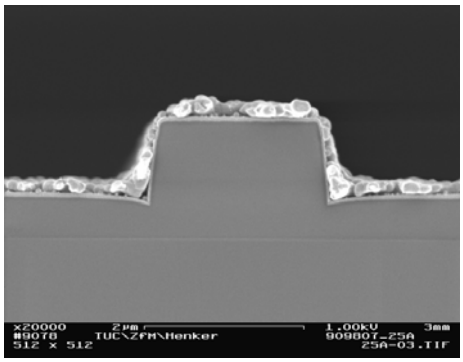

Fig. 5 SEM image of the Cu layer laid over the substrate structure

For a precursor with a higher Cu yield the gap-fill was promising. The non-structure-conformal deposition is shown in Fig. 6. Therefore the feature gap-fill capability of the precursors will be a key for the success of “spin on metal” deposition into high aspect ratio patterns.

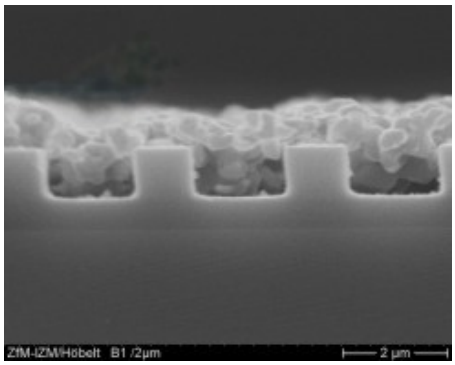

Fig. 6 SEM image of a Cu filled SiO_2/TiN pattern prepared by spin coating

3 Acknowledgement

Main part of this work was carried out under industrial contract with BASF AG, Ludwigshafen. We thank Dr. L. Wittenbecher, Dr. J. Sterzel and Dr. K. Tiefensee for the fruitful scientific discussion and cooperation.

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CMP process development for Cu/low-k based interconnect systems

Gottfried, Knut [1]; Schubert, Ina [2]
[1] FhG-IZM Chemnitz, Department Micro Devices & Equipment
[2]TU Chemnitz, Center for Microtechnologies

1 Introduction

The necessary integration of low-k dielectrics in actual and future device generations is one of the big challenges in microelectronics currently and in the coming technology nodes. The significantly lower E-modulus of low-k dielectrics (compared to traditional used materials) lead to a lower mechanical strength in general. This challenge will be intensified, if porous materials are considered. Beside that, low-k dielectrics show lower adhesion to other materials. These issues have to be taken into account especially for Chemical Mechanical Polishing (CMP) processes, as commonly used in Cu interconnect fabrication. Consequently, Cu and barrier CMP needs to be developed and adapted, when applied together with porous low-k materials. Selected results related to that topic will be described in the following.

2 Experimental

Low-k stacks based on two different low-k materials were considered within these investigations. Material #1 is a porous methylsilsesquioxane based material (p-MSQ). Material #2 is a porous silicon oxide (Aerogel). SiC was used as dielectric cap layer for both materials. Additional samples with a SiO_2 instead of low-k were used to determine principle CMP effects like dishing and erosion. Figure 1 summarizes the prepared layer stacks. The impact of pattern factor was investigated using test structures with and without additional dummy patterns (see figure 2).
An Applied Materials Mirra polisher and an On-Trak DSS 200 scrubber have been available for experiments. Commercialised and research grade consumables (slurries, pads) were provided by Rohm and Haas Electronic Materials as well as Cabot Microelectronics. All experiments were carried out using 6 inch wafers. Dishing and erosion were determined by profiler (Alpha Step 500) measurements on 10µm lines with 4µm space in between. Furthermore, polished samples were analyzed applying light microscopy and SEM inspection (plain view and cross section).

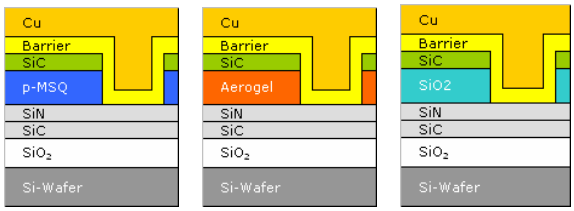

Figure 1 – Prepared layer stacks for polishing experiments: left p-MSQ, middle Aerogel, right silicon oxide

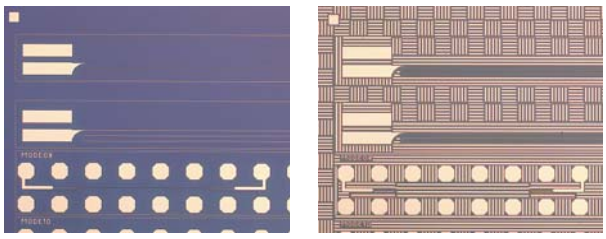

Figure 2 – Test patterns without (left) & with (right) dummy structures for the evaluation of pattern factor impact

3 Results

Dishing and erosion were investigated to figure out their dependence on down force and relative velocity. Low and uniformly distributed erosion was found (fig. 3a), except 3 outliers. Moreover, a slight dependence on down force is visible. However, differences are very small even for 1 psi and 2 psi. From relative velocity no clear dependence has been found (not shown here). For dishing an obvious dependence from location on the wafer is visible (fig. 3b). It is 4 to 5 times higher at the wafer edge than in the centre. Beside that, a distinct dependence on down force and relative velocity could not be observed.
Concluding from these results it can be assumed that the weak dependences of dishing and erosion from down force and relative velocity enable large process windows for the development of low-k compatible polishing processes.

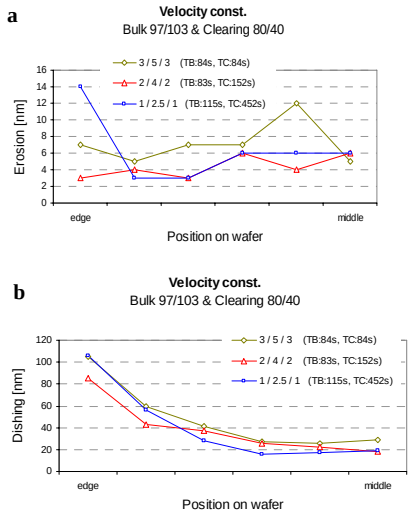

Figure 3: Erosion (a) and dishing (b) depending on down force (TB … polish time bulk, TC … polish time clearing, 3/5/3 … pressure membrane/pressure retaining ring/pressure inner tube, 140/130 … platen speed/head speed)

Polishing of low-k samples was performed to figure out process parameters, which enable a damage free polishing with very low dishing and erosion. The most critical parameter in that context is down force. For Cu polish down force was varied form 5 to 1 psi. Barrier polish was done at 1.5 psi. Platen and head speed were kept on recommended values due to their low impact on dishing and erosion.

For ***p-MSQ capped with SiC*** neither large area defects nor film delamination have been observed within light microscope, even for the samples polished at 5 psi down force. In very particular cases some small Cu residues have been detected at the wafer edge as well as in the middle. These residues could be removed by an over polish of 10 … 30 s. Using resistance measurements typically 1 … 3 shortcuts were found for 177 patterns in total, which gives an evidence for a complete material removal. Within SEM investigations for both layouts damages of the low-k stacks as well as film delamination have never been found, even for a down force of 5 psi. Exemplary results for 2 psi down force are shown in figure 4. Concluding these results and taking dishing and erosion into account down force should not exceed 3 psi for Cu-bulk removal. Cu-clearing should be done at a down force not higher than 2 psi. Barrier removal can be done at 1.5 psi because of the low film thickness.

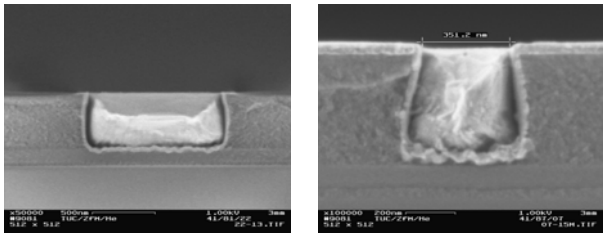

Figure 4: Cross section of p-MSQ samples capped with SiC after polishing at 2 psi down force

Aerogel capped with SiC has been polished in a first experiment at 2 psi down force which resulted in numerous defects. Thereby for the layout filled with dummy patterns the number of defects was lower. For further experiments down force were reduced to 1 psi, what is the lower limit of the equipment. Additionally, platen and head speed were increased to 140 rpm (upper tool limit) because higher relative velocities result in a lower shear force. However, the obtained results were very similar to those for 2 psi and lower speed. To study the failure mechanism more in detail plain view and cross section SEM records were taken from these wafers. From these records delamination of the SiC cap layer from Aerogel could be identified as failure mechanism. The Aerogel itself also seems to be attacked at some locations (fig. 5 left) however, a complete film loss has never been observed. In conclusion of these results it is to note: damage free polishing of Aerogel based low-k stacks could not be achieved with the current integration scheme, even at low down force. Ongoing work is necessary to find appropriate adhesion enhancing treatments before SiC cap layer deposition.

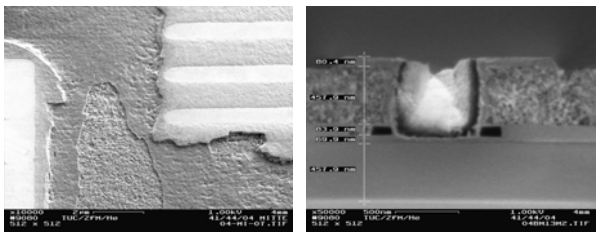

Figure 5: Aerogel/SiC low-k stack after polishing at 1 psi down force

Acknowledgement

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Simulation of Advanced PVD in Copper Damascene Process Flows

Hermann Wolf [1], Reinhard Streiter [1], Petr Belsky [2]
[1] FhG-IZM Chemnitz, Dept. MDE
[2] University of Essex, Colchester, Great Britain

1 Introduction

Ultra-thin films are needed as contact layers, barriers, and seed layers for the fabrication of present and future interconnection systems. As long as possible the deposition of such thin metal films is performed by PVD or IPVD. Conformal deposition in 3d structures of increasing aspect ratio as well as uniform bottom and sidewall coverage in the features across a large wafer diameter require a near normal incidence of the film-forming particles. This can be achieved by a combination of a long target-to-wafer distance, a high degree of (post-) ionization, and wafer bias voltages down to – 300 V. Because of their increased energy the ions undergo various interactions with the surfaces they hit: adsorption, reflection, and resputtering of one or more film particles. An optimization of process conditions has to be supported by a multi-scale simulation of particle generation, transport, and deposition.

Reactor-scale simulation comprises calculation of target emission spectra and simulation of transport at the reactor scale by the Monte Carlo (MC) approach to take into account the collisions of sputtered atoms with the background gas. In addition, the transport of ionized particles is affected by electromagnetic fields, especially during their motion across the plasma sheath. The goal of reactor-scale simulation is to obtain the profile of the film across the whole wafer disregarding the features, and the energy and angular distributions of particles arriving on the wafer. The results of reactor-scale simulation serve as input for feature-scale simulation.

Feature-scale simulation comprises simulation of transport at the feature scale using the MC approach and is influenced on how the impinging particles interact with the film surface. Such data can be obtained on the atomistic level using the molecular dynamic (MD) approach. The main goal of feature-scale simulation is to obtain the topography of the film in the features for various positions on the wafer and thus to be able to predict whether bottom and sidewall coverage of the features as well as conformity of the deposited films will be sufficient or not.

A general flowchart of the proprietary simulation tool T2 that covers the above mentioned issues is depicted in Fig. 1, showing the main components and their interaction

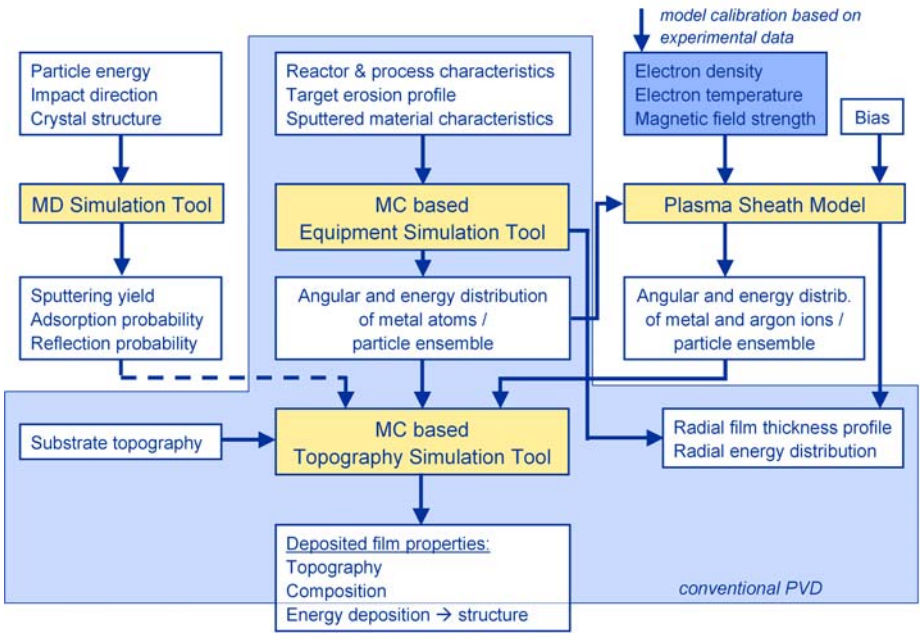

Fig. 1: Flowchart of the simulation tool T2.

2 Topography simulation

Simulation of seed layer deposition in dual damascene structures has been studied. Fig 2 shows the micrograph of such a structure with two adjacent vias and the shortest possible interconnect between them. Because the actual structures differ slightly between each other we use for simulation the 3d structure mapped on the right hand side representing the average topography

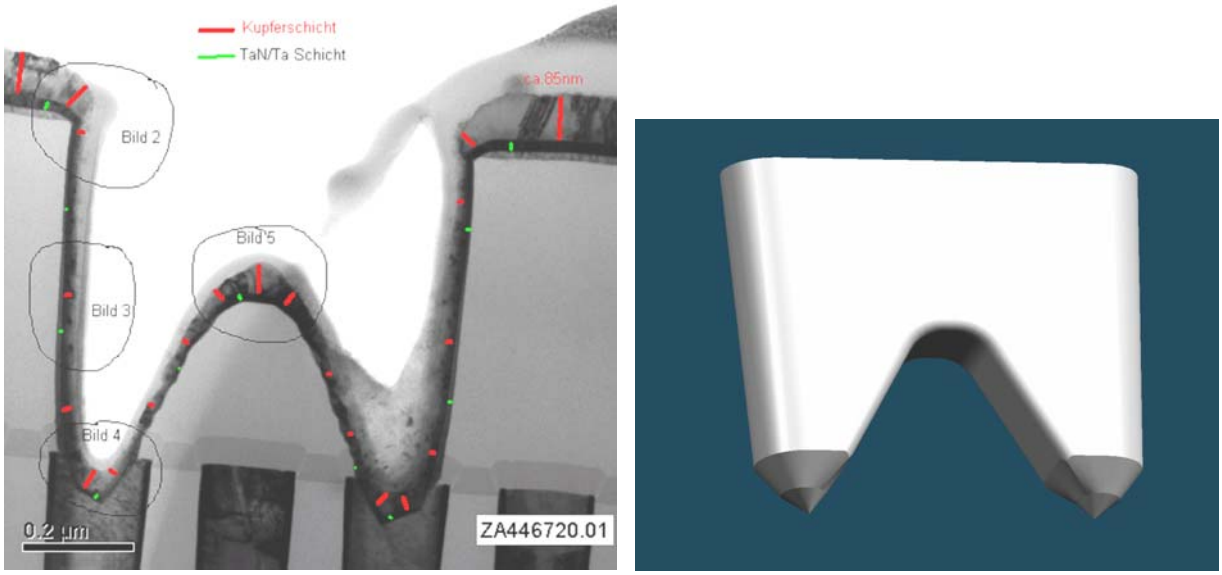

Fig.2: Micrograph of a dual damascene test structure (left) and 3d topography used for simulation (right).

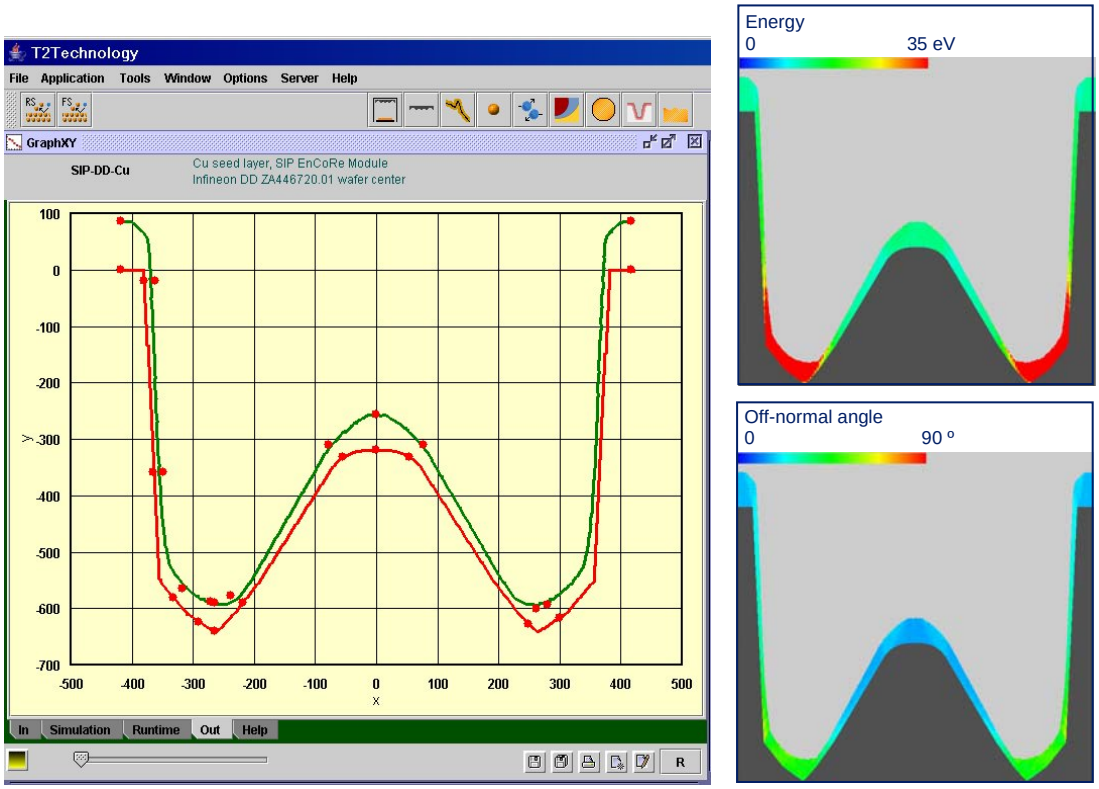

Fig.3: Simulation results: Comparison with measured film thicknesses (left), average energy (top right) and polar angle (bottom right) of copper particles impinging on the feature surface.

The simulation result is in reasonable agreement with film thickness measurements as shown in Fig 3. The colored representations show the locally averaged values of energy and angle of incidence of the metal particles hitting the surface. Colors in the lower diagram show a considerable amount of reflected and resputtered material in the valleys compared with direct deposition which dominates on the hill and in the more exposed field regions.

After having checked the consistency of the simulation, investigations are going on to identify limitations of PVD seed layer deposition and to look for means to push them further. It can be shown that a critical situation arises near the wafer edge because of the very thin films deposited in the shadowed regions. The diagrams in Fig. 4 show the simulation results for two different orientations of the damascene structure. The walls are completely covered, but the minimum film thickness is down to about two nanometers. Nevertheless, researchers from LETI were able to show that on such PVD seed layers void free filling of the structures is possible if electrochemical seed repair precedes the superfill step (NanoCMOS D4322). Thus, PVD seed with seed repair remains one possible option towards to the 45 nm node.

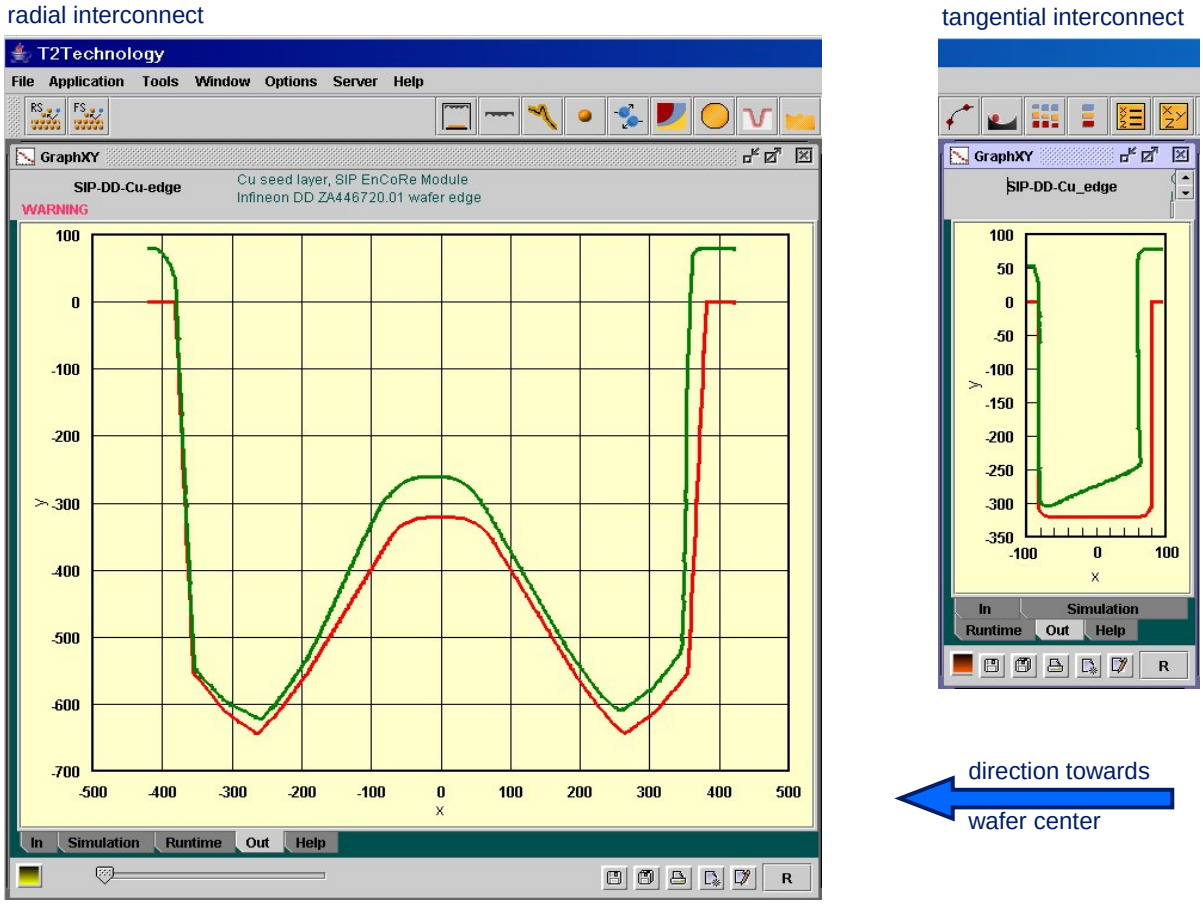

Fig.4: Simulation of Cu seed layer PVD in a damascene structure near the edge of a 200 mm wafer for different alignments of the feature. The "interconnect" has a radial direction in the left frame and a tangential direction in the right frame. The diagrams show a cross section of the 3d topography made at one of the mirror planes of the structure.

Different approaches to integrate patterned buried $CoSi_2$ layers in SOI substrates

S. Zimmermann[1], Q.T. Zhao[3], H. Höhnemann[4], M. Wiemer[2], C. Kaufmann[1], S. Mantl[3], V. Dudek[4], T. Gessner[1,2]

1) Chemnitz University of Technology, Center for Microtechnologies, 09107 Chemnitz, Germany
2) Fraunhofer IZM, Department Micro Devices and Equipment, 09126 Chemnitz, Germany
3) Forschungszentrum Jülich, ISG 1-IT, 52425 Jülich, Germany
4) Atmel Germany GmbH, 74072 Heilbronn, Germany

1 Introduction

The common integration of bipolar and MOS structures on SOI is hampered by conflicting requirements: Very thin silicon film is needed for fully depleted MOS but rather thick silicon film is necessary for the bipolar devices, to reach sufficient electrical properties. As a consequence, new ways to reduce collector series resistances of bipolar transistors must be found. A new technology, named Silicon on Silicide on Insulator (SSOI), consists of a thin silicon film on a buried silicide layer on top of a buried oxide (BOX). For the common integration of bipolar and MOS devices, SOI and SSOI areas must be available on the same wafer. For this, a new technology, which makes it possible to introduce patterned buried $CoSi_2$ layers on SOI substrates, will be generated.

2 Experimental

The developed SSOI technology combines the known cobalt salicide process [1] and a SOI wafer fabrication technology. We used two different process flows to prepare SSOI substrates, shown in Figure 1.

The first technology has some similarities with the BESOI process [2]. Aside from the cobalt salicide process, which includes metal deposition, RTA and selective etching steps, the wafer bonding and the removal of the start substrate are key technologies to produce SSOI substrates with device quality. We optimized the CMP polishing of the PECVD oxide to guarantee optimum bond results without failures in the bond interface. To remove the start substrate a two step process was developed, which includes wafer grinding and KOH etching with stop at the former buried oxide.

The second technology is based on the Smart Cut™ process [3]. An overview about the process flow is described in Fig. 1. A critical technology step is the hydrogen implantation through the structures on the wafer surface. We optimized the ratio between the thicknesses of the oxide hard mask and the cobalt silicide to get a homogenous deep distribution of the implantation layer.

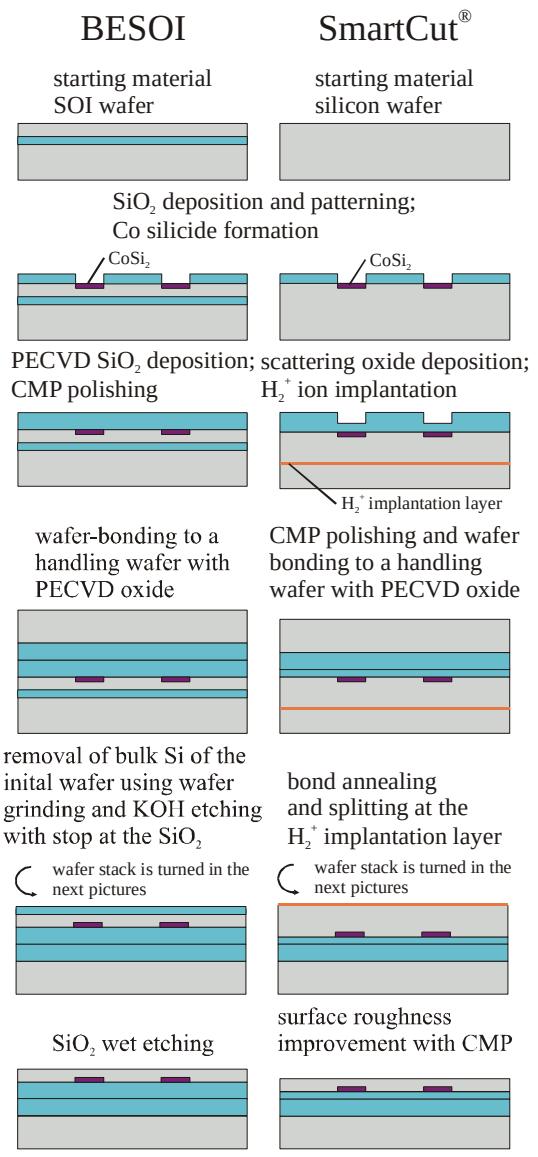

Fig.1. Process flows to prepare a SSOI substrate left BESOI method right SmartCut® variant

The cross sectional SEM image of the SSOI substrate, produced with the BESOI regime,

shows an homogenous silicon device layer with excellent surface quality (Figure 3). The cross sectional SEM image of the SmartCut® SSOI substrate (Figure 3) shows a failure free silicon layer with a large surface roughness.

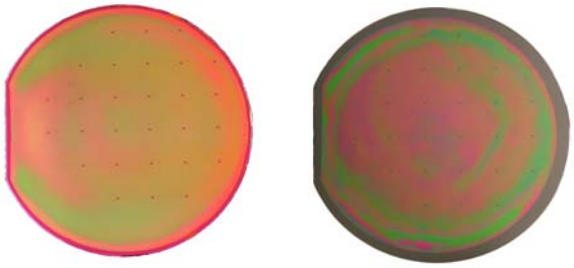

Fig.2. Finished SSOI Substrates right produced with the BESOI regime left prepared with the SmartCut® process

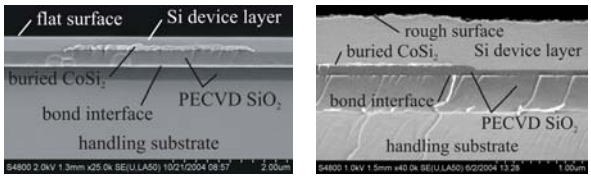

Fig.3. Cross sectional SEM images of SSOI Substrates right produced with the BESOI regime left prepared with the SmartCut® process without CMP surface roughness improvement

The main disadvantage of the robust BESOI technology is the expensive SOI start substrate. The SmartCut technology is more complex than the BESOI regime but has the advantage that the splitted wafer can used as handling substrate for the next SSOI process and the thickness of the silicon device film can be controlled in a wider range over the applied implantation energy.
Cobalt disilicide is used to form the SSOI substrate, because $CoSi_2$ has a high thermal stability, a low resistivity, and is easy to fabricate. The requirements, which were defined for the buried silicides, are somewhat different from the demands for these materials in the contact area. The resistivity of 16-17 µΩcm for our polycrystalline $CoSi_2$ films is sufficient for an application. Using the conventional cobalt salicide process the roughness of the $CoSi_2$/Si interface (R_{ms} ~ 11 nm) is far beyond the requirements of the device application, shown in Fig. 3 and Fig. 5 The potential of metallic layers between Co and Si during the silicidation to grow epitaxial $CoSi_2$ is reported in the literature for interlayers of titanium [4] and tantalum [5]. We tried to use these technologies to improve the interface roughness after the silicidation. The results are shown in Figure 4. All metallic and metal silicide layers have a thickness of 5 nm. A process with a titanium layer results in the same interface roughness like the conventional process. A tantalum interlayer yields no improvement in the surface roughness after the silicidation, just as a tungsten silicide and a molybdenum silicide layer. A 110 nm thick film of polycrystalline or amorphous silicon between Co and Si during the silicidation results in a clear improvement of the interface roughness. For polycrystalline silicon an excellent value of $R_{ms} < 1$ nm could be reached.

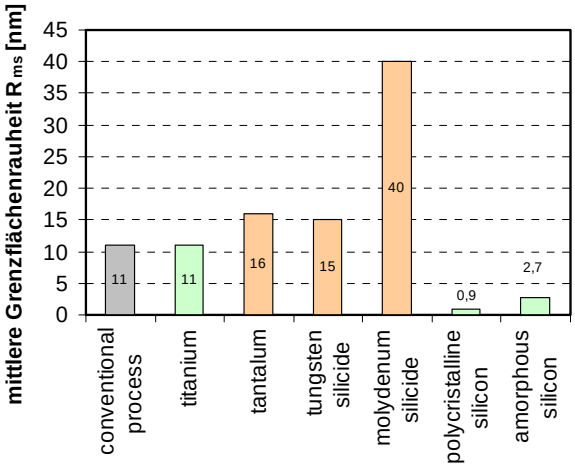

Fig. 4. Results of the roughness improvement of the $CoSi_2$/Si interface using different interlayers

Finally the thermal stability of the silicide films was in the focus of our investigations. We found that our $CoSi_2$ is thermally stable up to 1050 °C for 1 h.

3 Acknowledgement

This work was financially supported by the Federal Ministry of Education and Research (BMBF) in the framework of the project ISOSURF (01 M 3134 A).

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First principle calculations of silicon- oxynitride gate dielectrics

M. Bouhassoune, R. Janisch, A. Martinez-Limia, , E. Nakhmedov, E. Nadimi,
Ph. Plänitz and Ch. Radehaus
TU Chemnitz
Department of Electrical & Information Engineering, Opto- and Solid State Electronics

Abstract

A complete first-principle scheme is described to calculate the structural and electronic properties of high-k materials. Particularly, the DFT-LDA based ab-initio results for silicon oxynitride materials are reported. Comparison of the computed results with experimental data shows a good agreement.

1 Introduction

The reduction of conventional SiO_2 gate oxid thickness to a few atomic layers according to Moore's Law [1], the leakage current of modern microelectronic devices reaches a limit. High-k materials, with a higher capacitance per unit area as that of SiO_2, are suggested to replace the SiO_2 gate oxide. Besides the higher dielectric constant, k>30, new high-k materials must satisfy various requirements, such as the thermodynamic stability and high quality interface in contact with the Si substrate, large band offsets, higher than 1 eV, at both conduction and valence bands, small amount of dangling bounds at the interface, and defect charge densities as small as $\sim 10^{10}/cm^2$. All these requirements limit the choice of high-k materials. More prominent candidates that could potentially replace SiO_2 are HfO_2, ZrO_2, Al_2O_3, MgO, SrO, CaO, Y_2O_3 and La_2O_3 as well as their silicites and nitrided alloys, [2,3].

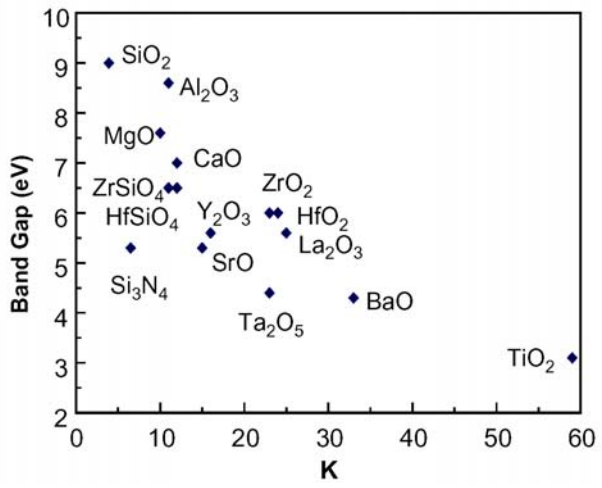

Fig.1: The dielectric constant against the band gap for various high-k dielectrics, (data from Ref.[3]).

A sharp decrease of the band gap by increasing the dielectric constant, eliminates well known high-k materials as TiO_2, Ta_2O_5 and Nb_2O_5 (see, Fig.1).

Silicon oxynitride (SiO_xN_y) materials are used as next-term gate dielectrics, but not as a future high-k material [1].

In this work we report our first principle results on SiO_xN_y compounds, that have been studied as a reference system for future investigations.

2 Computational methods for complex materials

The complex character of the structure and atomic bonds of ternary SiO_xN_y compounds need a complete and powerful ab initio tool of investigation.

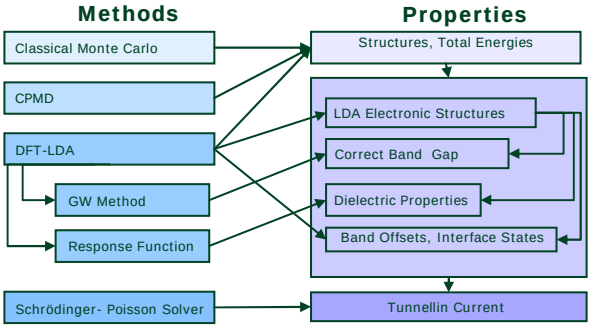

Fig.2: Schematic demonstration of the computational tool and the obtained material properties.

A central tool of our investigation is the Density Functional Theory (DFT) within the Local Density Approximation (LDA), (see, Fig.2). The well known underestimation of the band gap in LDA calculations, which is peculiar to all wide gap dielectrics, is corrected by means of the GW method.

3 Properties of Silicon oxynitrides

The computation of structural properties of SiO_xN_y are based on Mott's rule, which excludes dangling bonds in the structure. Calculations of various bond energies show that more favourable bonds in the structure are *Si-O* and *Si-N* configured in the tetragonal units with a central *Si* atom.

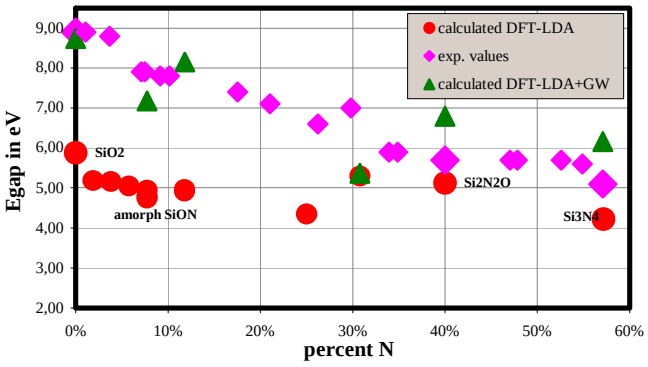

Fig.3: Dependence of the calculated energy gap of SiO_xN_y on the nitrogen concentration in comparison with the experimental data.

The optimized structural parameters as well as the electronic characteristics, such as the band gap, the dielectric constant and the atomic density of states (DOS), of SiO_xN_y compounds are calculated for different nitrogen concentrations within the DFT-LDA method by CPMD and ABINIT codes. The GW corrections rigorously update the LDA values of the band gap to the experimental ones, Fig. 3.

4 The interface to *Si*

Investigation of a *high-k oxide/ Si* interface at the atomic level will provide useful information to improve the electrical properties of a device. The site-projected DOS of a SiO_2 / *Si* interface, computed by the DFT-LDA method, is depicted in Fig. 4. Control of the DOS evolution with nitrogen concentration allows us to choose an optimal band gap minimizing the leakage current.

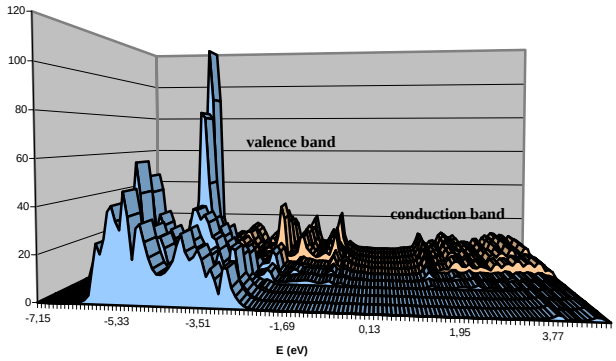

Fig.4: The DOS of a SiO_2 / *Si* interface. The deep orange region corresponds to the bulk silicon DOS. Contributions of the surface states occur at the boundary of the blue and orange regions.

5 Conclusions

The first principle computational methods are an important tool in the selection and prediction of new high-k gate oxides. Main parameters, which define the leakage current, such as band offset, dielectric constant, effective masses of an electron and hole can be accurately computed by means of the ab initio methods. Computation of the interface properties, such as the surface states and the dangling bounds, lattice mismatching and interface deformation potential etc., may provide an effective guidance for the high-k oxide selection and grown technology. The thermodynamic stability of high-k dielectrics in contact with a *Si* substrate, which is one of essential subject in the gate oxide selection, can be also studied by means of first principle methods.

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System Identification for MEMS devices

Wolfram, Heiko; Dötzel, Wolfram
Chemnitz University of Technology, Faculty of Electrical Engineering and Information Technology,
Department of Micro Systems and Devices,

1 Introduction

A major problem for the control design of Micro-Electro-Mechanical systems (MEMS) is the nonlinearity of the electrostatic field component. Several nonlinear (NL) approaches use a model of the nonlinearity to compensate the system's NL behavior. Therefore an exact representation of the nonlinearity is needed.
The linear system identification [1,2] is a well-established field. And even for NL systems exist a wide range of textbooks [3,4] and publications [5]. But the number of applications to identify MEMS is very minor.
A curve fitting, using the gradient method [6] as well as a NL optimization method [7] is performed to get the mechanical parameter estimates for an accelerometer. The Newton method [8] is used to identify the NL model of a MEMS optical switch, the nonlinear least-square method [9] fits the approximate solution by multiple time scales of a MEMS microphone and a neural network (NN) approach [10] is successfully applied to an accelerometer. The linear approach was also applied to an accelerometer system [11] to get an approximate model of the mechanical system.
It is known, that the NL optimization is sensitive to initial conditions and might stuck in a local optimum and the NN approach just gives a black-box model with no knowledge of the inner structure or dependences. Both identification methods need large numerical computation and also a large amount of data. Problematic for the NN system is the under-/overfit for a wrong network size, which results in a biased estimation or in an estimation with high variance [12]. On the other side the linear two-stage identification scheme is easy to apply, but does not give any information about the nonlinearity.
Therefore, a NL parameter identification algorithm, based only on the least square method (LSM) and singular value decomposition (SVD), will be applied and tested for applicability.

2 Mathematical Model

A MEMS can be described as a spring-mass system

$$\begin{aligned}&\left[-\omega^2 \boldsymbol{M} + \mathrm{j}\omega\{\boldsymbol{D} + \boldsymbol{D}_s(\omega, \vec{v}(\omega))\} + \ldots\right.\\ &\quad \left. + \boldsymbol{K} + \boldsymbol{K}_s(\omega, \vec{v}(\omega))\right]\vec{v}(\omega)\\ &= \vec{p}_{mech}(\omega) + \vec{p}_{el}(\varphi(\omega), u(\omega))\end{aligned} \tag{1}$$

with the inertial matrix $\boldsymbol{M}$, the damping $\boldsymbol{D}$ and stiffness matrix $\boldsymbol{K}$, consisting of constant mechanical and frequency dependent squeeze-film parts, the electrostatic load vector $\vec{p}_{el}$ the displacement vector $\vec{v}$ and a possible mechanical disturbance vector $\vec{p}_{mech}$.
The mechanical mirror system is basically an under-damped conventional PT_2-system

$$G_{mech}(s) = \frac{k_p}{T_p^2 s^2 + 2 d_p T_p s + 1}\ , \tag{2}$$

which has been used as the basis for the identification.
It is shown in literature, that this model represents the system accurately [13,14,15]. This is actually clear, since the introduced poles by the squeeze-film effect lie at very high frequencies for large gaps [16]. The complex poles from the mechanical system become in that case dominant and the system is under-damped.
The electrostatic moment can be obtained from the capacitance, where the total moment derives to

$$\begin{aligned}M_{el} = f(\varphi, u) = M(\varphi, u + V_R) + \ldots\\ - M(-\varphi, u + V_L)\ .\end{aligned} \tag{3}$$

3 Identification

The aim of the identification is to tune a mathematical description of the system, so that the performance function, based on the error between model output and system output will be minimal. Unfortunately, no universal identification approaches exist for NL systems, and also depend on a-priori knowledges. NL models can be classified into groups, based on the model structure and mathematical description [3]:

- *nonparametric models*, which need theoretically an infinite number of parameters (e. g. Volterra or Wiener series),

- *block oriented models* (e. g. Wiener or Hammerstein models),
- *parametric models*, which can be described by a finite number of parameters.

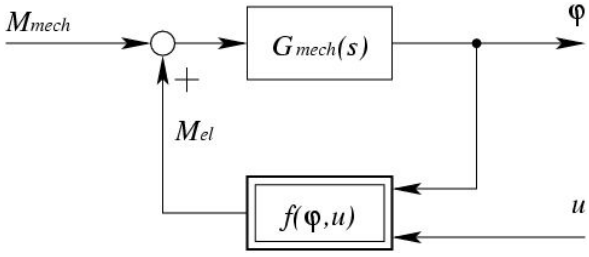


Fig. 1 System structure

Since the system structure for the micro-mirror is known (Fig. 1), a block-oriented parametric model is used for the NL approach. The mechanical Moment M_{mech} is considered to be negligible and set to zero, since it cannot be measured.

3.1 Mathematical Model

In this project we consider a single input-single output (SISO) system with the strictly proper linear time-invariant (LTI) part in Z-domain $G_{mech}(z^{-1}) = B(z^{-1})/A(z^{-1})$ and the nonlinearity will be described in Taylor series approximation

$$f(\varphi, u) \approx \sum_{l=0}^{r} u^l \sum_{m=0}^{q} \alpha_{lm} \varphi^m \,. \tag{4}$$

The bias part α_{00} is set to zero, since the NL function goes through the axis origin. Substituting the approximation (4) into the LTI-system gives the time series representation

$$\begin{aligned} \varphi(t) &= (1 - A(z^{-1}))\varphi(t) + \dots \\ &\quad + B(z^{-1}) f(\varphi(t), u(t)) \,. \end{aligned} \tag{5}$$

The series representation can be also written in vector notation form

$$\varphi(k) = \vec{\phi}^{\mathrm{T}}(k)\vec{\theta} \,, \tag{6}$$

where $\vec{\theta}$ is the parameter vector and $\vec{\phi}$ is the measurement vector with the measured in- and outputs at time step k.
All input-output measurements for $k = 0 \dots N$ can be written in the form

$$\vec{Y}_N = \Phi_N \vec{\theta} + \vec{E}_N \,, \tag{7}$$

where the vector $\vec{E}_N$ defines the noise representation in every sample.

3.2 Identification Task

The identification task is based on the LSM and SVD (see [17]). The task is done in the following steps:

- Collect input-output measurements $u(k)$ and $\varphi(k)$ for $k = 0 \dots N$.
- Form the output vector and compute the regression matrix in (7).
- Solve the least-square problem

  $\vec{\theta} = \Phi_N^{+} \vec{Y}_N$.
- Split up the estimated parameter vector $\vec{\theta}$ into the denominator estimates and product part of numerator and Taylor series estimates. Use the SVD to extract the factors from the product part.

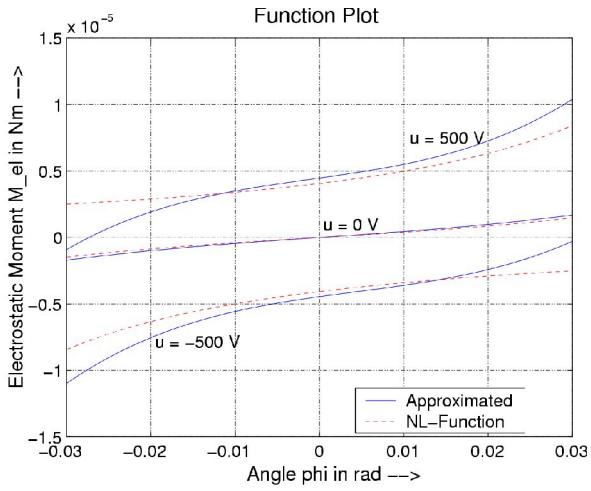
Problematic for the system identification is the possible correlation between the regression matrix Φ_N and the error $\vec{E}_N$, which results in a biased parameter vector. The *instrumental variable method* is one method to minimize the bias, assumed the system is stable.
Another drawback is the relative high order of the approximated nonlinearity to get acceptable results in a wide range of the measurements (Fig. 2).

4 Conclusion

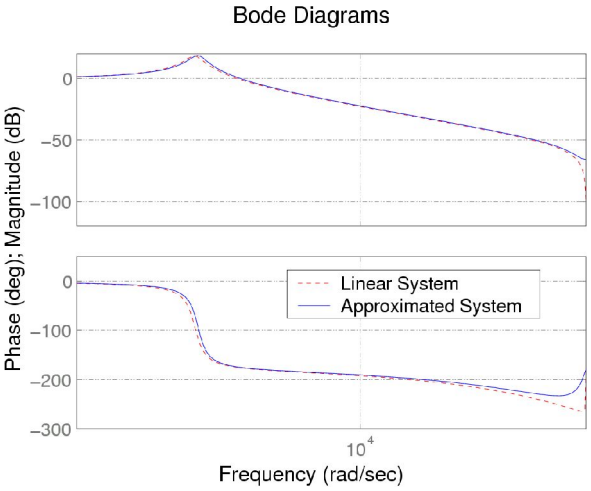
A nonlinear identification was provided for a feedback-nonlinearity, which depends on the input and LTI-system output. The simple regression model makes it possible to use the algorithm for on-line estimation.
Simulation has shown, that the order of the approximated nonlinearity must be sufficiently high to get a good agreement in a wide range with the electrostatic field function. One drawback is the power series approximation, which results in an infinite error in the two singularity points. The identification scheme is therefore only conditionally applicable to model the electrostatic moment.
The system under noise and the unstable system under feedback consideration as well as a practical implementation are left open for future tasks.

Acknowledgements

We want to thank the people at the Center for Microtechnologies (ZfM) at Chemnitz University of Technology, who designed and manufactured the actuator and other unnamed people, who were also involved into this project.



(a) Nonlinearity



(b) Normalized LTI-System

Fig. 2 Estimated system compared to the simulation model

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Multiparametric Simulation for MEMS Based on Automatic Differentiation and Series Expansion of Finite Element Codes

Kolchuzhin, Vladimir [1] **; Shaporin, Alexey** [1] **; Mehner, Jan E.** [2] **; Doetzel, Wolfram**[1]
[1]Chemnitz University of Technology, Department Microsystems and Precision Engineering
[2]Fraunhofer Institute for Reliability and Microintegration, Department Micro Devices and Equipment

1 Introduction

Finite element techniques have become state of the art for component design of MEMS. Physical effects related with electromagnetic, mechanical, fluid and thermal fields in complex devices are accurately described for static, harmonic and transient load situations [1].

Drawback of existing FE techniques is that those algorithms can only analyze a single model configuration with specified dimensions and physical parameters. In practice, designers long for the influence of parameter variations on the structural response in the same way as known from analytical methods. Currently, parametric models of complex devices are extracted by numerical data sampling and subsequent fit algorithms. Each sample point must be obtained by a separate FE run whereby the change of geometrical dimensions is realized by mesh morphing or remesh functionality. Usually one needs between several ten to some hundreds of sample data in order to capture the influence of design parameters accurately [1].

Firstly variational technologies have been applied for thickness optimization of shell structures in mechanical engineering [2] and CFD problem. Then this approach was used to microwave device design.

This article extends the approach to design of coupled domain systems (e.g. sensors and actuators) where strain energy and capacitance functions relate interactions between electrostatic and structural domains.

2 Description of Method

The key idea of the new approach, which account for parameter variations in a ***single*** FE run, is to compute not only the governing system matrices of the FE problem but also their partial derivatives with regard to design variables, Fig.1. Difficulties arose mainly from the fact that extraction of high order derivatives becomes numerical unstable and time consuming.

In contrast to symbolic differentiation which propagates mathematical functions, novel approaches make use automatic differentiation algorithms which process numerical values extracted at the initial position. Differentiation rules describe how to combine partial derivatives and binomial coefficients in order to form elementary mathematical operations and where to store results in 3-dimensional arrays [3]. Finally, Taylor vectors of the goal function can be expanded covering the system response in the vicinity of the initial position with regard to design parameters (Fig. 1).

3 Conclusion

Variational FE technologies have been implemented in MATLAB for eight and twenty node solid elements up to 6 geometrical parameters. The algorithms support linear static analyses of structural, thermal and electrostatic domains and sequential couple-field problem. Solid modeling, mesh generation and visualization of results data has been realized within ANSYS/Multiphysics.

Variational FE technologies have been applied on a comb cell. Capacitance stroke functions have been computed in six dimensions. It could be shown that Taylor series can capture the system behaviour only in a very limited circle close the evaluation point. Basic transformation of a Taylor to a Pade type approximation allows extending the acceptable parameter range as shown in Fig. 2. The levitation effect of comb cells could be captured well with order 2.

It offers a unique way for time efficient model parameter extraction of MEMS needed for advanced component and system design. Especially for case studies of different geometrical dimensions, sensitivity analyses of manufacturing tolerances and model export for electronic design automation one needs fast and

accurate models which capture the parameter relationship. Special emphasis was put on strain energy and capacitance extraction for reduced order modeling of MEMS. Benefits of variational technologies compared to ordinary data sampling procedures become obvious for multi-parameter problems. Response functions provide not only capacitance data but also the first and second derivatives needed for Maxwell force and electrostatic softening computations.

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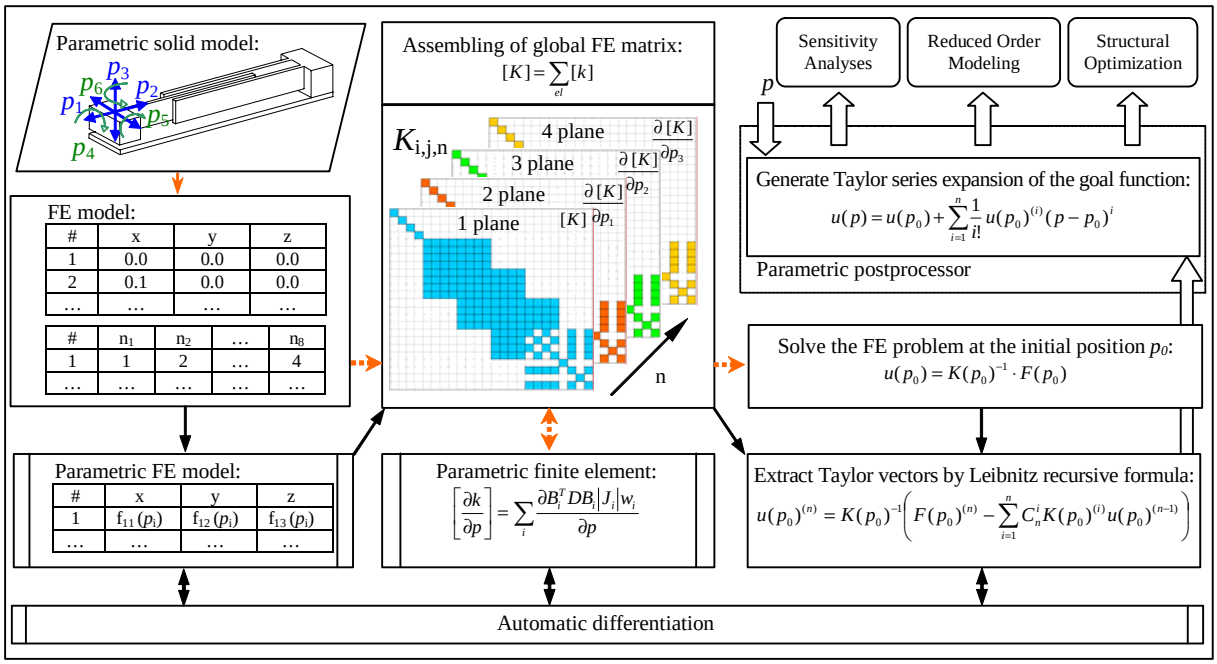

Fig. 1: Flow chart of parametric FE techniques.

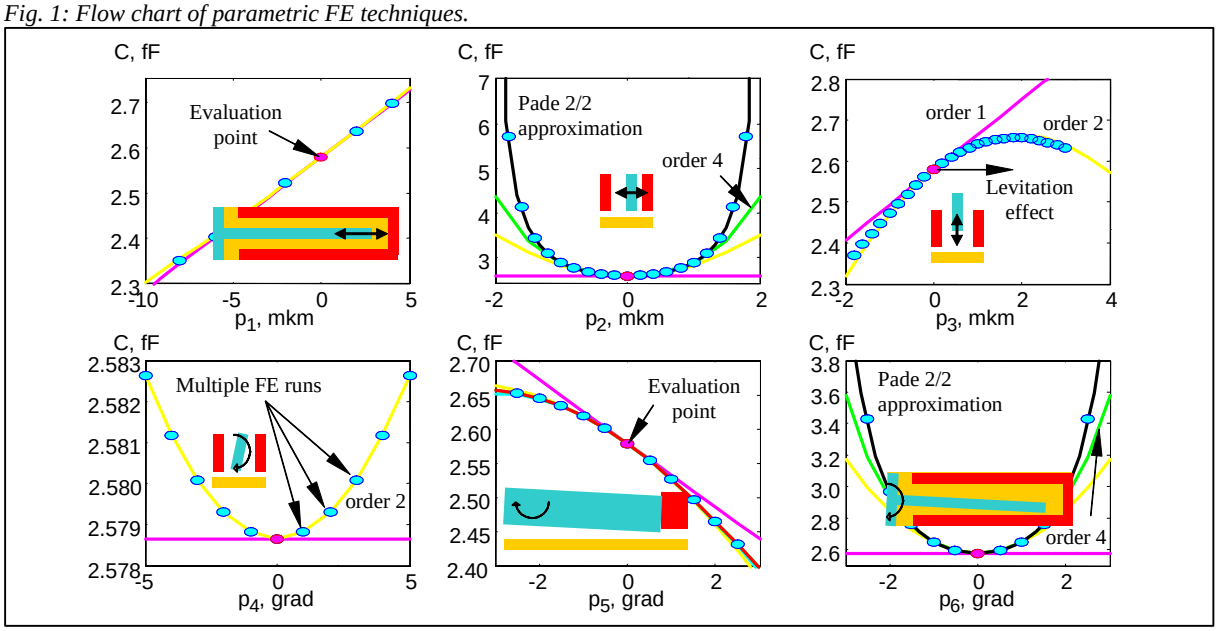

Fig. 2: Comparison of parametric FEM to sampling and fit method for 6-D capacitances functions of the movable finger.

Methods for model validation and wafer level test, PARTEST-Project

Kurth, Steffen[1] ; Hanf, Marian; Shaporin, Alexej[2]
[1] FhG-IZM Chemnitz, Abteilung MDE
[2]TU Chemnitz, Fakultät für Elektrotechnik, Professur Mikrosystem- und Gerätetechnik

1 Introduction

Fabricating MEMS devices, a major portion of cost is caused by the packaging in almost every case. A test of the dies to classify the chips is necessary before packaging where it is important to obtain reliable information about characteristics related to device specification, reliability or even to detect faults. Performing this tests sequently beginning at early fabrication steps provides additional information that is suitable for process control and fine tuning of process parameters. The difficulty is that a wide range of measurement data needs to be reduced to the small amount of information necessary to control the manufacturing process. To solve this problem, processes to adapt model parameters are still being developed and used. It has been found that resonant frequencies and resonant mode shapes of movable parts of MEMS devices are heavy influenced by geometric properties and by material parameters or even by faults like cracks or delaminations. Since resonant frequencies and mode shapes are known as most accurately measurable mechanical properties, the approach followed in the project PARTEST is focused on the the development of procedures for measuring it at wafer level and is aimed to derive geometric and material data from primary test results.

2 Modelling for test

When FEM analysis of the MEMS device has been done during its development, numerous simulation models are generated which describe the mechanical behavior at a large number of geometric locations and are available for test purposes later on. Since six degrees of freedom are allocated to each location, the results reflect the behavior of a mechanical system with a large number of degrees of freedom and resonance points. Practically, for such an ensemble of points, only a few degrees of freedom are significant and lumped element models are derived to utilize as model for test. The approach is to determine its model parameters on base of measured data and derive material and geometry parameters and process control data (Fig 1).

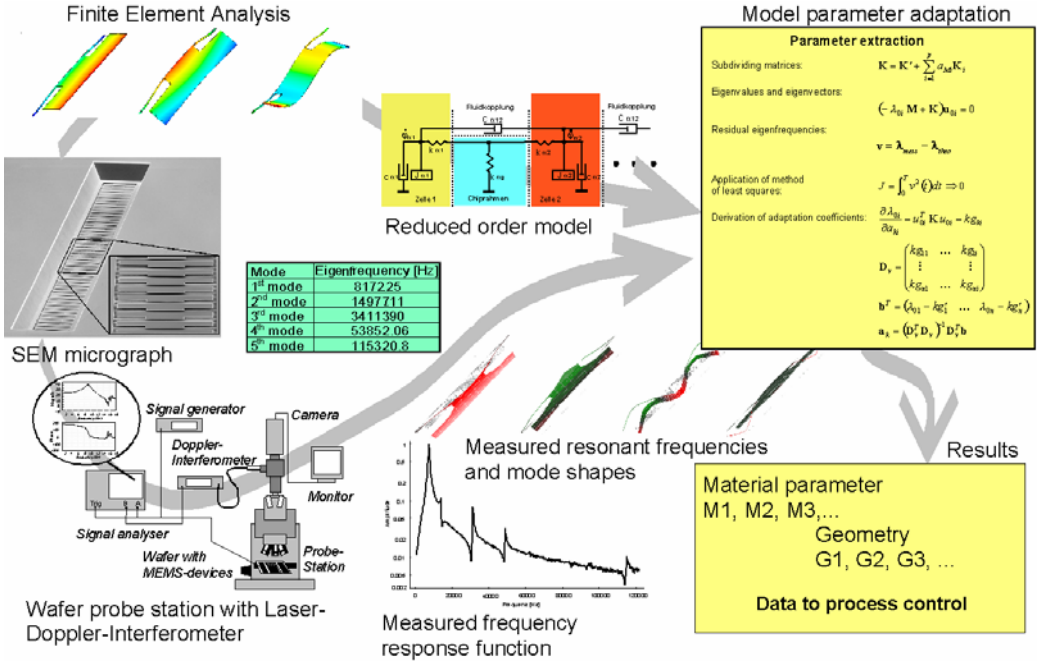

Fig. 1: Derivation of material and geometry data from measurement

3 Experimental Setup

The measurement data obtained from MEMS components mainly contains information on the dynamic deformation of movable components in form of time series or frequency response functions. A combination of a Laser Vibrometer and a Wafer Probe Station (Fig. 2) has proven to be an excellent technique for optically detecting the mechanical movement of structures within MEMS components.

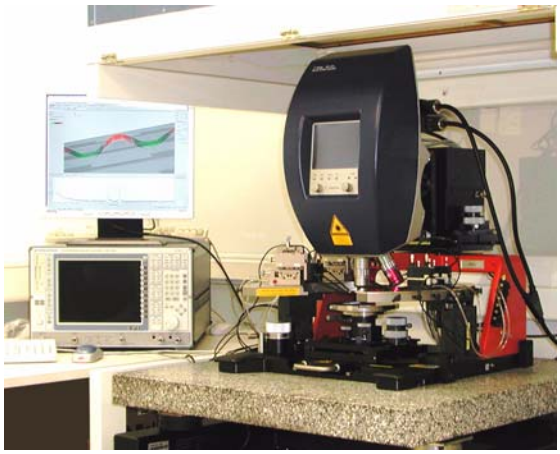

Fig. 2: Probe station with Polytec Microscope Scanning Vibrometer

Because of the optical sampling, the measurement procedure very little influence the MEMS device. The diameter of the laser beam on the test sample is in the range of a few micro meters, so that even very small structures such as single cells of micro mirror arrays can be tested. In parallel, experimental data is taken on MEMS components excited to induce mechanical vibrations. The vibration amplitudes are typically between several hundred pico meters and a few microns. Recording both the excitation signal and the resulting system response, provides the input signals from which the frequency transfer function is derived.

Finally, the parameters of the order-reduced model are adapted for a best fit to the measured system response data. To make the adaptation, the evaluation of resonance frequencies, the comparison with the model's eigenfrequencies and the least squares fitting method are used. The question regarding the accuracy of the simulation can be answered after a comparison between the calculated and the measured reaction, or by comparing the model parameters before and after adaptation. The adapted model is used to simulate the behavior of the MEMS components, taking various outline conditions as a basis.

4 Example

The MEMS device used for example here is sensitive for in plane vibration (Fig. 3) in a specific frequency range around a characteristic centre frequency [1]. It is a part of a sensor designed for vibration monitoring.

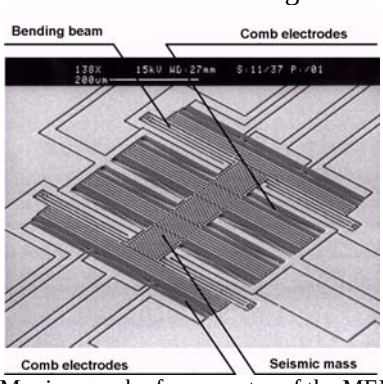

Fig. 3: SEM micrograph of a resonator of the MEMS accelerometer chip

The frequency response function in Fig. 4 shows an in plane resonance at 2.8 kHz. This information allows to identify the chip as known good die. Although the frequency selective dual axis MEMS accelerometer chip is expected to have only in-plane movements, the experience shows, that every in-plane device always has some out-of-plane movements, in this case at the resonant frequencies 17.7 kHz and 87.3 kHz (Fig. 4 and Fig. 5). It can be an indicator for tolerances in structuring the bending beams.

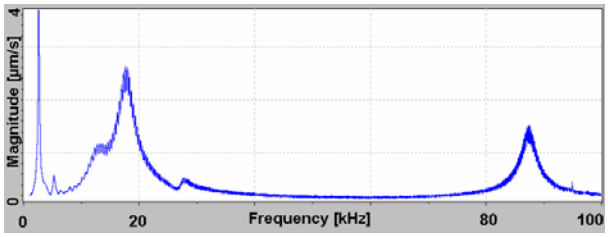

Fig. 4: Average of the magnitude transfer function of every measurement point

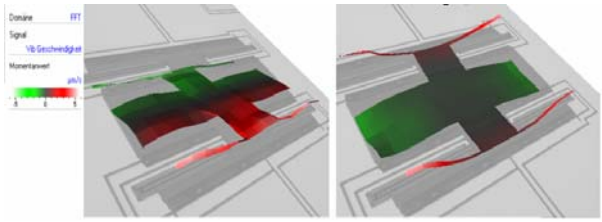

Fig. 5: Out-of-plane motion at 17.7 kHz (left) and at 87.3 kHz (right)

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Modeling and Simulation of MicroElectroMechanical Systems

Mehner, Jan[2]; Shaporin, Alexey[1]; Kolchuzhin, Vladimir[1]; Dötzel, Wolfram[1]; Gessner, Thomas[2]
[1]Chemnitz University of Technology, Chair Microsystems and Precision Engineering
[2]Fraunhofer-IZM Chemnitz, Department Microdevices & Equipment

1 Introduction

Modeling and simulation of MEMS is of vital importance to develop innovative products and to reduce time-to-market at lower total costs. Advanced design methodologies and a variety of software tools are utilized by the MEMS-Design group in order to analyze complex geometrical structures, to account for interactions among different physical domains and to capture the cooperative play of micro devices and connected electronic circuitry or signal processing units. Computer simulations provide a deep understanding of the device behavior and lead to systems with optimized performance parameters.
Activities of the MEMS-Design group are focused on software development for component and system simulations, on modeling and simulation of user-specific applications and practical Microsystems design for prototypes manufactured at our clean room facilities.

2 Microsystems Design

2.1 Design Flow for MEMS

Microsystems design exploits various analytical and numerical methods for virtual prototyping of MEMS. The entire design procedure consists of the following steps:

- High level system simulations,
- Process simulation and optimization,
- Component and device analyses and
- Simulation of the system behavior.

2.2 High level system models

The design process usually starts with high-level system models in order to find a preliminary layout and process sequence. Simplified models are utilized for analyzing the interactions of different components and to estimate and optimize the system performance. Results are physical properties such as stiffness data, desired eigenfrequencies or inertial masses, damping ratios and electrostatic coupling terms needed for electrostatic actuation and capacitive detection.

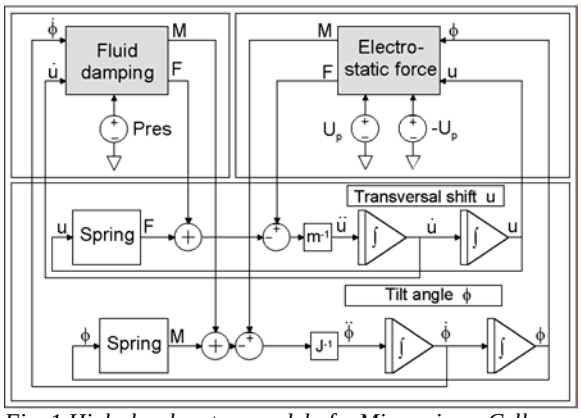

Fig. 1 High- level system model of a Micromirror Cell.

2.3 Process level simulations

Process level simulations are employed to obtain structural solid models from the mask layout and process description. Often, material properties depend on chosen process parameters and must be simulated likewise.

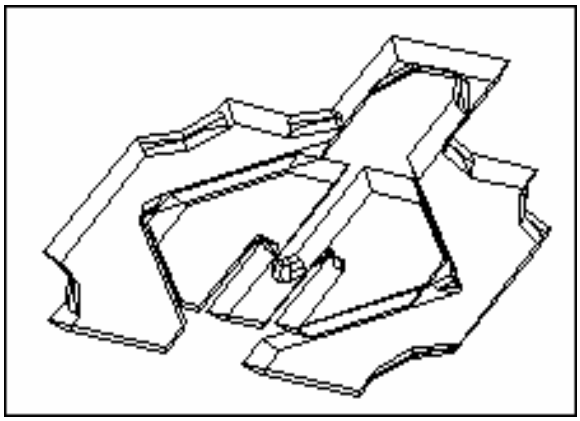

Fig. 2 Simulation of the anisotropic wet etching processes

2.4 Component and device simulations

The physical behavior of micro components is described by partial differential equations which are typically solved by Finite Element or Boundary Element Methods. Device level simulations are classified in *single domain* and *coupled field* simulations.
Single domain simulations are state of the art and can be realized by a series of commercial software tools. For example, Fig. 3 shows the mechanical response of an accelerometer at external loads in operating direction.

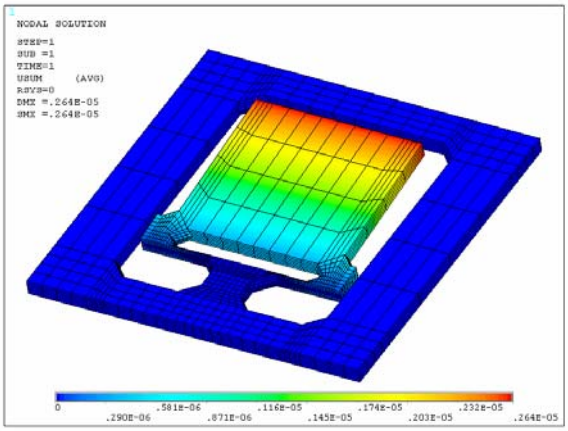

Fig. 3 Displacements at acceleration loads.

Coupled field simulations are vital to capture electrostatic-structural or fluid-structural interactions in sensors and actuators. Usually coupling algorithms must be adapted to special needs in order to account for non-linear effects which are inherent in MEMS devices.

Exemplarily, the performance of comb drive actuators is strongly affected by electrostatic fringing fields. This leads to levitation forces which lift the movable component out of the wafer plane. Eventually the forces may cause oscillations which disturb the system's response.

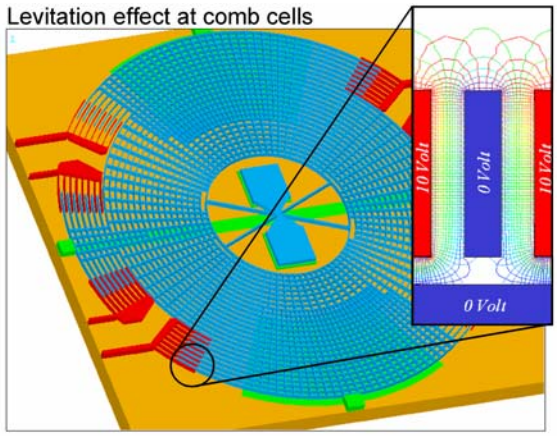

Fig. 4 Electrostatic fields at movable microcomponents.

2.5 System simulations of MEMS

Goal of system modeling is to study the relationship of microelectromechanical components, the controller unit and the electronic circuitry with the environment. Fig. 5 shows a Simulink model which was utilized to predict the image quality of an micro optical laser projection system.

Component models deployed for the mirror cells are directly extracted from finite element models by Reduced Order Modeling techniques. Reduced order black-box models relate essential input signals (e.g. electrode voltage) to output parameter such as tilt angle, plate warp or mirror temperature required for failure analyses.

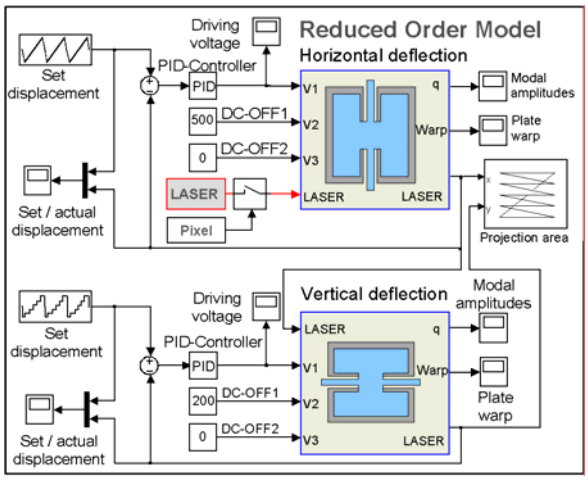

Fig. 5 System model of a micromirror laser display unit.

Fig. 6 shows the voltage time relationship needed for a saw-tooth like displacement function of image projection systems. In the lower part of Fig. 6, one can observe and evaluate signal distortions of the projected laser light.

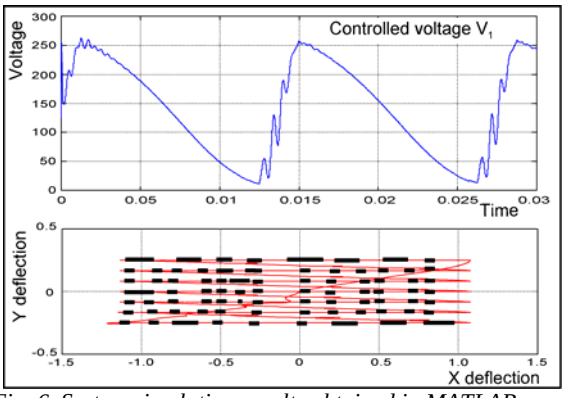

Fig. 6 System simulation results obtained in MATLAB.

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Microwave Phase Shifter in MEMS-Technology

Voigt, Sebastian[1]; Leidich Stefan[1]; Kurth, Steffen[2]; Hiller, Karla[1]; Gessner, Thomas[1,2]; Dötzel, Wolfram[2]
[1]Chemnitz University of Technology, Center for Microtechnologies
[2]Fraunhofer Institute for Reliability and Microintegration, Dept. Microdevices and Equipment

1. Introduction

The utilization of micro electro mechanical systems (MEMS) instead of conventional semiconductor devices can obtain fundamental improvements in microwave circuits with respect to signal attenuation and DC power consumption. Roadmaps and studies predict a wide field of application for RF-MEMS devices. The development of civil radar systems for automotive applications would strongly gain from the advantageous characteristics of RF-MEMS. Mechanical antenna scanning can be replaced by low loss electrical beam steering. MEMS Technology has great potential for the fabrication of low loss 360° phase shifters required for this application.
For the design of an analog tunable DMTL phase shifter the Silicon-Bulk Technology offers advantages compared to surface technologies. The capability of etching structures into the wafer allows the use of the extended tuning range concept described in [1] and to suspend all capacitive loads on one movable plate. This leads to wide range and homogeneous analog tunability [2].

2. A DMTL Phase Shifter in Silicon Bulk-Technology

The top view in Fig. 1 and the corresponding cross section in Fig. 2 show the two wafer concept of the phase shifter. Six beam springs suspend a structured movable plate forming 25 capacitive loads. In contrast to the referenced approaches [3] and [4] these loads are capacitively coupled to the ground plane of a high impedance coplanar waveguide (CPW) structure which is situated on the bottom wafer. The coupling capacitors change with the moving bridges. As can be seen in Fig. 2 the actuation electrodes on the bottom wafer are placed in a cavity to enhance the tunability of the functional bridge gap. The CPW is suspended on a 30 µm silicon membrane to reduce dielectric loss and to achieve a high impedance despite the high permittivity of silicon. Eqn. (1) shows the linear dependence of the phase shift Δφ from frequency f and unloaded line impedance Z_0.

$$\Delta\varphi = \frac{\omega \cdot Z_0 \cdot \sqrt{\varepsilon_{eff}}}{c_0} \cdot \sqrt{\frac{1}{Z_{\max}} - \frac{1}{Z_{\min}}} \qquad (1)$$

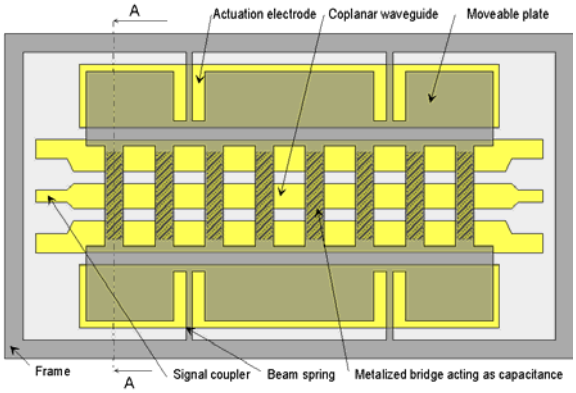

Fig. 1: Schematic top view of the phase shifter

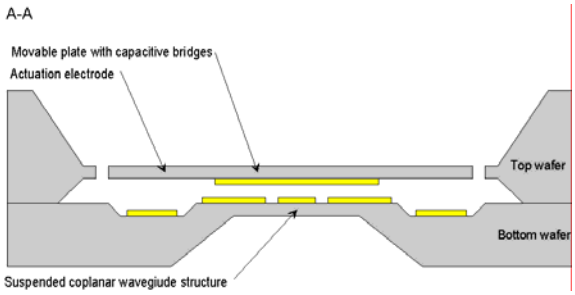

Fig. 2: Schematic cross section of the phase shifter

The design was optimized with respect to phase shift per line length. For the dimensions listed in Table 1 Method of Moment (MoM) and Finite Difference Time Domain Simulations (FDTD) predicted a phase shift of 17°/mm line length at 24 GHz by tuning the bridge gap from 4 µm to 2 µm. This corresponds to a return loss of better than 25 dB caused by the impedance mismatch. The designed maximum mechanical tuning range of the bridge gap is from 6 µm to 1 µm. Due to this wide range tunability of the bridge gap this phase shift can be increased if one can tolerate

more return loss [2]. The fabricated phase shifter consists of 25 bridges with a spacing of 300 µm and a width of 100 µm creating a line length of 10 mm. The maximum actuation voltage is designed to be 45 V with the constraint that the movable plate's maximum displacement due to gravity is 5% of the bridge gap. Considering the bulk conductivity ρ=3000 Ωcm of the 30 µm thick silicon membrane the simulated insertion loss for the coplanar waveguide is 0.8 dB/cm at a frequency of 24 GHz.

Table 1: Dimensions of the phase shifter

Bridge width	100 µm
Bridge spacing	300 µm
Number of Bridges	25
CPW center conductor strip width	175 µm
CPW ground gap	175 µm
Vertical adjustable bridge gap	6 µm - 1 µm

Using bulk micromachining the phase shifter has been fabricated in on-wafer testing variants and together with an asymmetric coplanar signal coupler [5]. The gold metallization is sputtered and structured by sputter mask and photolithography and the two wafers are joined by silicon fusion bonding. Fig. 3 shows a photograph of the fabricated device in an on-wafer measurement setup.

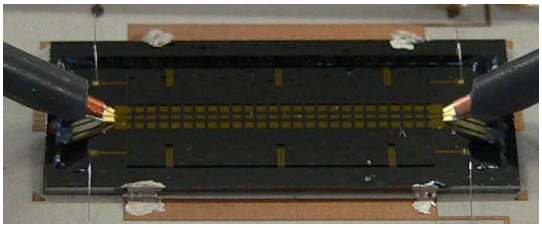

Fig. 3: Photograph of the fabricated device

3. Results

Within the first prototypes the two parts of the chip were manually assembled by epoxy gluing. They showed a continuously tunable phase shift and a promising RF-performance at different bias voltages over the full measurement range up to 40 GHz. The measured phase shift for a bias voltage of 60 V is 5.4°/mm. Fig. 4 shows the measured insertion loss of the phase shifter unit. It shows characteristic oscillations over frequency. This and the deviation of the phase shift from the expected value is caused by the manual gluing resulting in non perfect parallelism and planarity between the CPW transmission line and the capacitive loads. Considering the measured phase shift and the insertion loss for the matched condition occurring periodically in Fig. 4 the figure of merit would be about 50° phase shift per 1 dB insertion loss at 24 GHz. This is, yet, a very good value compared to competing structures and principles. Nevertheless, it is expected that current investigations, in order to improve the fabrication process, yield lower and non-periodic insertion loss and higher differential phase shift which will lead to a significant higher figure of merit.

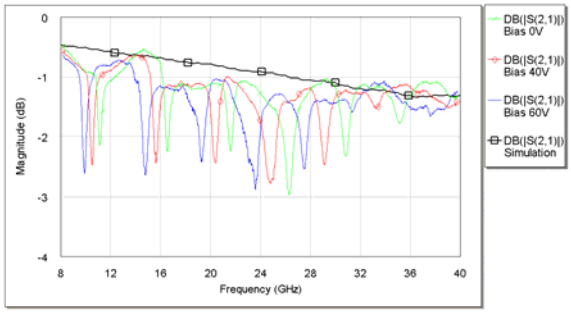

Fig. 4: Measured insertion loss of the phase shifter

The DMTL phase shifter principle was successfully implemented in Silicon-Bulk Technology. Using the advantages of this technology it has been shown that it is possible to fabricate high performance phase shifters for microwave frequencies. The figure of merit increases with frequency and the design is suitable to be scaled to higher frequencies.

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A MEMS friction vacuum gauge suitable for high temperature environment

Tenholte, D.[1]; Kurth, S.[2]; Geßner, T.[2]; Dötzel, W.[1]
[1]Chemnitz University of Technology, Faculty of Electrical Engineering and Information Technology, D-09107 Chemnitz, Germany,
[2]Fraunhofer IZM, Abt. Micro Devices and Equipment, D-09126 Chemnitz

1 Introduction

During the last years several new MEMS based vacuum gauges have been developed by scaling down conventional working principles [1].

Friction based vacuum gauges are commonly used for measurement of medium and low vacuum pressure. They are exerted for reference and calibration measurements. An utilization of the dependency of damping by ambient pressure in MEMS, customized for vacuum measurement, is described by Kurth [2], but besides this work there hardly deal any articles with this. We have contrived a new MEMS vacuum gauge based on gas friction. The advantages to actual implementations are significant smaller dimensions, therefore the sensitivity above 1 mbar, which is a limit for conventional friction gauges, is conspicuously higher. The sensor is suitable for high temperature environment up to 350° C.

2 Assembly and working principle

The working principle of the sensor is based on the pressure depending gas friction in narrow gaps. Methods for numerical analysis of this so called Squeeze-Film-Effect for two parallel, towards moving plates are presented by Veijola [3,4] and van Kampen [5].

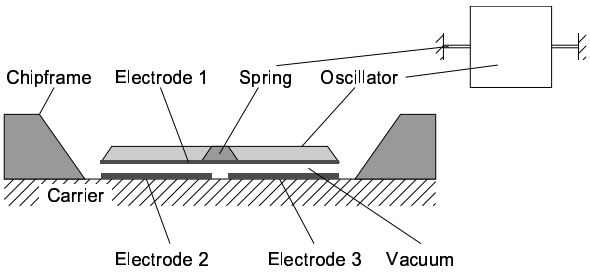

Fig. 1: Cross sectional view of the sensor

In this work we describe an electrostatically driven torsional Si resonator with a resonance frequency of about 500 Hz, which uses the dependency of damping on the pressure for determining the vacuum pressure. The structure of the sensor is shown in Fig. 1. It consists of a 30 µm thick, 4x4 mm² oscillating plate which is fixed in the centre of the chipframe by two 1,8 mm long torsional springs. The length of the complete chip is 9 mm, the width 8 mm and the thickness is 1 mm.

The resonator tilts due to an electrostatic moment caused by a driving voltage. After switching off the driving voltage, the damped oscillation

$$\varphi(t) = \hat{\varphi} e^{-\delta t} \cdot \cos(\omega_d t) \qquad (1)$$

of the resonator is measured either optically or capacitively. The decay constant δ of the system is determined by detecting the maxima of the oscillation and calculating their logarithm. These values are located on a straight line which gradient is the decay constant δ:

$$\ln \varphi(t) = \ln \hat{\varphi} - \delta t \qquad (2)$$

Depending on the pressure, the decay constant can be calculated from several 10 to several 1000 measured values, so it is possible to determine the δ with a relative deviation of less than 5% of reading.

3 Simulation

Because of the narrow gap of 10 µm between oscillator and opposite electrode, the Squeeze-Effect appears for a wide pressure range nearly up to ambient pressure. The molecular damping has not been considered for the simulation of the damping behavior of the sensor, because the Squeeze-Damping is dominant due to the narrow gap at the interesting pressure range.

The effective viscosity of the gas around the sensor is pressure sensitive. Owing to the pressure sensitive viscosity you get a likewise pressure dependent Squeeze-Damping β_{Sq} and Squeeze-Stiffness k_{Sq}.

On the basis of the developed simulation model it is possible to optimize the geometry of the sensor, so that the measurement range is as wide as possible and the sensor is sensitive nearly up to ambient pressure. According to the simulation

it is possible to reach a measurement range of about 7 decades.

4 Measurement results

Several measurements have been performed inside a vacuum system to investigate the damping behavior of the sensor under different conditions.

4.1 Measurements at room temperature

To determine the accuracy of the developed simulation model, the damping has been measured as a function of the ambient pressure.

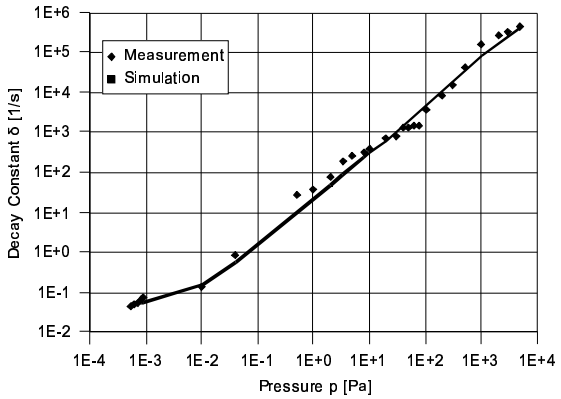

Fig. 2: Simulated and measured decay constant

Fig. 2 shows the results of the measurements in comparison with the simulated decay constant. As one can see, measurement and simulation match very well. The lower end of the measurement range results from damping mechanisms like thermocompression and intrinsic damping.

The measurements have been iterated once a week during one month to verify the repeatability, and no deviations have occurred.

4.2 Measurements at high temperatures

The contrived sensor consists only of glas, silicon and aluminium. All these materials are temperature stable up to temperatures of 400° C. Therefore it is theoretically possible to apply the sensor in high temperature environment up to 350° C.

To determine the behavior of the sensor at high temperatures, it has been fixed within a copper pipe which was heated at one end by a halogen lamp. Due to heat radiation inside the pipe one can assume that the temperature will be homogeneous after one hour.

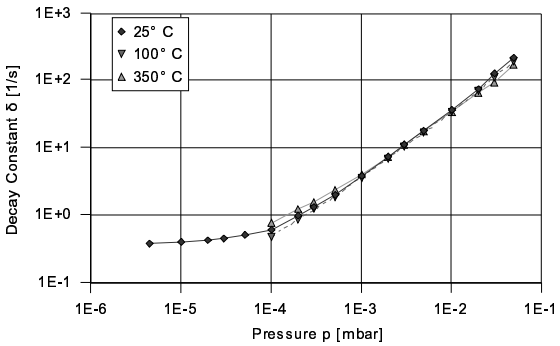

Fig. 3: Pressure dependency of the decay constant at various temperatures

Fig. 3 shows the pressure dependency of the decay constant at various temperatures. As to see, there is no influence of the temperature on the damping. The small deviations between the curves issue from the used reference Pirani-Gauge.

5 Conclusions

We have developed a new MEMS friction vacuum gauge with a measurement range of about 7 decades nearly up to ambient pressure. The sensor can be applied in high temperature environment up to 350° C without any modifications. Owing to the measurements so far, we assume that the relative deviation is less than 5% of reading.

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Coplanar Electromagnetic Signal Coupler for RF-MEMS Devices

Leidich, Stefan[1]; Voigt, Sebastian[1]; Kurth, Steffen[2]; Hiller, Karla[1]; Gessner, Thomas[1,2]
[1]Chemnitz University of Technology, Center for Microtechnologies
[2]Fraunhofer Institute for Reliability and Microintegration, Dept. Microdevices and Equipment

1 Introduction

The main focus of international research on RF-MEMS has been the development of actual MEMS functional elements, whereas less attention has been paid to comprehensive concepts considering assembly and packaging issues as well. Conventional wire bond techniques cause matching problems at microwave frequencies while flip chip connections require technologically challenging through wafer vias [1] and introduce high mechanical stress that might cause undesirable deflection and bending of the movable MEMS structure. An impedance matched asymmetric coplanar signal coupler, according to Fig. 1, connects the MEMS phase shifter to the printed circuit board non-galvanically. Epoxy adhesive mounting is used to fabricate self-contained RF-MEMS devices easy to integrate in many circuits.

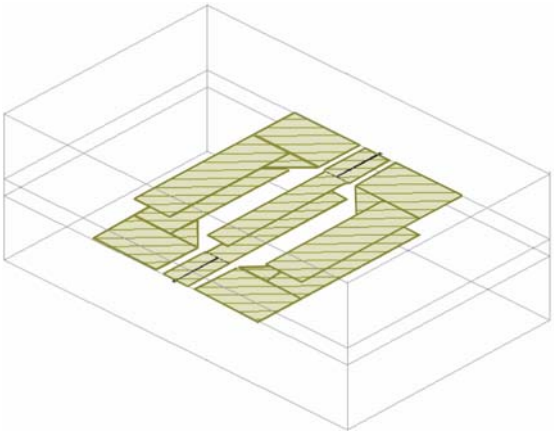

Fig. 1: Coplanar electromagnetic coupler

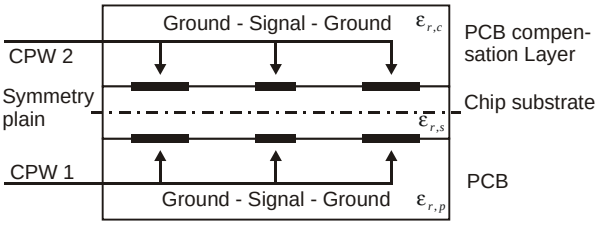

Fig. 2: Schematic cross section of the coupler

2 Modeling and Simulation

The general concept of electromagnetic coupling is presented in many text books while a surface-to-surface transition was investigated in [2]. Fig. 2 shows the adapted symmetric model necessary for even and odd mode analysis, where the symmetry condition leads to even and odd mode impedances and phase velocities. The open circuit boundary condition for two diagonally opposite ports, according to Fig. 1, results in the symmetric transmission matrix (ABCD-matrix) presented in [3]. Using the image impedance concept, the transmission characteristics can be described. Eqn. (1) yields an equivalent transmission coefficient γ_{eq}.

$$\gamma_{eq} = \cosh^{-1}\sqrt{AD} \qquad (1)$$

At an electrical length of $\theta = \pi/2$, the real and imaginary part of γ_{eq} are $\mathrm{Re}(\gamma_{eq}) = 0$ and $\mathrm{Im}(\gamma_{eq}) > 0$. The structure is equivalent to a lossless transmission line with frequency dependent impedance.

According to (2), the maximum of the image impedance at port 1 and port 2 has to be higher than the system impedance to achieve a matched condition. Electromagnetic simulations show that this condition can not be fulfilled for the given material stack and practical dimensions. It is therefore necessary to use impedance transformers at both ports [4].

$$\left(Z_{0,e} - Z_{0,o}\right)/2 \geq Z_{0,S} \qquad (2)$$

The signal coupler used in this design is not symmetric because there is no compensation layer on top of the structure which has the same relative permittivity ε_r as the PCB substrate (Fig. 3). In addition, there is a small air gap between chip substrate and PCB caused by surface roughness and conductor thickness. Consequently, it is an asymmetric configuration. In this case, the image impedances for port 1 and port 2 are different because the matrix elements A and D are not equal [5]. The investigation in [4] showed that it is possible to match the structure to the

system impedance with λ/4-transformers, since the impedances at both sides are real in the proximity of the maximum at port 1. For a center frequency of 24 GHz, the designed structure has dimensions according to Table I. A bandwidth of 10% with an insertion loss of less than 0.1 dB (RL > 20 dB) was determined by electromagnetic simulations using the Method of Moment (MoM) and the Finite Difference Time Domain (FDTD) Method, respectively.

Table I: Dimensions of the coupler

Strip width	150 µm
Ground gap	250 µm
Ground width	250 µm
Coupler length	850 µm
Substrate thickness (silicon)	100 µm
PCB thickness (Rogers TMM10i)	380 µm

3 Results

The signal coupler, shown in Fig. 3, is characterized with prototypes containing a single coupling structure.

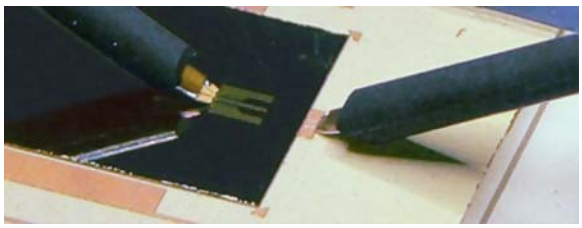

Fig. 3: Photograph of the coupler prototype

According to Fig. 4, the fabricated coupler shows the expected transmission behavior. Due to the initially approximated effective air gap between chip and PCB carrier, the center frequency of about 28 GHz and the impedance match deviate from the specification. By comparing the measurements with modified simulation models, using different air gap heights, the air gap could be determined to be d_{air} = 5 µm. The Smith chart in Fig. 5 shows that the fitted simulation not only matches the amplitude very exactly but even the phase, which supports the theory that the air gap is the only reason for the observed deviations.
Simulated optimizations based on the measured numbers predict a loss per transition of 0.28 dB-0.43 dB. Using the method of normalized losses, the attenuation caused by the structure itself is expected to be 0.13 dB-0.17 dB.

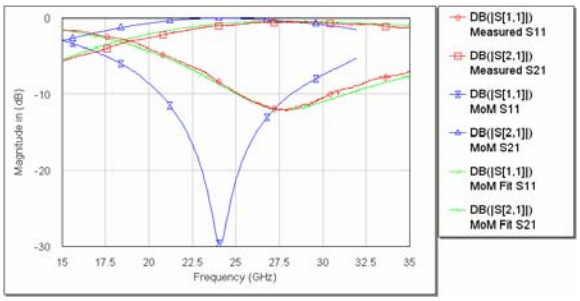

Fig. 4: Measured S-Parameter of the coupler and modified simulation results approximating the air gap

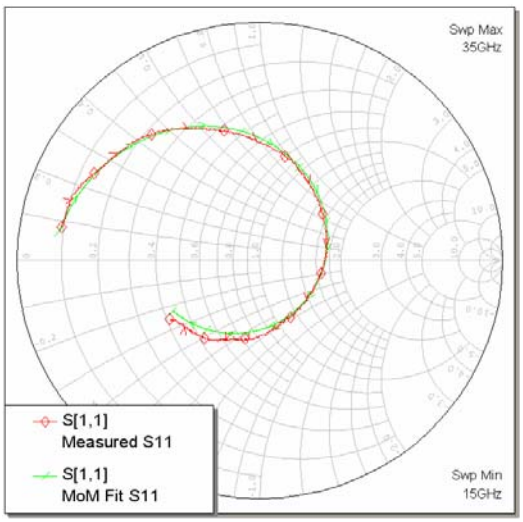

Fig. 5: Smith chart of Fig. 4 graphs

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High resolution low-g AIM sensor

Reuter, Danny[1]; Lohmann, Christian[1]; Bertz, Andreas[1]; Billep, Detlef[1]; Wiemer, Maik[2]; Gessner, Thomas[1,2]
[1]Chemnitz University of Technology, Center for Microtechnologies
[2] Fraunhofer Institute for Reliability and Microintegration, Departement MD&E

1 Introduction

Silicon Inertial sensors have been one of the driving applications for MEMS technology and supply a rapidly growing market. Since price and performance are the major factors for market success novel cost effective technologies have been developed. [1] In case of capacitive transducers, technologies for High Aspect Ratio Microstructures (HARMS) combine the advantages of both, Bulk and Surface Micromachining. High aspect ratio trenches enable large electrode areas with small gaps and large seismic masses, the near surface fabrication requires less chip area. However, the width of the sensing electrode gap can not be decreased arbitrarily, so the sensitivity for a given chip area is limited. Beside cost reduction and performance the reliability and long term stability of the sensor structures are the decisive factors to bringing a product to the market. Therefore a novel technique has been developed in order to enhance the sensitivity of accelerometers [2]. Furthermore the mechanical stability of the structures has been simulated, tested [3] and has finally been increased.

2 Sensitivity Enhancement Method

For detection of small signals, transverse moving interdigitated comb electrodes are very common, because of their high capacitive sensitivity. The capacitive sensitivity is given by:

$$\frac{\partial C}{\partial x} = \left(\frac{\varepsilon_0 \cdot h \cdot l}{(d_1 - x)^2} - \frac{\varepsilon_0 \cdot h \cdot l}{(d_2 + x)^2} \right) \approx \varepsilon_0 \cdot h \cdot l \cdot \left(\frac{1}{d_1^2} - \frac{1}{d_2^2} \right) \quad (1)$$

where d_1 and d_2 are the gap widths, h and l are the gap height and the gap length, respectively.
Presuming, the gap length scales with the chip area, the remaining variable for increasing the capacitive sensitivity, without increasing the chip area, is the aspect ratio of the trench. However, the DRIE limits the aspect ratio.
In order to reduce the trench width of the electrode gap below the technological limitations, a partial structure is moved in-plane against a stopper during the release etching step, reducing the sensitive electrode gap (fig. 1). The infeed device is actuated by a buckling beam mechanism, whereas the buckling is caused by residual mechanical film stress induced during the fabrication.

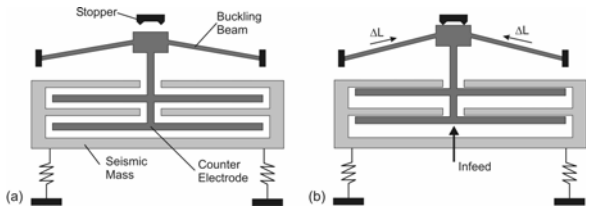

Fig.1: Schematic of the in-process gap reduction mechanism (a) before displacement of the substructure (b) after the displacement exited by the mechanical compressive stress in the buckling beams

The buckling beam mechanism is shown in figure 2. Assuming a small expansion Δl_b of the buckling beam and therewith a small change of the angle α, the deformation of the beam at the clamping points can be neglected and the form of the beam can be considered as linear. For this condition the mechanical gain of the buckling beam mechanism $\Delta h/\Delta l_b$ can be calculated from

$$\frac{\Delta h}{\Delta l_b} = \frac{\sqrt{(1+\varepsilon)^2 - (\cos\alpha)^2} - \sin\alpha}{\varepsilon} \quad (2)$$

using the strain ε. High values for the mechanical gain can be achieved for a small angle α and a small strain value.

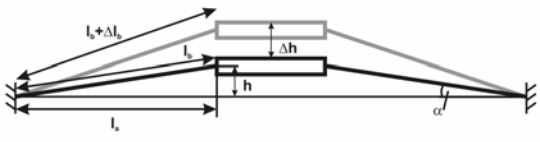

Fig. 2: Model of the buckling beam mechanism

The successful implementation of the method can be seen in figure 3. It shows SEM photographs of mechanism before and after the actuation of the infeed device.

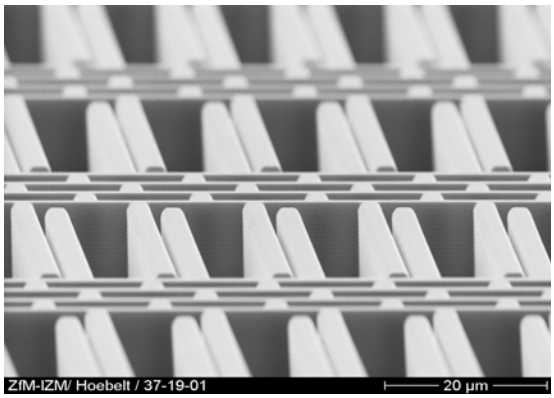

Fig. 3: SEM micrograph of the capacitive transducer after release etching

3 Ruggedization of Microstructures

The reliability of the low-g acceleration sensors has been tested by rapid thermal cycling of equivalent test structures [3] and impact load according to the DIN EN 60068-2-27 standard test method [4]. The thermal shock was applied 500 cycles between -25°C and 150°C and 750 cycles between -25°C and 125°C. No functional damage could be observed by optical characterization.
For the impact test the devices were accelerated 500g for 1ms and 1500g for 0.5ms. Depending on the type of the device the failure rate could be determined 20% up to 50%. An FEM model of the sensor was created in order to investigate the origin of the failure. Figure 4 shows the result of a static simulation, focusing on the deflection of the anchor structure causing inhomogeneous load on the interconnection beams.

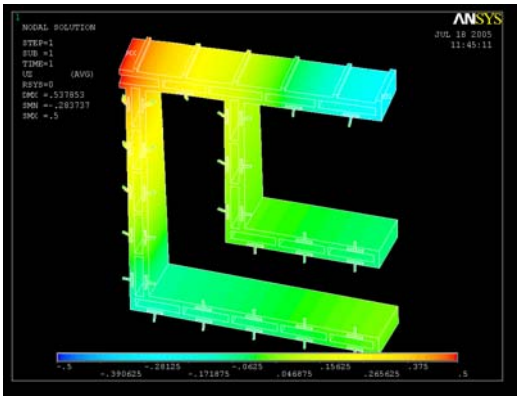

Fig. 4: Simulation of the anchor structure using static load

Including the results of the simulation, a new optimized anchor has been designed and integrated in the sensor layout. No failure due to mechanical shock could be observed during single impact tests. However these results will be confirmed with further investigations within the next months.

4 Wafer-Level-Packaging

For reliability and long term stability the microstructures have to be protected from environmental impact like particles and moisture. As industrial proven process, glass-frit bonding of silicon cap wafers has been used to hermetical seal the structures at the wafer level (Fig. 5). Coating and pattering of the glass paste were performed by screen printing. Electrical interconnection was realized by etching through-holes in the cap wafer enabling wire bonding.
The performance of the packaged low-g sensors was measured. The measurements show excellent results concerning sensitivity, temperature dependence and long time stability.

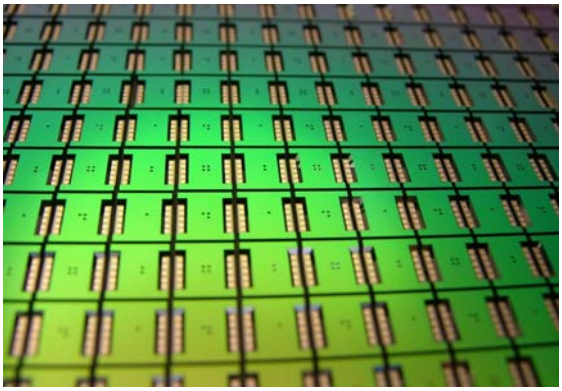

Fig 5: Photograph of glass sealed low-g sensors

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Development and Integration of Inertial Sensors within Active Smart RF-ID Label for Transportation Monitoring (Project ASIL)

Reuter, Danny[1]; Bertz, Andreas[1]; Wiemer, Maik[2]; Gessner, Thomas[1,2]
[1]Chemnitz Univ. of Technology, Center for Microtechnologies
[2] Fraunhofer Institute for Reliability and Microintegration, Departement MDE

1 Introduction

Within the project "ASIL" an active radio frequency identification (RFID) label for the monitoring of shock and inclination during transportation processes is being developed. For this purpose the requirements on the inertial sensors, measuring shock and inclination, are different to common applications. Therefore, the technology, the design and the packaging of the sensors have to be modified or developed respectively.

2 Sensor design and technology

The goal of the project is the integration of inertial sensors in already existing RFID labels. The specific problems are the limited energy supply, the very thin and flexible complete system and the high dynamic range of the sensor by low manufacturing costs.
The principle of the Active Smart ID Label (ASIL) is shown in figure 1. It includes the RF-chip with antenna and battery for the energy supply, as well as the sensor system, consisting of the micro mechanic transducer chip and the signal processing electronic chip.

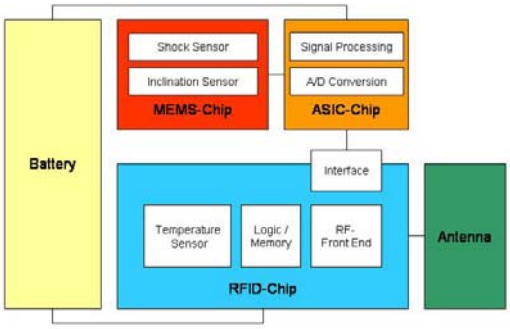

Fig. 1: Principle of the Active Smart ID Label transportation monitoring system

For the monitoring of transportation processes, the system has to detect and record illegal inclination and mechanical impact. In order to reduce the complexity of the system, it is reasonable to measure both with the same microstructure. Since inclination measurement means low-g acceleration, even a low resolution sensor for 15g shock needs a dynamic range of 80dB.
To achieve these ambitious requirements, we use the *Air gap Insulated Microstructures* (AIM) technology for sensor fabrication [1]. The capacitive working principle enables low energy operation, the high aspect ratio of the structures allows high sensitivity, and hence the required dynamic range. Figure 2 shows the SEM micrograph of a section of an AIM low-g sensor with high aspect ratio electrode plates.

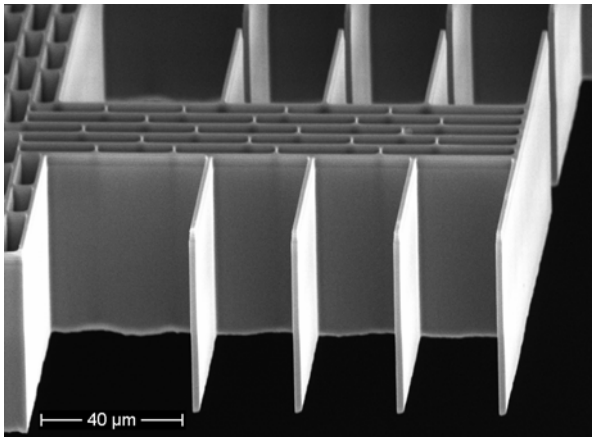

Fig. 2: SEM micrograph of AIM electrode plates with high aspect ratio

3 Sensor and System Packaging

The size of the label will be the format of a cash card. Therefore the height of the subsystems and hence the silicon dies is limited. So far, the sensors are packaged by bonding a silicon wafer to the sensor wafer using seal glass. Due to wafer handling, the minimum height of the wafers is limited. To meet the terms regarding the chip seize, it is possibly necessary to grind and polish the wafer stack to the final thickness.

Furthermore, the glass frit bonding is chip area consuming, due to the wide bonding frame.
Since wafer bonding, grinding and polishing are costly processes, thin film encapsulation (TFE) of microstructures could be the cost effective technology. The approach of this technology is the capping of microstructures using a sacrificial layer during deposition of the micro cap. The sacrificial layer is removed via inlet holes in the cap. The final deposition step is sealing the inlets hermetically [2]. Figure 3 shows the principle of the TFE.

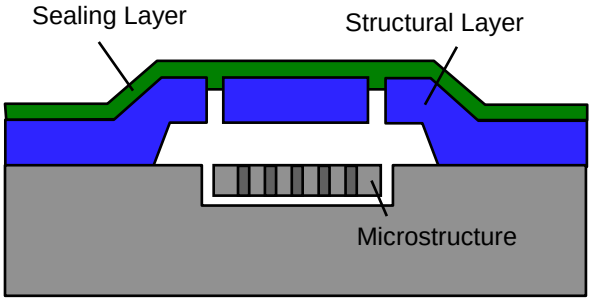

Fig. 3: Sketch of a thin film encapsulated microstructure

In contrast to sacrificial layer technologies which are using silicon dioxide as sacrificial material, for AIM other materials must be found. To avoid sticking of the microstructures after removal of the sacrificial layer, a dry etch process is preferable.

Figure 4 shows the SEM micrograph of a throughout dry processed microcap. With test structures a TFE technology compatible to the AIM could be demonstrated.

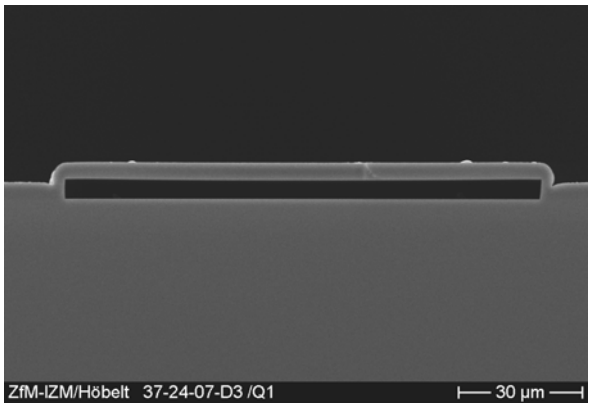

Fig. 4: SEM micrograph of a dry processed microcap

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Integrated analogue, mixed-signal and high-voltage design and device modelling

Steffen Heinz, Hendrik Zeun, Gunter Ebest
Chemnitz University of Technology, Faculty for Electrical Engineering and Information Technologies,
Chair Electronic Devices

1 Introduction

The main research areas of the professorship are characterisation and modelling of electronic devices as well as integrated analogue and mixed signal circuit design beside the investigation in cost-efficient processes for solar cells. The characterisation of semiconductor technologies contains the measurement and modelling of integrated electronic devices. In the context of miniaturisation different effects, such as contact phenomena, electro-migration, carrier lifetime, tunnel effects, ballistic and quantum effects and oxide respectively interface interactions, will be investigated.
The first research topic of the professorship is the creating of compact device models, especially for analogue and high-voltage technologies. Integrated high-voltage driver circuits are essential in MEMS applications with electrostatic driven actuators. A subset of device models in a high-voltage BCD technology has been developed in cooperation with alpha microelectronics gmbh. Also a new macro-model for high-voltage DMOS transistors has contrives in this cooperation project.
At present the physical and electrical behaviour of dielectric insulated structures in a high-voltage semiconductor technology will be investigated in cooperation with the X-FAB Semiconductor Foundries.
The interface between micro sensor or micro actuator and the information processing unit needs special adapted front-end electronics. This is the second research topic of the professorship. The knowledge in device modelling and the design skills for integrated circuits of the research group to be in demand in joint projects with alpha microelectronics gmbh, BMW AG Munich and Atmel Design Centre Dresden.
Low noise solutions, energy management, wireless data interfaces and reliability of integrated circuits are performance characteristics in MEMS applications especially in automotive implementations.

One example of the research activities of the professorship is the modelling of high-ohmic polysilicon resistors for applications in integrated high-voltage circuits.

2 Nonlinear Behaviour of integrated High-ohmic Polysilicon Resistors

Polysilicon resistors play a leading role in integrated circuits but their temperature and voltage dependence have to be considered. Different manufacturing methods exist for integrated resistors. High value polysilicon resistors as thin films on the field oxide (FOX) are entrenched in integrated high-voltage circuits. Important features are electrical strength, small parasitic elements and small size. These demands exist beside sufficient linearity and proper functioning at maximum occurring power dissipation. Another important feature is their lithographical accuracy of tenth part of the minimum technology feature size. Matching techniques with common centroid layout and dummy structures are used to minimize the tolerance gap additionally [2].
Polysilicon resistors produced by low pressure chemical vapour deposition (LPCVD) have a grain structure. The grains are sections with mono crystalline character. Their orientation and sizes are different. The grain-boundaries have a thickness of a few atomic layers with crystal imperfections. The crystal binding is impaired in these sections. Therefore, the grain-boundaries destine the electrical parameters of polysilicon resistors mainly.
Polysilicon resistors are divided in weak, middle and heavily doped sheet resistors. Weakly doped polysilicon has a negative temperature coefficient and heavily doped polysilicon gets a positive temperature coefficient. A temperature coefficient of about zero is obtained by middle doped sheet resistance.
High value polysilicon resistors are exclusive weakly doped sheet resistors. In small layers

nonlinear current-voltage dependence is caused by effects in the grain-boundaries. The necessary field strength must be greater than 103 V/cm for these nonlinear effects [5]. Publications with two theoretical approaches exist. The first one, the segregation model, was founded by Cowher and Sedgwick [6] and Fripp [7]. This model explained the nonlinearity with diffusion of dopant to grain-boundaries and the precipitation of dopant. The segregation model is inexact at higher temperature and higher doping levels.
The other one is the grain-boundaries trapping model. It was founded by Kamins [8] and refined by Seto [9]. In the grain-boundaries trapping of charge carriers reduce the conductivity of the polysilicon thin film. The trapped carriers create potential barriers in a space-charge region. Thereby, the mobility of charge carriers will be reduced. The crossing of these potential barriers will be described with thermionic emission of electrons to the vacuum energy level. The mono crystalline grains have no effect in this assumption. Additionally, a unity grain size and uniform dopant distribution will be assumed in the polycrystalline structure. The film thickness is very small compared to grain size and the grain-boundaries thickness is negligible. The charge distribution at the grain-boundaries is symmetrical. Tarng expands the model to small grain sizes, smaller than 10 nm [10]. In small grains the space-charge region overlaid the whole grain. Corresponding to current-voltage characteristic of a metal-semiconductor junction the symmetrical schottky barrier model is derived by:

$$J_{SSB} = 2A^{*}T^{2} \exp\left(-\frac{W_g}{kT}\right)\sinh\left(\frac{V}{2N_K U_T}\right) \qquad (1)$$

Another work describes variable grain sizes and modelling the grain region with tunnelling effect by higher doping concentrations.
For high value polysilicon resistors the symmetrical schottky-barrier model delivers sufficient results. Equation 1 is starting point of our implementation [1].

3 Scalable Resistor Model and Measurements

In most integrated circuit designs a lot of trade-offs have to be made. To minimize the time to market, scalability is a valuable aspect in up-to-date model development. For scalability in respect to width W the equation $n \cdot I(W) \equiv I(n \cdot W)$ and in respect to length L the equation $m \cdot V(L) \equiv V(m \cdot L)$ have to be satisfied. The hyperbolic function (1) that we use as model core satisfies these demands. Equation 1 is a function of temperature. Therefore, measurements versus temperature are necessary. Figure 1 shows measured and simulated resistance and current versus temperature of a 600 µm long and 20 µm wide resistor. A negative temperature coefficient can be seen as expected. Self heating was negligible because low currents were used.

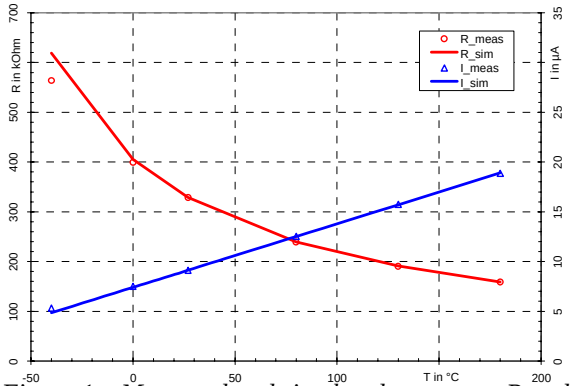

Figure 1: Measured and simulated resistance R and current I dTj without self heating and substrate effect

At some applications resistors can not be designed to prevent self heating. A separate circuit part with three elements models the self heating effect. A voltage source represents the power dissipation. A resistor and a capacitor correspond to thermal resistance and capacitance. The DC characteristics of the resistors were measured by a HP4062UX parameter test system. Its maximum applicable voltage with two high power source-monitor-units (HPSMUs) in series is 400 V and its minimum pulse width is 1 ms. Time constants for self-heating are on the order of microseconds. Therefore, measurements with pulse lengths of milliseconds and unpulsed measurements will give identical results.
Measurements showed a strong dependency on substrate voltage. Figure 2 shows measurement data where the substrate effect was compensated by connecting both terminals of the resistor to voltages with the same absolute value but different signs. A symmetric behaviour in respect to 0 V can be seen. In addition the simulated self heating temperature of our model is shown. A self heating of about 25 K is estimated at the maximum applied voltage of ±200 V.

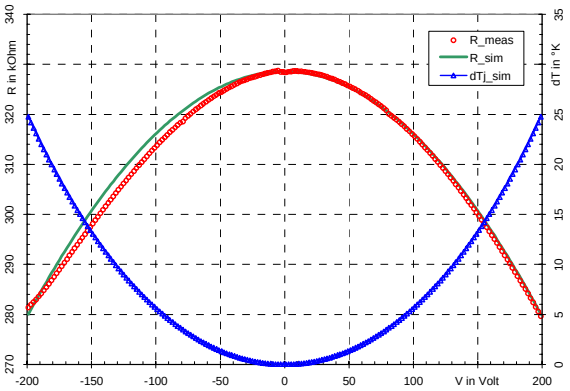

Figure 2: Measured and simulated resistance R and simulated self heating temperature dTj without substrate effect

Figure 3 contains data for the same measurement as in Figure 2 but without compensation of substrate effect. An asymmetrical behaviour can be seen. To keep the scalability of the model a linear factor is introduced to the actual model only. The linear representation of this behaviour improves the model accuracy significantly. A maximum error of less than 5% at all available geometries was achieved easily. Temperature parameters were optimized before optimization of parameters for self heating and substrate effects. This gave accurate optimization results fast.

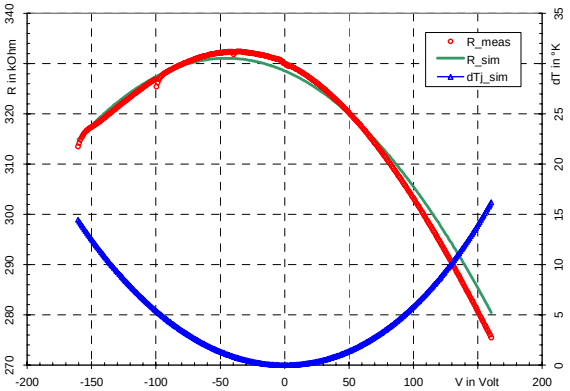

Figure 3: Measured and simulated resistance R and simulated self heating temperature dTj with substrate effect

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p-n junction formation at RIE textured silicon surfaces

Ebest, Gunter[1] ; Diefenbach, Karl Heinz; Denissov, Serguei; Erler, Klaus; Mrwa, Axel
[1]TU Chemnitz, Fakultät für Elektrotechnik und Informationstechnik, Professur Elektronische Bauelemente

1 Introduction

Reactive ion etching (RIE) is a promising tool in order to texture the surfaces of silicon (Si) wafers. If processed further to solar cells the resulting low reflectance coefficient leads to an increased photo current. A typical RIE-texture consists of small peaks spaced in sub-wavelength dimensions of the incident light (see Fig. 1). The texture consists of structures with heights of (50...200) nm.

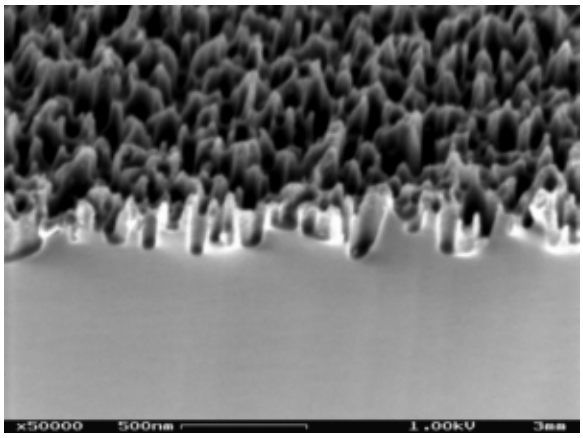

Fig. 1: Typical RIE-textured Si surface

However, during the fabrication of solar cells, in particular during the phosphorous (P) diffusion, the subtle RIE texture could be damaged: oxygen employed in an O_2-assisted (e.g. $POCl_3/O_2$-based) diffusion step could oxidise the texture. This oxide would be removed in the subsequent step (phosphorosilicate glass (PSG) removal via HF-etch). Therefore in addition to the $POCl_3$-based process the following methods of P-source forming, which have the potential to leave the texture unaffected, were investigated: spin-on dopant (SOD), plasma-enhanced chemical vapour deposited (PE-CVD) and low pressure (LP) CVD PSG. A comparison to the $POCl_3$-based process was performed by means of Scanning Electron Microscopy (SEM), sheet resistance mappings, and reflection coefficient measurements. Finally, RIE textured solar cells were manufactured with the diffusion technique, which turned out to be most suitable.

2 Experimental

For the investigations p-type (0.5...1.7) Ωcm Czochralski Si wafers were used. The RIE texturing was performed in a XPL 251 reactor (Secon) by means of an SF_6/O_2-based plasma, followed by a RCA cleaning step.
The PSG depositions were performed as follows:
Spin-on doping: Just after a HF treatment, which leaves the surface hydrophobic, a Merck KGaA dopant was spun onto the wafer. The layer was dried for 15 min at 200 °C.
PE-CVD: The deposition was carried out from MSF GmbH Frankfurt/Oder, Germany, at a temperature of 400 °C. The resulting layer with a thickness of 700 nm contained 4% P.
LP-CVD: As well the LP-CVD-PSG was deposited at MSF GmbH. The film with a P-concentration of 3% and a thickness of 1100 nm was deposited at T= 425 °C. An adjacent SiO_2-layer with a thickness of 100 nm followed, in order to protect the PSG against undesired contamination.
$POCl_3$: The PSG was generated in an $N_2/O_2/POCl_3$ gas flow at the same temperature as in the subsequent in situ annealing step.

The wafers with different PSG layers were annealed in N_2-atmosphere in order to perform the P-diffusion. During a subsequent immersion in hydrofluoric acid the layers were removed.
Afterwards, sheet resistances were taken by means of 4-point probe measurements.
In order to fabricate solar cells, the wafers were coated on their front side with a PE-CVD SiN_x antireflection and passivation layer. The deposition was performed with the same process parameters as necessary for the formation of 80 nm thick layers onto planar surfaces. Consequently, the deposition led to a thickness of less than 80 nm on textured surfaces. The metallisation was made up of sputtered Al at the back side and screen printed Ag paste on the front side.
Measurings of the reflection coefficient were carried out with an extended Bruker IFS/66 spectrometer.

3 Results and discussion

3.1 Comparison of sheet resistances

Assuming that the PSG-components are sufficiently able to reach the bottom of the texture the surface would be completely covered with PSG. In this case, the emitter generation would result in similar sheet resistances (R_s) as obtained in the case of planar wafers.

In contrast, Table I shows partly tremendous differences in R_s between both types of surfaces. Deposited on a RIE texture, SOD PSG delivers an enhanced R_s, compared to planar surfaces.

Table I: Sheet resistance R_s versus PSG-type

PSG	T [°C]	t [min]	R_s [Ω/sq.]	
			planar	RIE
SOD	900	15	50	57
PE-CVD	900	15	31	2698
LP-CVD	900	15	-	2439
$POCl_3$	850	25	39	39
PE-CVD	950	60	-	109
LP-CVD	950	60	-	51

Whereas SOD PSG is generally able to fill cavities between the peaks the drying gives rise to shrinkage due to evaporation of solvents. Consequently, the PSG could loose contact to the silicon surface at the bottom of the texture. This circumstance leads obviously to a reduced diffusion of P-atoms in regions without direct contact between PSG and Si surface. Since the P-concentration in regions without direct contact of both surfaces would be decreased, the resulting sheet resistance rises with an enlargement of the delaminated areas.

A similar situation should occur for LP-CVD PSG. In the case of textured surfaces the LP-CVD PSG leads also to a strong increased R_s.

According to the SEM pictures in Fig. 2 and 3 the differences in R_s seems to originate from a lack of PSG on the bottom of the texture: both of the deposits precipitated mainly on the top of the peaks. With proceeding deposition the emerging PSG rods increased their widths and coalesced. In this situation the P atoms obviously have to evaporate from the PSG-cap into the hollows before they would be able to cross the Si surface at the bottom of the texture. Analogue to the case of SOD-PSG during annealing the diffusion of P-atoms will be diminished in the regions at the bottom of the texture. Consequently the PSG-depleted area gives rise to an increased R_s as shown in Table 1.

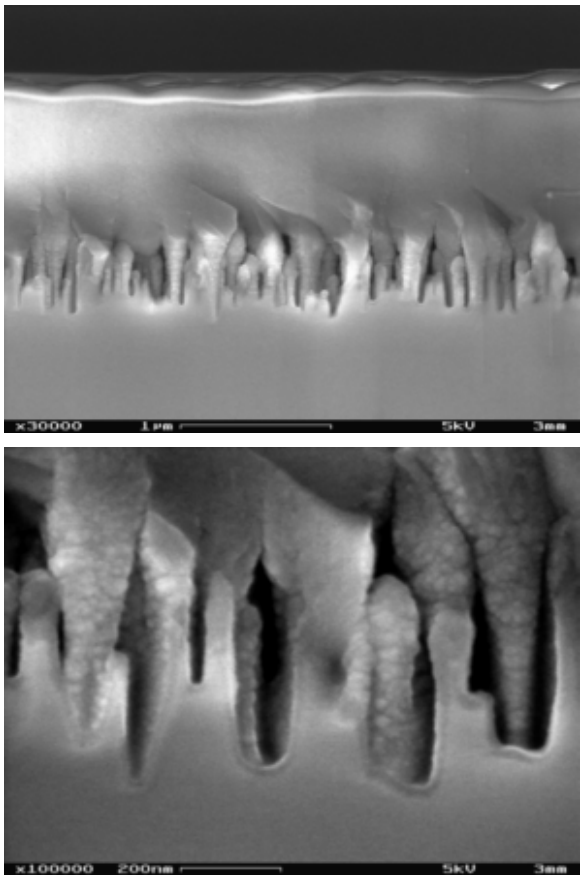

Fig. 2: LP-CVD PSG deposited on a RIE-textured silicon surface

The differences of R_s between textured and planar surfaces imply that the diffusion performed using the LP- and PE-CVD deposited PSG layers gives rise to a microscopically inhomogeneous distribution of P-atoms.

With regard to the processing costs one should also consider the application of energy: An annealing at 900 °C / 15 min was already sufficient in order to create an emitter at a planar surface with R_s= 31 Ω/sq. by means of PE-CVD. On the contrary, at textured wafers coated by means of PE-CVD (LP-CVD) needed 950 °C and 60 min to achieve sheet resistances of 109Ω/sq. (51 Ω/sq.).

Another situation arises if $POCl_3$ is used to create the P-source, since the resulting PSG grows accompanied by an oxidation of the silicon surface. This technique allows the generation of PSG-layers which exhibit a throughout sufficient thickness on the top as well as on the bottom of the texture (see Fig. 3). An annealing of the wafers covered with this layer leads to the R_s-values shown in Table 1, apparently with similar results for textured and planar surfaces.

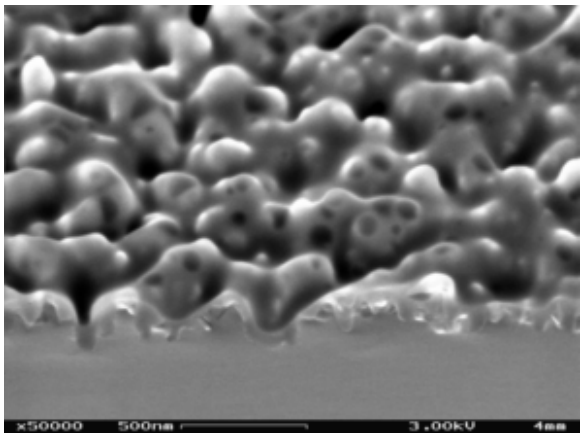

Fig. 3: Growth of $POCl_3$ PSG oxidises the RIE texture

On the other hand, a comparison of Fig. 1 and 3 shows that the subtle texture undergoes a modification: the thin peaks apparently have been disappeared. This caused the reflection coefficient to increase, as can be seen in Fig. 4 from graphs (a) and (b). But (c) shows that the deposition of a SiN_x layer decreases the reflection coefficient again to (1…2) % in the range of (400...1000) nm. For wavelengths greater than 600 nm the surface exhibit even a lower reflection coefficient then just before the diffusion process. Graph (d) shows that the firing-through step does obviously not affect the reflection coefficient.

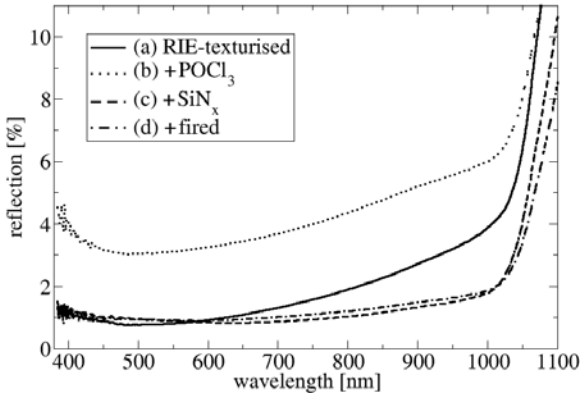

Fig. 4: Reflection coefficient of a RIE textured surface at different solar cell processing stages: (a) solely RIE textured; (b) after a $POCl_3$ diffusion; (c) $POCl_3$ diffusion + SiN_x passivation; (d) surface from "(c)" additionally fired

It is worthy of mention that in contrast to a first apprehension the subtle texture was neither completely oxidised nor heavily damaged. Also remarkable is, that the deposition of the SiN_x-layer restored the excellent reflection properties of the RIE-textured but O_2-affected surface. Since the $POCl_3$-based process led obviously to emitters with a primarily homogeneous distribution of P-atoms it was applied in a solar cell processing sequence.

3.2 Solar Cells

Table II shows parameters of the best textured and planar cells as well as the mean values for groups of 15 cells, respectively.

Table II: Parameters of the solar cells

surface		**U_{oc} [mV]**	**j_{sc} [$\frac{mA}{cm^2}$]**	**FF [%]**	**η [%]**
planar	best	614.5	32.5	78.9	15.8
	mean	603.8	32.9	76.3	15.2
RIE-textured	best	607.4	35.6	78.6	17.0
	mean	599.0	34.0	76.1	15.5

As expected, the textured cells exhibit increased short current densities j_{sc}. Whereas the best RIE-textured cell displays a clearly better efficiency (17.0 % versus 15.8 % on the planar surface) the corresponding mean value is slightly increased.

4 Summary and conclusions

A comparison of various P-sources (SOD, PE-CVD, LP-CVD and $POCl_3$) has revealed a crucial point of the PSG-generation: the formation of a sufficiently thick layer on the bottom of the texture. From this point of view, the $POCl_3$-based P-diffusion leads to optimal PSG-formation. The reflection coefficient obtained during the RIE treatment increased after the $POCl_3$-based P-diffusion. The subsequent deposition of a SiN_x-layer has recovered the excellent initial reflection properties. Therefore, this method seems to be suitable for the fabrication of RIE-textured solar cells. Planar and RIE-textured solar cells were fabricated by means of $POCl_3$. The latter exhibited an averaged short current density of 34.0mA/cm^2, i.e. an improvement of about 1.1mA/cm^2 compared to the planar cells. The mean efficiency shows a slightly enhanced value, too. The textured cells still suffer from plasma-generated damages. Therefore, the application of a defect removal is likely to improve the performance of RIE-textured solar cells.

Acknowledgement

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The authors would like to thank the staff of the Center of Microtechnologies for preparations, M. Henker for numerous SEM investigations as well as T. Schwarz (TU Chemnitz) for enabling measurements.

Silicon Standard for the Calibration of Instruments of Micro Hardness Testing

Frühauf, Joachim[1] ; Gärtner, Eva [2]
[1]TU Chemnitz, Fakultät für Elektrotechnik u. Informationstechnik, Fachgruppe Werkstoffe d. ET/Elektronik
[2] now: SiMETRICS GmbH, Limbach-Oberfrohna

1 Introduction

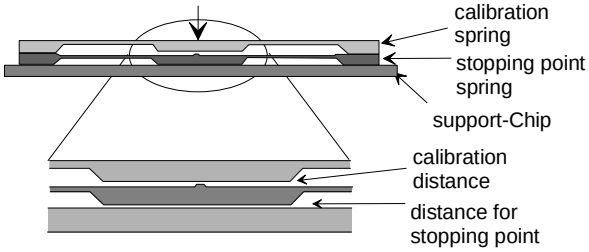
For the measurement of the hardness of materials a spherical or pyramidal tip will be pressed onto the surface by a defined loading force. The hardness correlates with the diameter or the depth of the produced depression. The so called instrumented indentation test (prEN ISO 14577 [1]) provides more detailed informations. This method records the complete relation between the increasing and hereafter decrea-sing force and the resulting values of the indentation depth. Most instruments measure the force and the indentation depth by electromagnetic transducers which have to be regularly and reliably calibrated. The usual method compares the shape of actual indentations with calibrated indentations on hardness test blocks. In the case of viscous materials this is an unsuitable method because of the instability of the indentations.
To overcome these disadventages a new material measure is developed as a standard which uses a linear elastic spring system. The spring system arrives at a stopping point with a definite distance when the force is increased up to a definite value. Silicon is a suitable base for material measures because of its very stable properties as elastic constants, low thermal expansion, large ther-mal conductivity and considerable hard-ness. Additionally, the processes of silicon micro-technologies guarantee the preparation of a material measure with precise parameters.

2 Design and Preparation

2.1 Requirements and Design

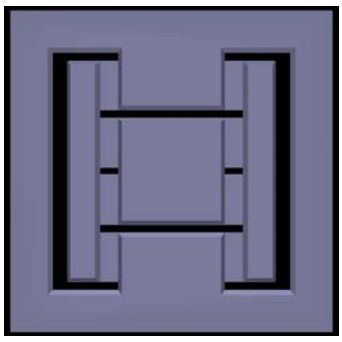
The standard is designed for the calibration of instruments of microhardness testing. An elastic deflection of 25 µm of the spring should be reached at a maximum load < 1 N indicated by an abrupt increase of stiffness at the stopping point. To avoid damages the stopping point is situated on a second spring limiting the stiffness, fig. 1.

Fig. 1: Principle of the standard



Besides of the main parameters F_A and f_A belonging to the sharp kink of the stiffness some further features must be demanded: the exact linear spring characteristic and the insensitivity to small excentric loading points. These demands can be fullfilled by a boss fixed at a system of parallel springs inside a frame, fig. 2.

Fig. 2: System of parallel springs (simulated by SIMODE). The middle plate (boss) is fixed by 2x2 springs connected with coupling bars which are fixed to the frame by 2x2 springs



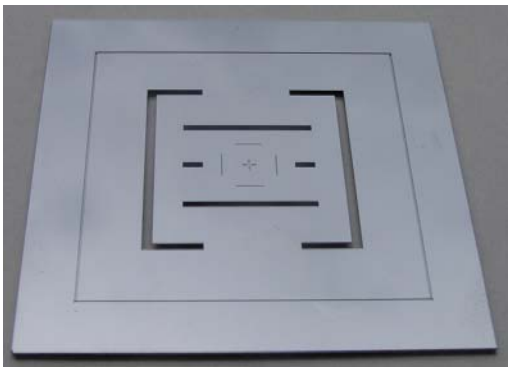
Excentric loading leads to a tilting of the boss and consequently to a changed distance of the stopping point. The resulting uncertainty can be minimized by enlarging the boss and reducing the area of contact at the spring system with the

stopping point. This spring system is similar designed. The only difference consists in the structures on the boss plate: the boss of the calibration spring has marks to limit the area for loading; the boss plate of the stopping point spring is thinned outside of a small contact area in the centre. The plateau of the contact area is lowered relative to the frame by the stopping point distance f_A. Finally, a third chip supports the stack of calibration spring and stopping point spring. This chip has a shallow central deepening giving space for a small deflection of the stopping point spring. Because of the demand on the insensitivity with regard to excentric loading the chips have relative large dimensions of 5x5 cm^2.

2.2 Preparation Steps

Because of the large chip size the preparation is based on 6“-wafers (orientation: {100}; n-type: 20 Ωcm). Four chips of each type (calibration spring, stopping point spring, support) are realized on different wafers with a thickness of 600 µm for the support and 525 µm for the other chips (double-sided polished).

Fig. 3: View of the standard. In the centre the marks for positioning can be seen. The support chip is larger by 5 mm than the other chips for a better handling.



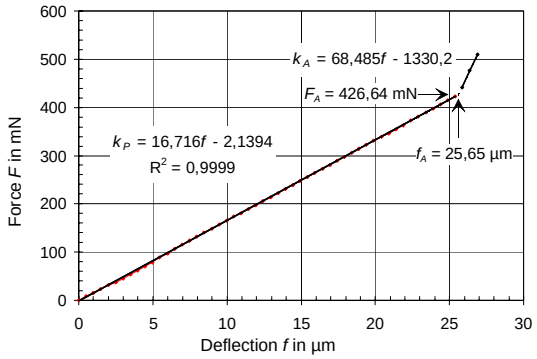
The preparation of the wafers with the support chips or the calibration springs are simple 1-mask (front) respective 2-mask (front, back) processes using KOH-etching for structuring. The preparation of the wafers with the stopping point spring needs 1 mask at the back side and 3 masks at the front (structures of springs and boss plate, structure of the contact region, etching of the stopping point distance). The mask for etching of the stopping point distance protects only the frame. Consequently all free convex edges are blunted preventing a wear at the edges of the contact region. This etching step uses TMAH producing a better uniformity.

After the wafer processes the wafers with the structures of calibration springs are silicon fusion bonded on the wafers with the stopping point springs. For the mounting of this stack on the wafer with the support two ways are tested: silicon fusion bonding (ideally but difficult because of stresses in the thick stack of 3 wafers) or glueing by SU8 epoxy. The project report gives more detailed information [2].
After packaging the standards are diced by sawing. Fig. 3 shows the standard.

3 Results

The characteristics of the produced standards (stiffness $k = F/f$; stopping point distance f_A) are measured using a micro force-deflection testing instrument and a commercial micro-hardness testing instrument. Fig. 4 presents a typical characteristic showing two linear branches with a sharp kink in between. f_A can be calculated by intersection of the Gaussian straights. Together with the stiff-ness of the calibration spring k_P the standard represents a defined stopping point force F_A.

Fig. 4: Typical force-deflection characteristic of the developed standard



Moreover the characteristics measured by other users (PTB, ASMEC) are in good agreement.

Acknowledgments

The authors thank the Stiftung Industrie-forschung for the financial support of the development. Further, the autors are grateful to the coworkers of the ZFM of the Chemnitz University of Technology for their help .

4 References

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[2] Frühauf, J.; Gärtner, E.: *Projektbericht*

Deposition of amorphous hydrogenated diamond-like carbon films (a-C:H)

Schirmer, Klaus; Lutz, Josef
TU Chemnitz, Fakultät für ET/IT, Professur Leistungselektronik und elektromagnetische Verträglichkeit

1 Introduction

The CVD reactor for deposition and etching of diamond-like carbon (DLC) layers was installed in Sept 2005 at the Chemnitz Center for Microtechnologies. The run in of the equipment was completed and process development started. The first aim is to develop amorphous hydrogenated carbon layers suitable for passivation of power semiconductors. Another future application is to use DLC as etch stop layer in MEMS fabrication because of its chemical inertness.

2 Passivation principles

The transition of the pn-junction of a high voltage power device to the surface of the device is very sensitive to surface charges . The desired blocking capability of the device can only be reached, if the peak value of the electric field at the transition can be suppressed by an adequate passivation technology. Due to the termination of the p-n junction at the surface, the blocking behaviour is very sensitive to the properties of the interface between amorphous carbon and crystalline semiconducting substrates. Because of the high density of states in the band gap of DLC, mirror charges can be created, which avoid high electrical field peaks, and which are able to compensate disturbing interface charges as shown in Fig. 1. This promises high breakdown voltage and excellent long term stability and reliability.

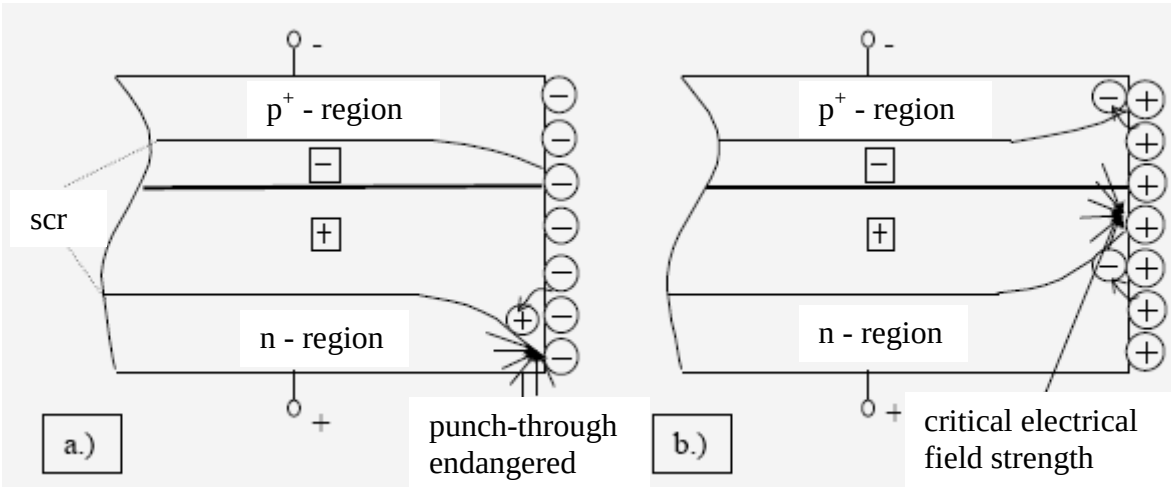

Fig 1: Influence of negative (a.) and positive (b.) surface charges on the space charge region of a p^+-n junction[1]

3 MicroSys400 system

The MicroSys 400 PECVD system consists in a adjustable parallel plate arrangement which allows to vary the distance from 30 – 130mm, a chamber of 500 mm in diameter, a water cooled substrate electrode for deposition dimensions up to 300 mm in diameter, a 5 kW rf generator and a gas supply system for 6 gas lines.

In the experiments performed so far we deposited DLC on Si wafer of 4, 5 and 6 inch in diameter. These wafers were mounted on special carriers with appropriate indentation for each wafer size.

4 Processing

Fig. 2: MicroSys400 with the load lock on the right side

One process requirement beside homogeneity is to ensure a maximum substrate temperature below 140°C during deposition. The measurement was done with thermo stripes directly on the substrate surface. Already low power densities of 0.8W/cm^2 resulted in temperatures of more than 240°C within deposition times of 5 minutes, although the wafer carrier remained with less than 80°C comparatively cool. Obviously the energy transfer from the substrate to the carrier was very small. Clamping the wafers onto the carrier was considered to be a properly remedy, but it turned out to be insufficient. With implementation of an additional active He-backside cooling to the wafer, the temperature remained below 140°C even at power densities above 2W/cm^2.

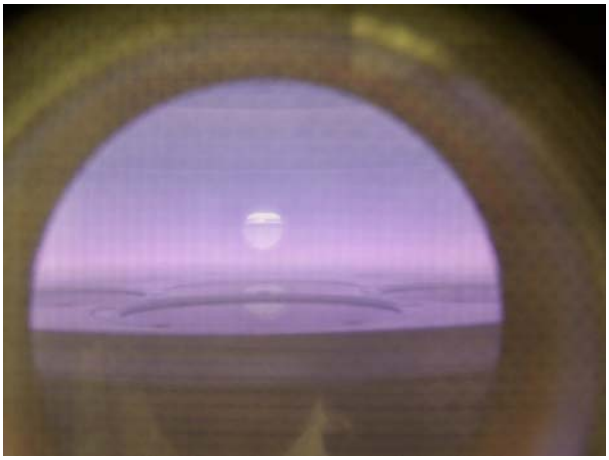

Fig. 3: View into the chamber during processing 7 4-inch wafer

Before metallization the DLC passivation has to be structured. Because of its chemical inertness the commonly used technique is the patterning with a resist mask and the exposure to an O_2-plasma. Resist mask usually are removed with oxygen after plasma processes in semiconductor fabrication processes. As a consequence, the structuring process has to be smooth enough not to aggress the resist and to leave it solvable for standard wet chemical removal. In the surrounding area of the clamping rings, plasma inhomogeneities lead to problems in the removal process. The problems have been solved by laying the wafers on a planar carrier. The power density remains at less than 0.25W/cm^2, accordingly no exalted temperatures occurred.

Fig 4: Carrier for 5-inch wafers. On the right the indentation with He channel in the middle and a viton gasket, on the left a diode wafer after plasma etching.

Currently we DLC-plate 5-inch wafers with 1600V rectifier diode chips in collaboration with the IXYS Semiconductor GmbH, Lampertheim. They will be metallized and packaged in the IXYS production line and then resend to Chemnitz for further electrical characterization and reliability tests.

References

[1] T. Wrase, Inauguraldissertation, Universität Basel, 2000

BMBF-Project : “Advanced Supercaps based on nanostructured materials (Nanocap®II)”

Bodach, Mirko; Mehlich, Heiko; Lutz, Josef
TU Chemnitz, Faculty of Electrical Engineering and Information Technology, Chair of Power Electronics and Electromagnetic Compatibility

1 Introduction

Chemnitz University of Technology is involved in the project “Advanced Supercaps based on nanostructured materials (Nanocap®)”. This project is supported by the German Government (BMBF) and controlled by the TÜV Rheinland Group. It was started in September 2005.
The aim of this project is the development of a new generation of supercaps with technical features better than commercial supercaps. Our part is the application-oriented research of the reliability of such components [1] an the implied “electrical design”.

2 Project tasks

For the measuring concept for the determination of the electrical qualities (e.g. capacity, intrinsic resistance into dependence of the temperature) of the partners with each other among other things according to DIN IEC 62391.
Some necessary tasks are:

- determination of temperature dependency of electrical characteristics
- temperature cycling
- active load cycling of supercaps
- determination of cycling capability in dependence of cycling conditions
- derivation of electrical and reliability parameters of advanced supercaps

3 First results

Figure 1 shows in a self discharge test the voltage of a state of the art supercap package in dependence on the temperature. The self-discharge effect is strongly increasing with temperature.
From measurements, adapted simulation models for use in a electrical circuit simulation systems are derived. Figure 2 shows the measurement of the charging of a supercap package, the measurement results are compared to predictions

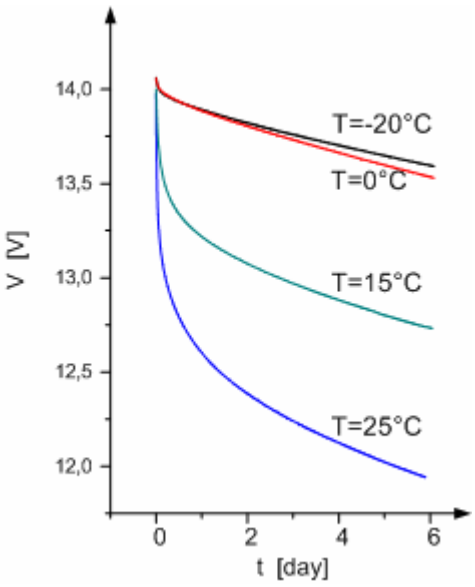

Fig. 1: Self-discharge-test of a Supercap package; Voltage depends on time and temperature

of the developed model. The agreement is sufficient. The derived models are used to predicict the behaivour of the supercaps in different application conditions.

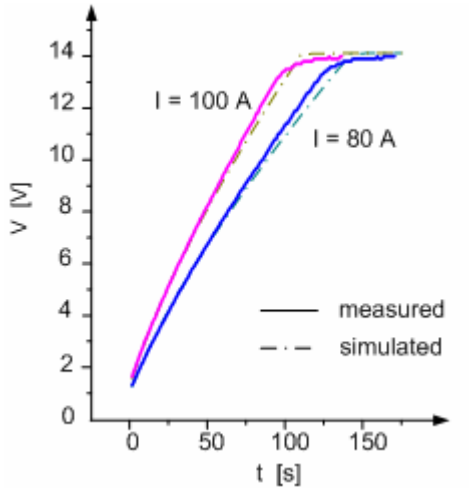

Fig. 2: Charging of a Supercap measured and simulated [1]

4 References

[1] Mehlich, Bodach, Lutz: "Investigations of Reliability of Supercaps ", Proceedings of the PCIM Europe 2006, Nuremberg

5 Cooperations with industry and universities

Partnerships with the following institutes and companies were continued and / or established in 2005:

- Advanced Micro Devices (AMD), Sunnyvale & Austin, USA and Dresden, Germany
- Aktiv Sensor GmbH, Stahnsdorf, Germany
- Alpha Microelectronics GmbH, Frankfurt (Oder), Germany
- AMTEC GmbH, Chemnitz, Germany
- Applied Materials, Santa Clara, USA and Dresden, Germany
- ASMEC Advanced Surface Mechanics GmbH, Radeberg, Germany
- Atmel Design Center, Dresden, Germany
- AUDI AG, Ingolstadt, Germany
- BASF AG, Ludwigshafen, Germany
- BMW AG München, Germany
- Robert Bosch GmbH, Reutlingen & Stuttgart, Germany
- Cabot Microelectronics Europe
- CAD-FEM GmbH Grafing, Germany
- CiS Institut für Mikrosensorik gGmbH, Erfurt, Germany
- Colour Control Farbmeßtechnik GmbH, Chemnitz, Germany
- DaimlerCrysler Research Lab Ulm, Germany
- Danfoss Silicon Power, Schleswig, Germany
- Digital Instruments – Veeco Instruments, Mannheim, Germany
- DILAS Diodenlaser GmbH
- EADS Deutschland GmbH, Corp. Res. Ctr. Germany, Dept. Microsystems, München, Germany
- Endress und Hauser Conducta GmbH & Co. KG, Germany
- Eupec GmbH Warstein, Germany
- FACRI , Research Institute, Xi´an, China
- Fahrzeugelektrik Pirna GmbH, Pirna, Germany
- FHR Anlagenbau GmbH, Ottendorf-Okrilla, Germany
- First Sensor Technology GmbH, Berlin, Germany
- FLEXIVA automation & robotics, Amtsberg, Germany
- Forschungszentrum Rossendorf, Germany
- Fujitsu Microelectronic GmbH, Dreieich-Buchschlag, Germany
- GEMAC mbH Chemnitz, Germany
- GF Messtechnik Teltow, Germany
- Gesellschaft für Prozeßrechnerprogrammierung mbH (GPP) Chemnitz, Germany
- GHF IWM Halle
- Heinrich-Hertz-Institut Berlin, Germany
- Hitachi Ltd., Japan
- Institut für Festkörper- und Werkstoffforschung e.V. IFW Dresden, Germany
- IMEC, Leuven, Belgium
- Infineon Technologies AG, Munich and Dresden, Germany
- InfraTec GmbH, Dresden
- ITIM International Training Center for Material Science, Vietnam
- IXYS Semiconductor GmbH, Lampertheim, Germany
- Jenoptik-LDT GmbH, Gera , Germany
- Kyocera Fineceramics GmbH
- L.A.A.S-C.N.R.S Toulouse, Prof. Dr. D. Esteve, France
- LETI, Grenoble, France
- LG Thermo Technologies GmbH
- Lionix, Enschede, Netherlands

- LITEF GmbH, Freiburg, Germany
- Lucent Technologies, Nürnberg, Germany
- Massachusetts Institute of Technology, Cambridge / Boston, Mass., USA
- Max-Planck-Institut (MPI) für Mikrostrukturphysik Halle, Germany
- Mechanical Engineering Laboratory AIST, MITI, Dr. Mitsuro Hattori and Chisato Tsutsumi, Tsukuba, Ibaraki, Japan
- memsfab GmbH, Chemnitz, Germany
- Merck KGaA, Darmstadt, Germany
- Mesa Research Institute, Prof. J. Fluitman, Twente, The Netherlands
- Microtech GmbH, Gefell, Germany
- Mitsui Engineering and Shipbuilding Co. Ltd., Japan
- Motorola, Phoenix, Arizona ,USA / Munich, Germany
- MPA NRW Materialprüfungsamt Nordrhein-Westfalen, Germany
- Nex Systems, Wilmington, MA. , USA and Berlin, Germany
- NICO Pyrotechnik, Trittau, Germany
- OEC GmbH, Germany
- PANALYTIK GmbH, Dresden, Germany
- Panasonic Plasma Display Dev. Lab., Inc., Highland, New York, USA
- Physikalisch-Technische Bundesanstalt Braunschweig (PTB), Germany
- PLASMACO Inc. Highland, New York, USA
- Preh GmbH, Bad Neustadt, Germany
- Raytek GmbH Berlin, Germany
- Rohm and Haas Electronic Materials, Marlborough, USA
- Roth & Rau Oberflächentechnik GmbH, Wüstenbrand, Germany
- RWE Schott Solar GmbH, Alzenau, Germany
- Schott Mainz & Schott Glas Landshut, Germany
- Seiko Epson, Japan
- Sentech Instruments GmbH, Berlin, Germany
- SICK AG, Waldkirch & Ottendorf-Okrilla, Germany
- SF Automotive GmbH, Freiberg, Germany
- Siegert TFT GmbH, Hermsdorf, Germany
- Siemens A&D ATS2 Nürnberg und AT Regensburg, Germany
- Institut für Solarenergieforschung Hameln-Emmerthal, Germany
- Solid State Measurements, Pittsburgh, PA., USA
- ST Microelectronics, Crolles, France
- Suss Microtec AG Vaihingen, Munich and Sacka, Germany
- Dr. Teschauer AG, Chemnitz, Germany
- Thales-Avionics, Valence and Orsay, France
- TRW Airbag Systems GmbH & Co. KG, Aschau/Inn, Germany
- X-Fab Gesellschaft zur Fertigung von Wafern mbH, Erfurt, Germany
- Yole Developpement, Lyon, France
- ZMD Dresden, Germany
- 3D-Micromac AG, Chemnitz, Germany

Universities:

- Johannes Kepler Universität Linz, Austria
- Atominstitut Universität Wien, Austria
- Chongqing University, Chongqing, China
- Fudan University, Shanghai, China
- TSINGHUA University, Beijing, China
- Xiamen University, Xiamen, China
- University of West Bohemia, Pilsen , Czech Republic

- Technische Universität Braunschweig, Germany
- Universität Bremen, Germany
- HTW Mittweida, Laserapplikationszentrum, Germany
- TU Dresden, Germany
- Universität Erlangen, Germany
- Universität Essen, Institut für anorganische Chemie, Germany
- Universität Hannover, Germany
- Westsächsische Hochschule Zwickau (FH), Zwickau, Germany
- TU Budapest, Hungary
- University of Tokyo, Res. Ctr. for Adv. Science & Technology (RCAST), Japan
- University of Delft, Netherlands
- University of Twente – MESA, Netherlands
- Warsaw University of Technology (WUT), Warsaw, Poland
- Nowosibirsk State University, Russia
- Technological University Singapore, Singapore
- Royal Institute of Technology, Stockholm, Sweden
- University of Hertfordshire, UK
- State University of New York at Binghamton, USA
- Portland State University, Portland, Oregon, USA
- Rensselaer Polytechnic Institute (RPI), Troy, N.Y., USA
- University of Nevada, Reno, USA
- University of California at Berkeley, Berkeley Sensor and Actuator Center, USA
- Case Western Reserve University, Cleveland, Ohio, USA
- University of Colorado at Boulder, USA
- University of Delaware, Newark, USA
- Hanoi University of Technology, Vietnam

6 Equipment and service offer

The ZfM facilities include 1000m² of clean rooms (about 30% of them class 10 to 100). Modern equipments were installed for processing of 100 mm and 150 mm wafers as well as design and testing laboratories providing the basis for the following processes, partly in cooperation with the Fraunhofer Institute IZM, branchlab Chemnitz:

- Design (Workstations)
- Mask fabrication 3" ... 7" / Electron beam lithography / Proximity and contact double-side lithography
- High temperature processes: Diffusion / Thermal oxidation / Annealing / RTP
- Etching (dry: Plasma- and RIE-mode & wet: isotropic / anisotropic → equipment: Alcatel MCM, SECON XPL 251, STS Multiplex ICP-ASE, Metal Etch DPS Centura & ARIAS silicon wet etching box for etchants based on KOH and TMAH)
- Chemical vapor deposition MOCVD (Precision 5000 [Cu, WN, TiN])
- Chemical vapor deposition PECVD (Precision 5000 [SiO_2, Si_3N_4, CF-Polymer, SiCH, SiCOH, SiCNH])
- Physical vapor deposition PVD (MRC 643, FHR 150x4, CLC 9000, ...)
- Chemical mechanical polishing CMP
- Wafer bonding: silicon direct, anodic, eutectic, glass frit
- Testing (SEM, AFM, electrical, mechanical …)

The ZfM provides the following services :

R & D

(e.g. Si processes, technology, development of sensors and actuators, metallization)

- Thermal oxidation of silicon wafers
- PVD (Cr, Au, Ag, Ti, TiN, Ta, Cu , Pt, Co, Al, W, TiW, $AlSi_x$,CrNi, Pyrex)
- CVD: PECVD / LPCVD (600° C ... 900° C)
  (SiO_2 , Si_3N_4 , Polysilicon, $Si_xO_yN_z$, Cu-MOCVD, TiN-MOCVD, SiCOH, SiCH)
- PECVD (diamond-like Carbon films, a-C:H)
- Dry etching (Si, SiO_2 , Si_3N_4 , Polysilicon, Silicides, Al, refr. metals, TiN, Cr, DLC, lowk dielectrics)
- Wet etching (SiO_2 , Si_3N_4 , Si, Polysilicon, Al, Cr, Au, Pt, Cu, Ti, W)
- Wafer lithography / Electron beam lithography / Mask fabrication (3“ ...7“ Cr mask)
- Design & simulation (technology, process....)
  Software: ANSYS, SIMODE, PHOENICS, SIMBAD, EVOLVE ,
  Etch mask design tool EMADE
- Parametric testing: Waferprober, HP Testsystem
- Design of low power and low noise, analogue-mixed signal integrated circuits
- Design of integrated high-voltage circuits
- Characterization of analogue-mixed signal circuits up to 500 MHz
- Characterization and modelling of devices from low-voltage and high-voltage micro technologies

and in **analytical fields** such as

- Scanning electron microscopy SEM / EDX
- Atomic force microscopy AFM (D 3000)
- Variable angle spectroscopic ellipsometry (Sentech SE-850, UV-VIS-NIR)
- Laser profilometry (UBM, TENCOR FLX-2900)
- Surface profilometer (TENCOR alpha step 200, Dektak 3)
- US-Microscope
- Zug-/Druckprüfmaschine Zwick 4660 universal
- Perkin-Elmer DMA 7e dynamic mechanical analyser
- Micromechanical testing instrument (Sartorius and PI)
- Lifetime scanner SEMILAB WT-85

In cooperation with the Fraunhofer Institute IZM, branchlab Chemnitz:

- STS „Multiplex ICP“ etch tool for deep silicon etching
- Wafer bonding (silicon fusion bonding, anodic bonding, eutectic bonding, Seal-glass-bonding, adhesive bonding)
- CMP MIRRA & ONTREK-cleaner (Copper, Silicon, SiO_2)
- Test measurements for MEMS

7 Education

7.1 Lectures

Electronic Devices and Circuits
Elektronische Bauelemente und Schaltungen
Lecturer: Prof. Dr. G. Ebest

Electrical Engineering / Electronics
Elektronik
Lecturer: Prof. Dr. C. Radehaus

Design Technology and Production Engineering
Konstruktions- und Fertigungstechnik
Lecturer: Prof. Dr. W. Dötzel

Materials Science in Electrical Engineering
Werkstoffe der Elektrotechnik / Elektronik
Lecturer: Prof. J. Frühauf

Fundamentals of Electronic
Grundlagen der Elektronik
Lecturer: Prof. Dr. G. Ebest

Electronic Devices
Elektronische Bauelemente
Lecturer: Prof. Dr. G. Ebest

Optoelectronics
Optoelektronik
Lecturer: Prof. Dr. C. Radehaus

Semiconductor Device Technology
Technologien der Mikroelektronik
Lecturer: Prof. Dr. T. Gessner

Solid State Electronics and Photonics
Festkörperelektronik und - photonik
Lecturer: Prof. Dr. C. Radehaus

Electrophysics
Elektrophysik
Lecturers: Prof. Dr. C. Radehaus

Fundamentals, Analysis and Design of Integrated Circuits
Integrierte Schaltungstechnik
Lecturer: Prof. Dr. G. Ebest

Physical and Electrical Design
Physikalischer und elektrischer Entwurf
Lecturer: Prof. Dr. G. Ebest

Analog Integrated Circuit Design
Analoge integrierte Schaltungstechnik
Lecturer: Prof. Dr. G. Ebest

Microtechnologies / Materials and Technologies of Microsystems and Devices
Mikrotechnologien / Werkstoffe und Technologien der Mikrosystem- und Gerätetechnik
Lecturers: Prof. J. Frühauf, Prof. Dr. T. Gessner

Basics and Application of Solar Power Engineering
Grundlagen und Anwendung der solaren Energietechnik
Lecturers: Prof. Dr. G. Ebest, Prof. Dr. U. Rindelhardt

Optocommunication
Optokommunikation
Lecturer: Prof. Dr. C. Radehaus

Electrooptics
Elektrooptische Bilderzeugung
Lecturer: Prof. Dr. C. Radehaus

Device Technology
Gerätekonstruktion
Lecturer: Prof. Dr. W. Dötzel

Microsystems
Mikrosystemtechnik
Lecturer: Prof. Dr. W. Dötzel

Reliability and Quality Assurance
Technische Zuverlässigkeit / Qualitätssicherung
Lecturer: Prof. Dr. W. Dötzel

Control Engineering (Microsystem Technology)
***Prüftechnik* (*Mikrosystemtechnik*)**
Lecturers: Dr. J. Markert, Dr. S. Kurth

Technical Optics
Technische Optik
Lecturer: Dr. B. Küttner

Computer Aided Design
CAD
Lecturer: Dr. J. Mehner

Semiconductor Measurement Techniques
Halbleitermeßtechnik
Lecturers: Prof. Dr. C. Radehaus, Prof. Dr. M. Hietschold

Electrical Drives
Elektrische Antriebe / Gerätetechnische Antriebe
Lecturers: Prof. Dr. W. Hofmann, Dr. R. Kiehnscherf

Integrated Circuit Design
Schaltkreisentwurf
Lecturer: Prof. Dr. D. Müller

System Design
Systementwurf
Lecturer: Prof. Dr. D. Müller

EDA-Tools
EDA-Tools
Lecturer: Prof. Dr. D. Müller

Rapid Prototyping
Rapid Prototyping
Lecturer: Prof. Dr. D. Müller

Components and Architectures
Components and Architectures
Lecturer: Prof. Dr. D. Müller

Design and Calculation of Power Electronic Systems
Entwurf und Berechnung leistungselektronischer Systeme
Lecturer: Prof. Dr. J. Lutz

Industrial Electronics
Industrielle Elektronik
Lecturer: Prof. Dr. J. Lutz

Power Electronics
Leistungselektronik
Lecturer: Prof. Dr. J. Lutz

Semiconductor Devices in Power Electronics
Bauelemente der Leistungselektronik
Lecturer: Prof. Dr. J. Lutz

Process and Equipment simulation
Prozesssimulation / Equipmentmodellierung
Lecturers: Prof. Dr. T. Gessner, Dr. R. Streiter

7.2 Student exchange programmes

SOCRATES / ERASMUS

I.S.M.R.A. – Ecole Nationale Supérieure d`Ingénieurs Caen, France
Technical University of Cluj-Napoca, Romania
Katholieke Universiteit Leuven / IMEC, Belgium
Danmarks Tekniske Universitet, Lyngby, Denmark
Ecole des Mines de Nancy, Nancy, France
University of Oulu, Finland
Universite de Rennes I, France
Technical University of Lodz, Poland
Royal Institute of Technology Stockholm, Sweden
University of West Bohemia, Pilsen , Czech Republic
Hristo Gendov, University of Burgas, Bulgaria

IAS/ ISAP Programme (DAAD)

University of Delaware, Newark, USA
University of Nevada, Reno, USA
Portland State University, Portland, USA

DAAD

University of Hanoi, Vietnam

7.3 Project reports/ Diploma theses / PhD

Project reports

Bleul, K.:	Entwicklung einer Lasermikrobearbeitungstechnologie für den Abgleich von Silizium-Mikroaktoren
Böhme, J.:	Entwicklung einer LED-Beleuchtung für flexible Endoskopie
Böhme, M.:	Entwurf eines Prozesssteuermoduls zur Atomlagenabscheidung
Erler, C.:	Untersuchung eines Mikromischers auf der Basis der sequentiellen Segmentierung
Gebauer, St.:	Ansteuerelektronik für einen Vakuumsensor unter Nutzung eines digitalen Signalprozessors
Günnel, H.:	Untersuchung zur technologischen Kompatibilität von porösen low-k Materialien bei CMP-Prozessen für die Herstellung moderner Leitbahnsysteme
Günnel, H.:	Entwicklung von Technologien für CMP von dünnen Si- und SiO_2-Schichten
Hofmann, L.:	Application of VCSELs in FTTH and Backplane Interconnects (University of Nevada, Reno)
Käsler, F.:	Kapazitive und induktive Energieübertragung in Mikrosystemen
Kirch, M.:	Lasermikrobearbeitung
Lasch, M.:	Redesign einer Rakelmaschine für das Lasermikrosintern von Mikropräzisionsbauteilen
Luf, A.:	Entwicklung eines integrierten rauscharmen CMOS-Operationsverstärkers für kleine Spannungen.
Noeth, N.:	Temperaturstabile Metallisierung für SOI-Drucksensoren
Nowack, M.:	Wafer-Level-Packaging
Päßler, F.:	Konzept und Funktionsnachweis eines mikrofluidischen Aktor-Prinzips in Polymersubstraten
Pohl, R.:	sign of bending structures with electrostatic switchable stiffness.
Reichmann, B.:	Entwicklung und Test eines geregelten zweiachsigen Scannsystems
Reinhold, S.:	Charakterisierung eines Piezo-Schwingerregers für Silizium-Mikrostrukturen.
Richtsteiger, A.:	Konzepterstellung für eine erweiterte Prozesssteuerung sowie deren Aufbau
Rieger, C.:	Messplatz zum Test von Beschleunigungssensoren
Schäfer, T.:	Characterization of silicon springs as standards for hardness testing instruments
Schaufuß, J.:	Metallisierung mikrostrukturierter Polymersubstrate
Schaufuß, J.:	Elektrostatische Sonden zur mechanischen Anregung von MEMS auf Waferlevel
Schmidt, A.:	Modifikation und Entwicklung von CMP-Prozessen zur Herstellung von Cu-basierten Leitbahnsystemen für Bauelemente der künftigen Technologie-niveaus
Schubert, T.:	Synthese eines Ansteuersignals für Horizontalscanner

Stammberger, K.:	Schwingungsanalysen im Maschinentestzentrum Chemnitz
Staude, D.:	Konzeption eines portablen optisch-fluidischen Analysesystems
Wittig, A.:	Überarbeitung des Praktikumsversuchs „Rechnergestütze Messwerterfassung“
Wolf, N.:	Entwicklung und Aufbau einer Abform- und Packagingtechnologie
Zeidler, H.:	Konzept und Funktionsnachweis zur Integration aktiver optischer Komponenten in mikrostrukturierte Polymersubstrate

Diploma works

Bonitz, J.:	Herstellung ultraschmaler Leitbahnen mit herkömmlichen Prozessen Advisor: Dr. S.E.Schulz
Drouve, P.:	Aufbau eines Messplatzes zur Charakterisierung von 2D-Beschleunigungssensoren Advisor: Dipl.-Ing. M. Dienel
Engelmann, M.:	Entwicklung eines digitalen Signalprozessorsystems für die Mikrosystemtechnik Advisors: Prof. W. Dötzel, Dr. S. Kurth (FhG IZM)
Forke, R.:	Entwicklung eins mikromechanischen gekoppelten Schwingungsmesssystems für frequenzselektive Vibrationsmessung Advisors: Prof. Dötzel, Dr. Scheibner, Siemens
Hambsch, M.:	Entwicklung eines neuen Lösungskonzeptes für ein rotatorisches absolutes Messsystem auf der Grundlage magnetoresistiver Sensorelemente Advisors: Dr. Kiehnscherf, Dipl.-Ing. Schönitz, Fa. Gemac Chemnitz
Hammer, K.:	Integrierte Sensorauswerteelektronik unter dem Aspekt der Anwendung im Automobil Advisors: Prof. G. Ebest, Dr. W. Koppehel , Atmel Dresden
Hientzsch, M.:	Integrierte Mikrosensorik zur Überwachung des temperaturbedingten Verschleißes an künstlichen Hüftgelenken Advisors: Prof. T. Otto (FhG-IZM), Dr. J. Boese-Landgraf (Klinikum Chemnitz)
Hillert, A.:	Entwurf eines integrierten AD-Wandlers Advisor: Prof. G. Ebest, DI H.Zeun
Hoppe, M.:	Lokale Energiegewinnung für Mikrosysteme Advisor: Dr. Billep
Hoyer, K.:	Konstruktion, Aufbau und Inbetriebnahme eines Laserbelichters zur Erzeugung von hochauflösenden rauscharmen holografisch-optischen Elementen in Dichromat-Gelatine-Schichten Advisors: Dr. Markert, Dr. Dittrich, Fa. sax3d.com GmbH Chemnitz
Klemm, L.:	Entwicklung einer optimalen Aufbau- und Verbindungstechnik für elektronisch kalibrierbare Si- Drucksensorelemente Advisors: Dr. D. Billep, Dr. Schroth, Fa. Intelligente Sensorsysteme GmbH Dresden
Kluth, M.:	Realisierung eines Messplatzes zur Bestimmung des elektrischen Oberflächenpotentials Advisor: Dipl.-Ing. M. Hanf
Koch, T.:	Aufbau und Charakterisierung einer Detektoreinheit und eines Referenzsystems für einen Temperaturscanner Advisors: Prof. T. Otto (FhG-IZM), Dipl.-Ing. R. Saupe

Krause, T.:	Der Roadmapping-Prozess einer Life Cycle Unit Advisors: Prof. Käschel, Prof. T. Gessner
Leidich, S.:	Koplanare elektromagnetische Signalkopplung für HF-MEMS- Bauelemente Advisor: Dr. S. Kurth (FhG IZM)
Ludewig, T.:	Plasma enhanced low temperature wafer level bonding of silicon to glass wafers Advisors: Prof. Käschel, Prof. T. Gessner, Dr. M. Wiemer
Otto, M.:	Einsatz von Mikrospiegelarrays in einem Hadamard-Transformations-Spektrometers Advisor: Dipl.-Ing. M. Hanf
Richter, G.:	Experimentelle Charakterisierung und Vergleich mikromechanischer Beschleunigungssensorarrays Advisor: Dipl.-Ing. M. Dienel
Scheffler, K.:	Polymersolarzelle auf Glas / PET Advisors: Prof. J. Grimm (FHS Zwickau), Dipl.-Ing. R. Saupe
Schmiedl, J.:	Abstandsmesssystem mit Mikrospiegel Advisor: Dr. J. Markert
Seifert, M.:	Anwendung von Si-Mikrostrukturen zur Kontrolle von Geräten der Oberflächenmesstechnik Advisor: Prof. J. Frühauf
Specht, H.:	Vertikal-Ablenksystem für Head-up-Display Advisors: Prof. W. Dötzel, Dr. S. Kurth (FhG-IZM)
Stürmer, M.:	Untersuchungen zur spektralen Empfindlichkeit eines IR-Spektrometers Advisors: Prof. T. Otto (FhG-IZM), Dipl.-Ing. R. Saupe
Voigt, S.:	Entwurf und Realisierung eines Mikrowellen-Phasenschiebers in MEMS-Technologie” Advisors: Prof. T. Gessner, Dr. S. Kurth (FhG-IZM)
Weber, M.:	Entwicklung und Realisierung eines Schwingungsmesssystems zur Charakterisierung von Mikroaktoren für die Lasermikromaterialbearbeitung Advisors: Dr. C. Kaufmann, DI Petsch

PhD / Habilitation

Dr.-Ing. Dirk Scheibner January 14, 2005
“Entwicklung eines frequenzselektiven Schwingungsmesssystems mit abstimmbaren mikromechanischen Resonatoren“
TU Chemnitz, Fakultät ET/IT

Dr.-Ing. Fouad Bennini February 25, 2005
„Ordnungsreduktion von elektrostatischen-mechanischen Finite Elemente Modellen für die Mikrosystemtechnik..“
TU Chemnitz, Fakultät ET/IT

Dr.-Ing. Roy Knechtel March 18, 2005
„Halbleiterwaferbondverbindungen mittels strukturierter Glaszwischenschichten zur Verkapselung oberflächenmikromechanischer Sensoren auf Waferebene“
TU Chemnitz, Fakultät für ET/IT

Dr.-Ing. Robert Siegmund March 24, 2005
„Ein Verfahren zur Protokollspezifikation für die Verifikation und Synthese protokollorientierter digitaler Systeme“
TU Chemnitz, Fakultät ET/IT

Dr. - Ing. habil. Martin Liess May 25, 2005
„Design neuer Sensoren unter Berücksichtigung von Strukturaspekten“
TU Chemnitz, Fakultät ET/IT

Dr.-Ing.Vasco Jerinic May 30, 2005
„ParaGraph – Parameterprüfung für Intellectual Properties“
TU Chemnitz, Fakultät ET/IT

Dr.-Ing. Michael Schlegel October 4, 2005
„Mixed-Level-Simulation heterogener Systeme mit VHDL-AMS durch Multi-Architecture-Modellierung“
TU Chemnitz, Fakultät ET/IT

Dr.-Ing. Chenping Jia December 12, 2005
„Mikromechanischer Ultraschallwandler aus Silizium – Silicon Micromachined Ultrasonic Transducers“
TU Chemnitz, Fakultät für Maschinenbau

8 Colloquia / Workshops at the Institute

March 10, 2005
Mario Seifert, Prof. J. Frühauf, TU Chemnitz, Fakultät ET/IT
“Rillengitter und Kraftnormale aus Si zur Überprüfung von Tastschnittgeräten”

May 17, 2005
Prof. James Morris, Department of Electr. & Computer Engn., Portland State University, Portland USA
„Resonant Tunnel Diode (RTD) Stability"

May 24, 2005
Prof. Dr. rer. nat. Gerd Bacher, Universität Duisburg-Essen, Fak. für Ingenieurwissenschaften
“Nanoanalyse innovativer Materialien und Bauelemente”

October 20 , 2005
Prof. Robert Magerle, TU Chemnitz, Fakultät für Naturwissenschaften, Inst. für Physik
"Selbstorganisation polymerer Nanostrukturen"

November 24, 2005
Prof. Ralph Spolenak, ETH Zürich, Dept. of Materials
„Local materials inhomogeneities – cause for reliability issues in microsystems ?“

November 30, 2005
Dipl.-Ing. Joachim Piltz, amtec Analysenmesstechnik GmbH Leipzig
„Röntgenfluoreszenzanalyse von dünnen Schichten“

9 Scientific publications 2005

Baum, M.; Hientzsch, M.; Boese-Landgraf, J.; Otto,T.; Gessner, T.: „Verschleißmonitoring bei Hüftgelenkendoprothesen durch integrierte Mikrosensorik“, Mikrosystemtechnik Kongress 2005; Proceedings, pp 633-636

Baum, M.; Nestler,J.; Rost,D.; Weissmantel,S.; Otto,T.; Reisse,G.; Gessner,T.: „Improved Silicon Master Tools for Hot Embossing“, Micro System Technologies 2005, Munich (Germany), 2005 Oct 5-6; Proceedings, pp 76-82

Belsky, P.; Streiter,R.; Wolf,H.; Gessner,T.: “Application of Molecular Dynamics to the Simulation of IPVD”, Advanced Metallization Conference 2004, San Diego CA, U.S.A., 2004 Oct 19-21; MRS Conf. Proc. AMC XX, Material Research Society, Warrendale PA (2005), pp 787-792

Bertz, A.; Lohmann,C.; Reuter,D.; Gessner,T.: “Efficient and Flexible High Aspect Ratio Micromachining for the Fabrication of low-g-Sensors (invited)”, Microcar 2005, Leipzig, June 22; Micromaterials and Nanomaterials, Volume of Abstracts, 04 2005 (2005) , p.79

Billep, D.; Hiller, K.; Frömel, J.; Tenholte, D.; Reuter, D.; Dötzel, W.; Gessner, T.: “Post-Processing Gap Reduction in a Micromachined Resonator for Vacuum Pressure Measurement”, SPIE Conference: Microtechnologies for the New Millennium 2005, Sevilla, Spain, 2005 May 09-11, Proc.

Blaschta, F.; Schulz, S.E.; Gessner, T.: “Impact of reducing resist stripping processes at elevated temperature on ULK and HM materials”, Materials for Advanced Metallization - MAM, Dresden, 2005 March 6-9; Microelectronic Engn. 82/3-4 (2005), pp. 427-433

Blaschta, F.; Schulz, S.E.; Gessner, T.: “H_2-Strip Processes on Low-k Materials”, Talk, European Congress on Advanced Materials and Processes EUROMAT, Prague, Czech Republic, 2005 Sep 5-8

Bonitz, J.; Ecke,R.; Schulz,S.E.; Gessner,T.: “Different SiH_4 Treatments of CVD TiN Barrier Layers”, Materials for Advanced Metallization - MAM, Dresden, 2005 March 6-9; Microelectronic Eng., 82/3-4 (2005), pp. 618-622

Dienel, M., Shaporin A., Richter, G., Kolchuzhin, W., Billep, D., Dötzel,W.: „Komponentenentwurf“, 7. Chemnitzer Fachtagung Mikrosystemtechnik- Mikromechanik & Mikroelektronik 26./27.10.2005, Chemnitz, 2005, pp 129-136

Dienel, M., Billep, D., Dötzel, W.: „Development of a drift compensated acceleration sensor array”, 50. Internationales wissenschaftliches Kolloquium, 19.-23.9.2005, Ilmenau, 2005, pp. 227-228

Dötzel, W.: „Mikrosystemtechnik - Wachstum ins Kleine“, Vortrag an der Sächsischen Akademie der Wissenschaften, Leipzig, March 2005

Ebest, G.; Mrwa, A.; Erler, K.; Rindelhardt, U.: “Light trapping and optical losses in solar cells with RIE textured surfaces”, 20th PVSEC, Barcelona (Spain), 2005 June 6-10

Ecke,R.; Schulz,S.E.; Hecker,M.; Engelmann,H.-J.; Gessner,T.: „W(Si)N Diffusion Barriers for Cu Metallization deposited by PECVD“, Advanced Metallization Conference 2004, San Diego CA, U.S.A., 2004 Oct 19-21; MRS Conf. Proc. AMC XX, Material Research Society, Warrendale PA (2005), pp. 793-799

Flaspöhler, M.; Bonitz, J.; Kaufmann, C.; Hahn, R.; Billep, D.; Hübler, A.: „Eigenschaften mikrotechnisch gefertigter Transmissionsgitter”, 7. Chemnitzer Fachtagung Mikrosystemtechnik- Mikromechanik & Mikroelektronik, Chemnitz, 2005 Oct 26-27; Proceedings, pp. 155-159

Forke,R.; Mehner,J.; Dötzel,W.; Gessner,T.: „Mikromechanisches gekoppeltes Schwingsystem für frequenzselektive Vibrationsmessungen”, 7. Chemnitzer Fachtagung Mikrosystemtechnik- Mikromechanik & Mikroelektronik, Chemnitz, 2005 Oct 26-27; Proceedings, pp. 143-148

Frömel,J.; Wiemer,M.; Bagdahn,J.: „Mechanische Zuverlässigkeit der Verkapselung von MEMS“, Microcar 2005, Leipzig, 22.06.2005

Frömel,J.; Wiemer,M.; Gessner,T.: “Packaging of MEMS structures in SCREAM technology using anodic bonding”, Micro System Technologies 2005, München , 2005 October 5-6; Proceedings , pp. 99-104

Frühauf, J.: „Werkstoffe der Mikrotechnik. Lehrbuch für Ingenieure“, Fachbuchverlag Leipzig im Carl Hanser Verlag, 2005, Carl Hanser Verlag München Wien

Frühauf, J.; Gärtner, E.; Seifert, M.: “Solid Hinge Guide Made by Silicon Bulk Technology”, Proceedings of the EUSPEN, p. 329, Montpellier 2005

Frühauf, J.; Krönert, S.: “Wet etching of silicon gratings with triangular profiles”, Microsyst. Technol. (2005) 11, pp.1287-1291

Frühauf,S.; Himcinschi,C.; Rennau,M.; Schulze,K.; Schulz,S.E.; Friedrich,M.; Gessner,T.; Zahn,D.R.T.; Led,Q.T.; Caluwaerts,R.: “Scaling down thickness of ULK materials for 65 node and below and its effect on electrical performance”, Materials for Advanced Metallization - MAM, Dresden, 2005 March 6-9; Microelectronic Eng.82, 3-4, 2005, pp. 405-410

Gessner,T.: Mikrosystemtechnik im Automobilbau, June 22, 2005, 2. Fachkongress Micro-Car 2005, Leipzig

Gessner,T.; Frömel,J.; Jung,E.; Reichl,H.: “MEMS and MOEMS Packaging”, 2nd Mechatronics and Microsystems Symposium DCMM, Delft (Netherlands), 2005 September 7-8

Gessner,T.; Schulz,S.E.; Schulze,K.; Ecke,R.; Frühauf,S.; Streiter,R.: Challenges of Advanced Interconnect Systems: Cu diffusion barrier, porous low k dielectrics and thermal issues, Invited Talk. ICMAT 2005, Singapore, 2005 June

Gessner,T.: Interconnect Systems: Challenges for Nanoelectronics, Saxon-British Nanotechnology Forum, October 3, 2005, DTI Conference Centre, London

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10 Guests & special international relations

Visiting Scientists / Guests:

January 3-4	Prof. Victor E. Drozd, St. Petersburg State University, Russia
February 9	Mr. Taniguchi, Mr. Sumita, Mr. Fukui HIROX Co. Ltd., Tokyo, Japan
April, 5	Prof. Li, President; Prof. Wu, Prof. Wen, Prof. Zheng, Prof. Liu, Chongqing University, China
April 13	Prof. M. Esashi, Tohoku University, Sendai, Japan
April 19-20	Dr. T. Lechtenberg, Vice President; Dr. Streckert, General Atomics, San Diego, USA
May 16-17	Prof. James E. Morris, Portland State University, Portland, USA
June	Doz. Dr.-Ing. Jan Mühlbacher, Dozentenaustausch, TU Pilsen, Tschechien
June	Doz. Dr.-Ing. Vaclav Kus, Dozentenaustausch, TU Pilsen, Tschechien
June	Doz. Dr.-Ing. Vlastimil Skocil, Dozentenaustausch, TU Pilsen, Tschechien
July 19-20	Prof. R. Bruch, University of Nevada, Reno, USA
August	Dr. Al-Douri, Al al Bayt University, Mafrag, Jordanien
August 25	25 Students from India
October 10	Dr. William (Bill) T. Siegle , Senior Vice President and Chief Scientist, retd. Advanced Micro Devices, Sunnyvale, USA
October 17	Delegation of the City of Columbia and the Columbia Office of Economic Development, USA
October	Doz. Dr.-Ing. S. Simeonov & Dr.-Ing. S. Kartunov, TU Gabrovo, Bulgarien
October	Doz. Dr.-Ing. Vladimir Shulgov, University Minsk, Belarus
November 15	Dr. Abbaspour & 8 students (MERC) Materials and Energy Research Center, Teheran, Iran
November 24-25	Prof. Dr. Ralph Spolenak, ETH Zürich, Laboratory for Nanometallurgy, Switzerland

Scientific coworkers / PhD:

DI Alexej Shaporin	Novosibirsk Technical University, Russia November 2002 – December 2005
DI Wladimir Kolchuzhin	Novosibirsk Technical University, Russia November 2002 – December 2005
Chenping Jia	University of Xian, China, January 2003 – December 2005
Yukito Sato	Ricoh Company Ltd., Japan October 2004 – February 2005

Students:

Markvart, Jan	TU Pilsen April 2005 – August 2005	SOCRATES
Hodacova, Martina	TU Pilsen April 2005 – August 2005	SOCRATES
Vartika Gupta	New Delhi, India July 1 – August 12, 2005	IAESTE Program
Seat, Filip	University of Ljubljana, Slovenia October 2005 – March 2006	SOCRATES
Zhang, Xiao Chuan	MEMS Res. Ctr., Xiamen Univ., China Since September 2005	PhD