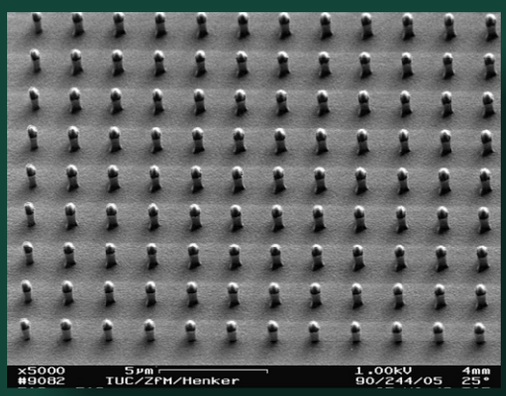
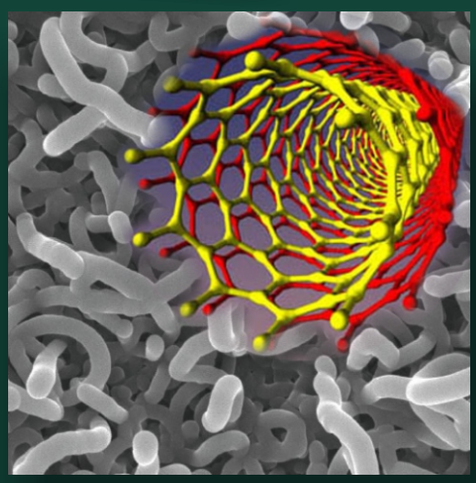
CHEMNITZ UNIVERSITY OF TECHNOLOGY

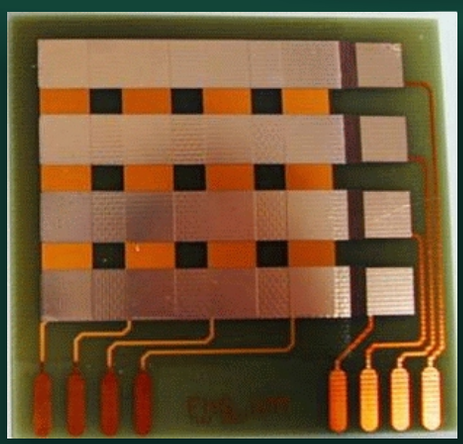
FACULTY OF ELECTRICAL ENGINEERING AND INFORMATION TECHNOLOGY

CENTER FOR MICROTECHNOLOGIES

ANNUAL REPORT 2007







ZfM

CHEMNITZ UNIVERSITY
OF TECHNOLOGY

Information online: www.zfm.tu-chemnitz.de

Chairman's letter

Dear ladies and gentlemen,

The year 2007 was a very successful year. As in preceding years, the Center for Microtechnologies in close cooperation with the Branch Chemnitz of the Fraunhofer Institute for Microintegration and Reliability (Fraunhofer IZM, headquarter Berlin) has further consolidated its position as a Center of Excellence in the fields of micro- and nanoelectronics back end technologies and micro- and nanosystem technologies.

The key to our success was an interdisciplinary cooperation of several chairs within the ZfM. Based on this idea, ZfM's primary mission is to provide an intellectual and working environment that makes possible student education and research in areas that require or may benefit from advanced ULSI-interconnect technologies, Si-nanotechnology and new developments and ideas in the field of MEMS/NEMS by using microfabrication technologies. ZfM's technology laboratories provide a complex of modern microelectronics laboratories, clean rooms and microfabrication facilities.

We are very pleased that Prof. Dr. Jan Mehner and Prof. Dr. John-Thomas Horstmann were elected as new members of the board of directors of the ZfM in 2007. Prof. Jan Mehner has replaced Prof. Wolfram Dötzel, who retired 2007. Prof. John-Thomas Horstmann has replaced Prof. Gunter Ebest, who also retired 2007. We would like to thank Prof. Wolfram Dötzel and Prof. Gunter Ebest for their long term contribution within the ZfM, especially for their very successful participation in the Collaborative Research Center "Arrays of micromechanical sensors and actuators".

We spent a lot of effort in the year 2007 regarding the organisation and design of the Smart Systems Campus Chemnitz nearby our already existing buildings. Starting in the year 2006 the construction of new buildings for

- cleanroom facilities of the ZfM together with the Institute of Physics of the TU Chemnitz
- the Branch Chemnitz of the Fraunhofer IZM
- facilities for start up companies

is carried out. The new clean room of the Center for Microtechnologies within the building of the Institute of Physics was finished in 2007.

The 2007 Annual Report of the Center for Microtechnologies provides an overview of the facilities, staff, faculty and students associated with the ZfM, as well as a description of many of the ongoing research projects which make use of the ZfM facilities.

These developments, which are based on close links with industry and cooperation with German as well as international institutes, contribute to an advanced education for our students. We kindly acknowledge the support of the Federal Ministry of Research, the German Research Foundation, the Saxon Ministry of Science and the European Commission.

As always, we are driven by our triple aims of excellence in education, scientific and technological research and by providing a comprehensive range of research and development services to industry.

Thomas Gessner
President of the Center for Microtechnologies
Director of Chemnitz Branch of Fraunhofer IZM

Contents

Center for Microtechnologies

Highlights in the year 2007

The year 2007 startet with the final presentation of the **Collaborative Research Center (SFB) No. 379 : „Arrays of micromechanical sensors and actuators“**. This SFB dealt with the realization of sensor and actuator arrays consisting of a number of single components. New technologies among them the AIM technology have been developed. The final results have been demonstrated to partners from industry and research during the fair SIT on March 1st 2007 in Chemnitz.

Fig.1: Prof. Dr. Dieter Tischendorf, Prof. Dr. Thomas Gessner, and Prof. Dr. Dietrich Zahn at ceremonial kick-off presentation of Smart Systems Campus Chemnitz

In early June the deputy director of the Chinese Academy of Sciences, Prof. Yu De Yu, conferred the title of visiting professor at the Institute of Semiconductors on Prof. Thomas Gessner to acknowledge his outstanding contribution to micro and nano technology as well as system integration. With about 1000 employees the Institute of Semiconductors at the Chinese Academy of Sciences in Beijing is one of China's biggest research institutions.

On July 9th 2007 the ceremonial kick-off presentation of the **Smart Systems Campus Chemnitz** at the Chemnitz University of Technology took place. The Smart Systems Campus provides a pool of microsystems technology expertise in a dynamic network in Chemnitz. The park provides a home for renowned scientific and technical institutes and links them to a pioneering spirit, entrepreneurship and an economic upswing right on the doorstep. The Center for Microtechnologies as well as the branch Chemnitz of the Fraunhofer Institute for Reliability and Microintegration belong to this campus. The Center for Microtechnologies got a new clean room within this campus, which was finished in December 2007.

Since November 2007 Prof. Thomas Gessner works as a Principal Investigator in the World Premier International Research Center of the Tohoku University Sendai. The main objective of the center is to promote the development of new materials under world-leading organization for interdisciplinary research in functional materials, by use of an innovative method of atom and molecular control, departing from the typical approaches and moving towards the next generation. The center will pursue the creation of new compounds and materials with innovative functions with exceed the existing ones, the construction of devices based on a new fundamental paradigm and the promotion of applied research projects on materials and system architecture that will generate direct social impacts. Main task of the common research are system integration issues of advanced materials and technologies.

Fig.2: New clean room (clean room class 10) in the new building of the Institute for Physics

In December 2007 the new clean room (clean room class 10) has been finished.

Center for Microtechnologies

The Center for Microtechnologies (ZfM) founded in 1991, belongs to the department of Electrical Engineering and Information Technology of the Chemnitz University of Technology. It is the basis for education, research and developments in the fields of micro and nano electronics, micro mechanics and microsystem technologies in close cooperation with various chairs of different TUC departments.

The ZfM's predecessor was the "Technikum Mikroelektronik" which was established in 1979 as a link between university research and industrie. For that reason the Chemnitz University of Technology has had a tradition and experience for more than 30 years in the fields of microsystem technology, micro and nanoelectronics, as well as opto-electronics and integrated optics.

Within 2007 two professors left the Center for Microtechnologies. At this place we want to thank again Prof. Wolfram Dötzel and Prof. Gunter Ebest for their scientific work, their commitment and their support. The work will be continued based on the traditions but with new ideas by the new professors Prof. Jan Mehner and Prof. John-Thomas Horstmann.

The ZfM carries out basic research, practical joint projects and direct research & development orders for the industry in the following fields:

- Basic technologies and components for microsystems and nanosystems (sensors, actuators, arrays, back end of line)
- Design of components and systems
- Nanotechnologies, nanocomponents and ultrathin functional layers

In education, the specified and related topics are taught in the basic and main courses.

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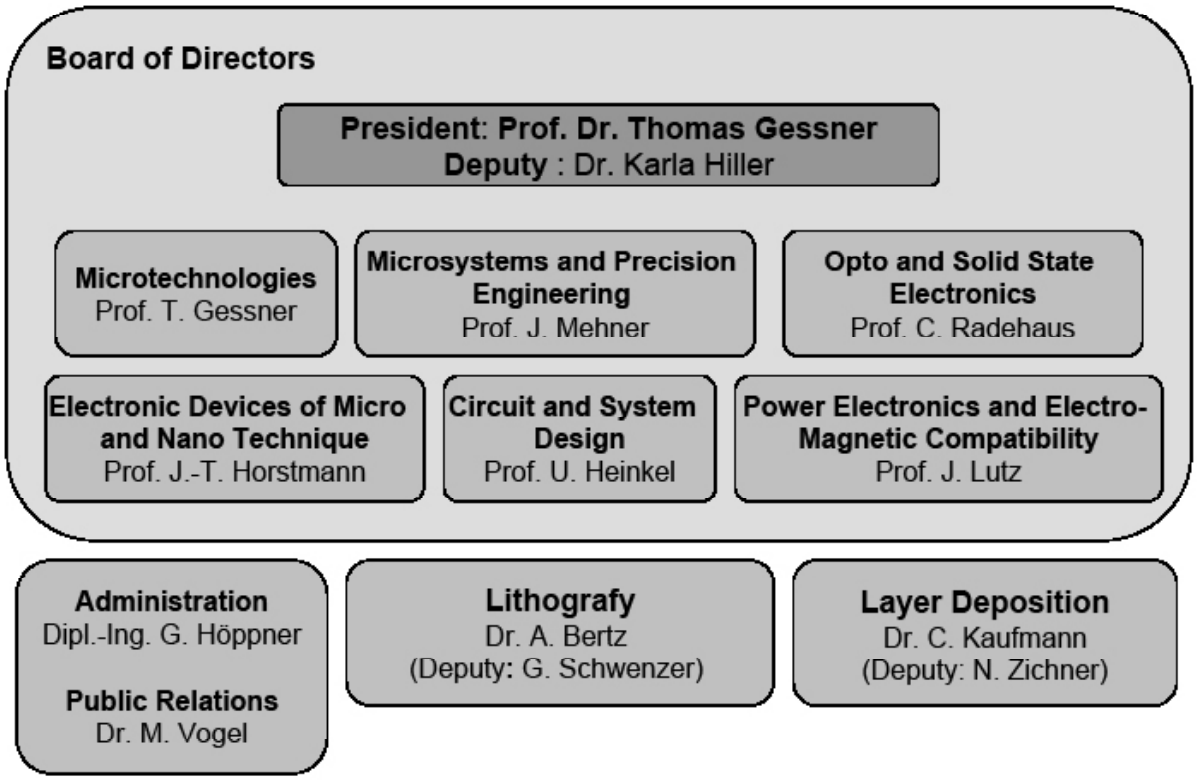


Chair Microtechnology

Contact: Prof. Dr. Thomas Gessner

Phone: +49 (0) 371 531 33130

Email: thomas.gessner@zfm.tu-chemnitz.de

Main working fields:

- Development of new materials and processes for metallization systems in micro and nanoelectronics
- Development of technologies and components for micro and nano systems (sensors, actuators and arrays)
- Development of nanotechnologies, nano components and ultra-thin functional films
- Simulation of equipment and processes for micro and nanoelectronics

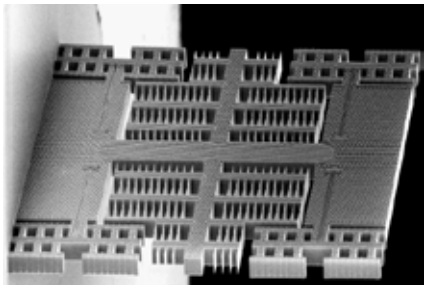


Fig.1: Seismic mass of an acceleration sensor in AIM technology

Research focus on:

- ULSI metallization
- High temperature stable metallization
- Copper metallization/ diffusion barriers/CMP
- Carbon nano tubes
- Low k dielectrics/ air gap structures for ultra low – k values
- micromechanical elements and arrays, MEMS/NEMS
- Inertial sensors (acceleration sensors, inclination sensors, gyroscopes)
- Actuators (mirrors)
- Integrated optics (spectrometer)
- RF-MEMS
- Polymer-MEMS and systems
- MEMS/NEMS technologies - Air gap insulated microstructures, bulk microstructures, high aspect ratio microstructures
- Analysis of micromechanical systems
- Integrated optics
- Wafer bond techniques
- MEMS packaging on wafer level

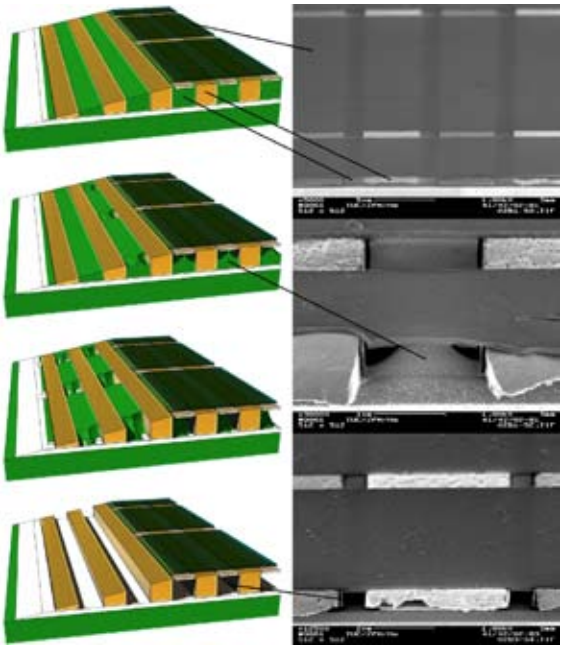


Fig.2: Airgap structures for low parasitic coupling in advanced interconnect systems

Chair Microsystems and Precision Engineering

Contact: Prof. Dr. Jan Mehner

Phone: +49 (0)371 531 36652

E-Mail: jan.mehner@etit.tu-chemnitz.de

The professorship is focused on design and experimental characterization of Microsystems and their applications in precision engineering. Innovative technologies are investigated in order to link mechanics, optics, electrical engineering and electronics for highly integrated smart products.

Research topics are:

- Modeling and simulation of physical domains and their interactions
- Experimental characterization and measurement methodologies
- Sensor and actuator development
- Wireless communication and energy scavenging
- Microsystems are key components of complex heterogeneous devices such as automotives products, industrial automation and consumer applications
- Academic research and education is strongly related to partners as industrial enterprises, Fraunhofer Institutes, software companies

Examples are

- Accelerometers and gyroscopes
- Micro mirrors for image projection
- Vibration sensor for process control
- Sensor networks and communication
- Flow rate sensors and vacuum gauges
- Components for medical applications

The effects of Microsystems technology on intelligence, reliability, energy consumption, volume, mass and costs of market products will be dramatic, similar to the replacement of electronics based on discrete components by microelectronics in the early 1970s.

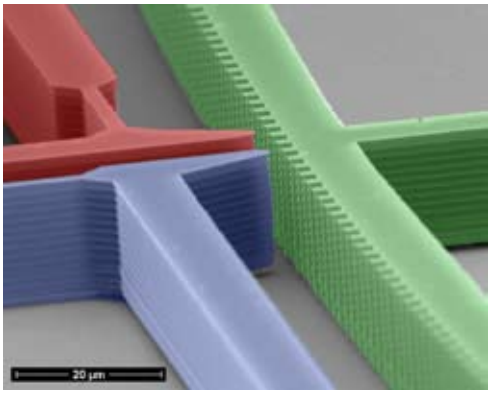


Fig.1: Step gear system for micro positioning applications

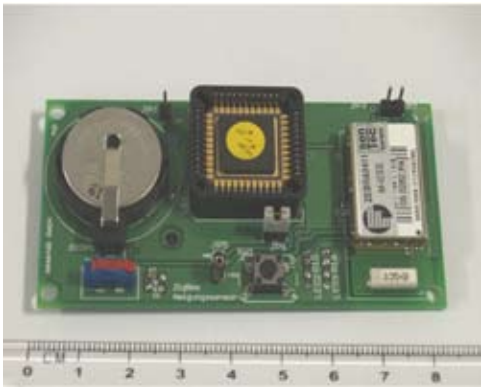


Fig.2: Wireless sensor node developed for MEMSFAB GmbH

Chair Circuit and System Design Chair

Contact: Prof. Dr.-Ing. Ulrich Heinkel

Phone: +49 (0)371 531 24310

E-Mail: ulrich.heinkel@etit.tu-chemnitz.de

Main working fields:

- design of ASICs (Application Specific Integrated Circuits) and FPGAs (Field Programmable Gate Arrays)
- design of heterogeneous systems (MEMS)
- design support and optimization by means of novel approaches, methodologies and dedicated design tools
- component (hardware and software) reuse
- high performance arithmetic
- digital image processing
- formal specifications capturing for analogue, digital and heterogeneous systems with VHDL, VHDL-AMS, SystemC, SystemC-AMS
- reconfigurable computing

During many years of work in the area of circuit and system design, an extensive knowledge in application specific integrated circuits (ASIC) design has been accumulated. Special know-how and experience exist in the field of PLD and FPGA (field programmable gate arrays) design and application. Many different systems have been designed, e.g. for real time processing, rapid prototyping systems for image processing, vibration pattern recognition systems and coupling of simulators and emulators.

Research areas include:

- system design of heterogeneous microsystems in co-operation with the Chair of Microsystems and Precision Engineering and the Center of Microtechnologies,
- research work in logic and system design and application of FPGAs and PLDs,
- high performance arithmetic for different special purposes (e.g. MPEG video decoders, image compression, graphic controllers),
- design of re-usable components and IP (Intellectual Properties), development of design environments for re-usable components and applications,
- specification capturing, formal specification with interface-based design methods,
- utilisation of fuzzy accelerators for recognition of vibration patterns and classification (noise analysis),
- development and application of a modular system (including graphical user interface) for real time functions (inspection of textile surfaces, analysis of skin diseases, real time image processing, fuzzy classification systems, controlling of projection systems),
- design and evaluation of high performance data path components,
- Low Power Design (system bus encoding techniques for reduced power dissipation)

Electronic Devices of Micro and Nano Technique

Contact: Prof. Dr. John-Thomas Horstmann

Phone: +49 (0)371 531 37114

E-Mail: john-thomas.horstmann@etit.tu-chemnitz.de

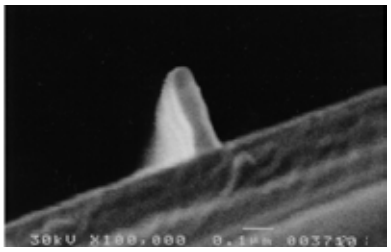
Main topics in the research activities of the "microsystem electronics" working group at the Chair of Electronic Devices of Micro and Nano Technique are the development of integrated microsystem front end electronics

The field of activity comprises:

- design of integrated high voltage circuits for electrostatically driven micro actuators
- characterisation and modelling of high voltage micro technology devices
- design of low power and low noise integrated circuits for signal editing of micro-mechanical sensor arrays, and
- electrical characterisation of microsystems.

Main working fields:

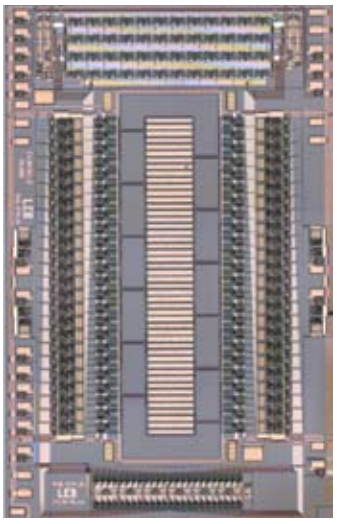
- Manufacturing, analysis and characterization of next-generation nanoelectronic devices
- integrated circuit design for microsystem electronics
- modelling and simulation of electronic devices for microsystem electronics



Main research topics of the "next-generation nanoelectronic devices" group at the Chair of Electronic Devices of Micro and Nano Technique are:

- fabrication and experimental characterization of sub-50 nm-MOS-transistors
- development of strategies to reduce the statistical parameter fluctuations of very small MOS-transistors
- invention of new materials in the CMOS-process for next generation nano-devices

Competence in integrated circuit design of the working group starts from linear amplifier circuits with an electrical strength of several hundreds of volts up to low voltage signal processing circuits in switched-capacitor technique.



Electrostatic driven micromechanical components with capacitive behaviour referring to their terminals include micro mirrors rotating in one or two dimensions and transducers based on the piezoelectric effect. Front-end circuits which are used to control such microelements for various applications have to be smart power amplifiers with the ability to drive up to 1000 V. Various examples of such circuits have been demonstrated over the last years.

Chair Opto and Solid State Electronics

Contact: Prof. Dr. rer. nat. Christian Radehaus

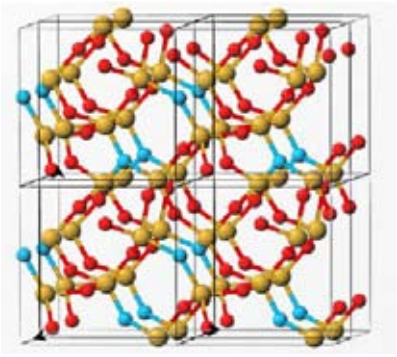
Phone: +49 (0)371 531 33085

E-Mail: cvr@zfm.tu-chemnitz.de

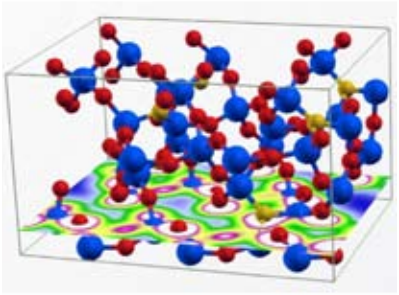
Main working fields:

First principle simulation of electronic, optical and mechanical properties of solids

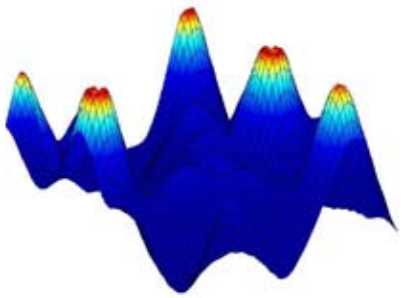
- Determination of bulk and interface structures, Classical Monte Carlo (CMC) and Classical Molecular Dynamics (CMD)



- Calculation of electronic band structures -including GW methods- and dielectric constants
- Modeling thermal stability using classical and ab initio molecular dynamics
- Electronic structure of crystalline and amorphous SiOxNy materials



- Si-Insulator Interfaces
- Simulation of defects and their influence



- Developing of new transport models for the leakage current in CMOS structures

Quantum mechanical simulation of electronic devices

- computation of gate tunneling current in MOSFETs with single and multilayer gate stacks

Interaction of molecules with solid state surfaces

- cleaning und sticking problems of various substances on surfaces

Chair Power Electronics and Electromagnetic Compatibility

Contact: Prof. Dr. Prof. h.c. Josef Lutz

Phone: +49 (0)371 531 33618

Email: josef.lutz@etit.tu-chemnitz.de

The education covers power devices, thermo-mechanical problems of power electronic systems, power circuits and electromagnetic compatibility. The focus of research is on power devices, especially their reliability. Actually the main working fields are

- Dynamic avalanche and ruggedness
- Diamond like carbon a-C:H
- Packaging technologies, thermal simulation and reliability
- Double layer capacitors - applications, reliability.

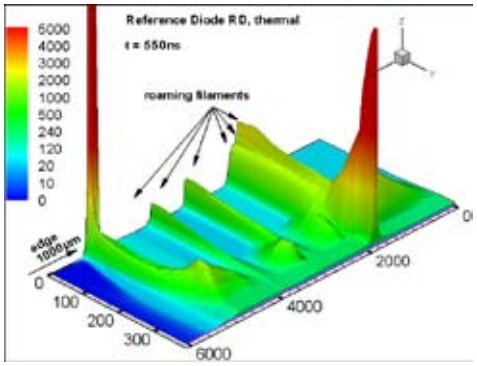


Fig.1: Simulation of current tubes at strong dynamic avalanche in a 3.3kV power diode.

Dynamic avalanche occurs in bipolar power devices at high switching slopes, as well as in ESD protection structures. A feedback between free carriers and the electric field exists in dynamic avalanche. At strong dynamic avalanche the current flows no longer homogeneous, but in current tubes or filaments (Fig. 1). Uncritical and critical situations are investigated. Also other high-stress conditions are analysed experimental and in numerical simulations, e.g. surge current and short circuit, for devices of Si and of SiC.

In the field of reliability, several power cycling stations have been build from 50A up to 400A DC current. Fig. 2 shows an example of bond-wire lift-off. Additional failure mechanisms occur in solder layers etc.

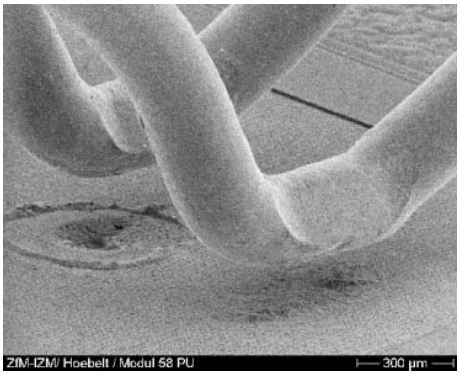


Fig.2: Bond wire lift-off at an IGBT-die after 18000 cycles with ΔTj 100K

For reliability investigations, further test stations for hot-reverse-tests and high humidity high temperature reverse bias tests are available. In the main fields of research is a close cooperation with professional industry companies in power semiconductors, packaging and automotive. A special interest is in projects to save electrical energy by high efficiency power electronic systems and in applications in renewable energy systems.

Fraunhofer Institute for Reliability and Microintegration IZM
Branch Chemnitz

Director: Prof. Thomas Gessner
Deputy: Dr. Thomas Otto

Since 1998 a strong co-operation exists between the Fraunhofer Institute for Reliability and Microintegration (Fraunhofer IZM, Berlin, Munich & Chemnitz) and the Center for Microtechnologies. Due to the positive development of the branch Chemnitz the Executive Board of the Fraunhofer Gesellschaft decided to build a new building for the branch Chemnitz of the Fraunhofer IZM. The groundbreaking ceremony took place on November 5th 2007. Prof. Buller pointed out in his talk: "With the new building and the new equipment in Chemnitz we support developments in nano and micro system technology, which belongs to German key technologies. This will help Saxon businessmen to transfer research results in products ready for the market in short time."

The new building of Fraunhofer IZM Chemnitz belongs to the Smart Systems Campus Chemnitz, which is a pooled dynamic network of Microsystems expertise in Chemnitz. Local synergies can be exploited once the Smart Systems Campus has been setup in 2009. A close network of science, research and industry will then not only be a pipe dream, but it is a specific element in the concept.

Fig.1: New building of the Fraunhofer IZM, branch Chemnitz

Now, the main focus of the branch Chemnitz is the smart systems integration. In near future systems will be quite more intelligent and multifunctional e. g. the integration of electronics for signal and information processing with sensors and actuators in silicon and nonsilicon technologies. The main research activities of the IZM branch Chemnitz can be divided in the following topics:

Multi Device Integration: development of MEMS/NEMS, prototyping of sensor and actuator devices, integration of such devices together with micro and nanoelectronic components to systems, design of component and systems, , development and implementation of test and characterization of MEMS/NEMS. Examples are micro mirror spectrometer or micro projection systems.

Development of Advanced Technologies: core competence in development and application of wafer bonding processes for MEMS Packaging (chip and wafer bonding including combinations of new materials and bonding at low temperatures), 3D-patterning technologies for silicon and non silicon materials, CMP (chemical mechanical polishing)

Back end of Line (BEOL): advanced metallization systems for the leading edge technology, 3D integration and interconnects, new materials (cupper, low k materials, CNTs,…) for advanced metallization, Simulation of process and equipment

Reliability of Micro and Nano Systems: thermo-mechanical reliability of micro and nano components in high tech systems, core competence combination of thermo-mechanical simulation with advanced experimental methods.

Printed Functionalities: utilizing inkjet and mass printing technologies for efficient industrial fabrication processes of printed components for smart systems, technology development and adapted measurement technique.

In general the strategic alliance between the Fraunhofer Institute for Reliability and Microintegration and the Center for Microtechnologies as described ensures strong synergies in the technology and device development.

Fig.2: Smart Systems Campus Chemnitz with the building of the Institute of Physics with cleanroom of ZfM (left side), the building of Fraunhofer IZM (in the middle) and the start-up building (right side)

Co-operations with industry and research institutes

Partnerships with the following companies and institutes were continued and / or established in 2007:

Advanced Micro Devices (AMD), Dresden, Germany
Agilion GmbH, Chemnitz, Germany
Air Products and Chemicals, Inc., Electronic Materials, Allentown (PA) and Carlsbad (CA), USA
Aktiv Sensor GmbH, Stahnsdorf, Germany
Alpha Microelectronics GmbH, Frankfurt (Oder), Germany
Alcatel-Lucent Deutschland AG, Nürnberg, Stuttgart, Germany
ALTATECH Semiconductor, Montbonnot, France
AMD Dresden, Germany
AMTEC GmbH, Chemnitz, Germany
Anfatec Instruments, Oelsnitz, Germany
ALSTOM Transport Tarbes, France
ASMEC Advanced Surface Mechanics GmbH, Radeberg, Germany
Atmel Design Center, Dresden, Germany
AUDI AG, Ingolstadt, Germany

BMW AG Munich, Germany
Robert Bosch GmbH, Reutlingen & Stuttgart, Germany

Cabot Microelectronics Europe
CAD-FEM GmbH Grafing, Germany
CiS Institut für Mikrosensorik gGmbH, Erfurt, Germany
CNRS, Grenoble, France
Colour Control Farbmeßtechnik GmbH, Chemnitz, Germany
Conti Temic microelectronic GmbH, Nürnberg, Germany
Core Mountains GmbH, Chemnitz, Germany

DaimlerCrysler AG, Research Lab Ulm & Sindelfingen, Germany
Danfoss Silicon Power, Schleswig, Germany
Digital Instruments – Veeco Instruments, Mannheim, Germany
DILAS Diodenlaser GmbH, Germany

EADS Deutschland GmbH, Corp. Res. Ctr. Germany, Dept. Microsystems, München, Germany
Endress und Hauser Conducta GmbH & Co. KG, Germany
Eupec GmbH Warstein, Germany

FACRI , Research Institute, Xi´an, China
Fahrzeugelektrik Pirna GmbH, Pirna, Germany
FHR Anlagenbau GmbH, Ottendorf-Okrilla, Germany
First Sensor Technology GmbH, Berlin, Germany
FLEXIVA automation & robotics, Amtsberg, Germany
Forschungszentrum Rossendorf, Germany
Fraunhofer Institut für Nachrichtentechnik, Heinrich-Hertz-Institut, Berlin, Germany
Fraunhofer Institut für Siliziumtechnologie, Ithehoe, Germany
Fujitsu Microelectronic GmbH, Dreieich-Buchschlag, Germany

Gesellschaft für Mikroelektronikanwendung Chemnitz mbH (GEMAC mbH), Chemnitz, Germany
GF Messtechnik Teltow, Germany
Gesellschaft für Prozeßrechnerprogrammierung mbH (GPP) Chemnitz, Germany
GHF IWM Halle, Germany
Gyrooptics Company Ltd., St. Petersburg, Russia

Heinrich-Hertz-Institut Berlin, Germany
Hitachi Ltd., Japan

IHP, Frankfurt/Oder, Germany
IMEC, Leuven, Belgium
IMST GmbH, Camp-Lintfort, Germany
Infineon Technologies AG, Munich, Dresden and Warstein, Germany
Infineon Technologies AG, Villach, Austria
InfraTec GmbH, Dresden, Germany
Institut für Festkörper- und Werkstoffforschung e.V. IFW Dresden, Germany
Intelligente Sensorsysteme Dresden GmbH, Germany
iSyst Intelligente Systeme GmbH, Nürnberg, Germany
ITIM International Training Center for Material Science, Vietnam
IXYS Semiconductor GmbH, Lampertheim, Germany

Jenoptik-LDT GmbH, Gera , Germany

Kyocera Fineceramics GmbH, Germany

L.A.A.S-C.N.R.S. Toulouse, Prof. Dr. D. Esteve, France
LETI, Grenoble, France
LG Thermo Technologies GmbH, Germany
Lionix, Enschede, The Netherlands
LITEF GmbH, Freiburg, Germany
Lucent Technologies, Nürnberg, Germany

Massachusetts Institute of Technology, Cambridge / Boston, Mass., USA
Max-Planck-Institut (MPI) für Mikrostrukturphysik Halle, Germany
Mechanical Engineering Laboratory AIST, MITI, Dr. Mitsuro Hattori and Chisato Tsutsumi, Tsukuba, Ibaraki, Japan
memsfab GmbH, Chemnitz, Germany
Mesa Research Institute, Prof. J. Fluitman, Twente, The Netherlands
Microtech GmbH, Gefell, Germany
Mitsui Engineering and Shipbuilding Co. Ltd., Japan
MPA NRW Materialprüfungsamt Nordrhein-Westfalen, Germany

Neumann Elektrotechnik GmbH, Chemnitz, Germany
Nex Systems, Wilmington, MA., USA and Berlin, Germany
NICO Pyrotechnik, Trittau, Germany
NXP (founded by Philips), Leuven, Belgium
NXP Semiconductors GmbH, Dresden, Germany

Océ B.V., Venlo, The Netherlands
OEC GmbH, Germany

Panasonic Plasma Display Dev. Lab., Inc., Highland, New York, USA
PANTA GmbH, Germany
Peppercon AG, Zwickau, Germany
Physikalisch-Technische Bundesanstalt Braunschweig (PTB), Germany
Philips Applied Technologies, Eindhoven, The Netherlands
PLASMACO Inc. Highland, New York, USA
Preh GmbH, Bad Neustadt, Germany
PRETTL Elektronik Radeberg GmbH, Germany

Qimonda AG, Dresden, Germany

Raritan AG, Zwickau, Germany
Raytek GmbH Berlin, Germany
Ricoh Company, Ltd., Yokohama, Japan
Rohm and Haas Electronic Materials, Marlborough, USA
Roth & Rau Oberflächentechnik GmbH, Wüstenbrand, Germany
RWE Schott Solar GmbH, Alzenau, Germany

Sana Herzzentrum gGmbH, Cottbus, Germany
Sarnoff Europe, Aalter, Belgium
SAW Components, Dresden, Germany
Schenker Deutschland AG, Dresden, Germany
Schott Mainz & Schott Glas Landshut, Germany
Sentech Instruments GmbH, Berlin, Germany
SICK AG, Waldkirch & Ottendorf-Okrilla, Germany
SF Automotive GmbH, Freiberg, Germany
Siegert TFT GmbH, Hermsdorf, Germany
Siemens AG, München, Germany
Siemens A&D ATS2 Nürnberg und AT Regensburg, Germany
Siemens VDO Automotive AG, Limbach-Oberfrohna, Germany
Signalion GmbH, Dresden, Germany
SiMetricS Silicon Metrological Components and Standards GmbH, Limbach-Oberfrohna, Germany
Institut für Solarenergieforschung Hameln-Emmerthal, Germany
Sony Corp., Semiconductor Business Unit, Japan
ST Microelectronics, Crolles, France and Agrate, Italy
Suss Microtec AG Munich and Sacka, Germany

TEKA Absaug- und Entsorgungstechnologie GmbH, Germany
Teleca Systems GmbH, Nürnberg, Germany
Dr. Teschauer AG, Chemnitz, Germany
Thales-Avionics, Valence and Orsay, France
TranSiC, Kista/Stockholm, Sweden
TRW Airbag Systems GmbH & Co. KG, Aschau/Inn, Germany

Unicontrol Systemtechnik GmbH, Germany

X-FAB Semiconductor Foundries AG, Erfurt, Germany

ZF Friedrichshafen AG, Friedrichshafen, Germany
ZMD Dresden, Germany

3D-Micromac AG, Chemnitz, Germany

Co-operations with universities

Austria
Atominstitut Universität Wien, Austria
Johannes Kepler Universität Linz, Austria

China
Chongqing University, Chongqing, China
Fudan University, Shanghai, China
Shanghai Jiao Tong University, China
TSINGHUA University, Beijing, China
Xiamen University, Xiamen, China

Czech Republic
University of West Bohemia, Pilsen, Czech Republic

Germany
Brandenburgische Technische Universität Cottbus, Germany
HTW Mittweida, Laserapplikationszentrum, Germany
Technische Fachhochschule Wildau, Germany
Technische Universität Berlin, Germany
Technische Universität Braunschweig, Germany
Technische Universität Dresden, Germany
Technische Universität Ilmenau, Germany
Universität Bremen, Germany
Universität Erlangen, Germany
Universität Essen, Institut für anorganische Chemie, Germany

Hungary
Technological University Budapest, Hungary

Japan
Tohoku University, Sendai, Japan
University of Tokyo, Res. Ctr. for Adv. Science & Technology (RCAST), Japan

The Netherlands
University of Delft, The Netherlands
University of Twente – MESA, The Netherlands

Norway
Norwegian University of Science and Technology (NTNU), Trondheim, Norway

Poland
Warsaw University of Technology (WUT), Warsaw, Poland

Russia
North Caucasus State Technical University, Stavropol, Russia
Nowosibirsk State University, Russia

Singapore
Technological University Singapore, Singapore

UK
Cardiff University, Cardiff, UK
University of Hertfordshire, UK
Universtiy of Newcastle, UK

USA
Case Western Reserve University, Cleveland, Ohio, USA
Portland State University, Portland, Oregon, USA
Rensselaer Polytechnic Institute (RPI), Troy, N.Y., USA
University of California at Berkeley, Berkeley Sensor and Actuator Center, USA
University of Colorado at Boulder, USA
University of Nevada, Reno, USA

Vietnam
Hanoi University of Technology, Vietnam

Networks

Networking is our formula for success. The Center for Microtechnologies is working in several national and international networks.

Silicon Saxony

Silicon Saxony e.V. is Europe's largest trade association for the microelectronic industry. It was founded on 19th December 2000 as a network for the semiconductor, electronic and micro system industry. The association connects manufacturers, suppliers, service providers, colleges, research institutes and public institutions in the economic location of Saxony. The current number of members has risen to 256. The member companies employ about 25,000 people and the total turnover of the companies is 3.5 billion € per year. The ZfM belongs to the foundation members.

10 working groups are working within the network. The working group "Smart Integrated Systems" has been founded on October 15th 2007 during the 2nd Micro System technology Congress in Dresden. It is leaded by Prof. Thomas Gessner.

IVAM

As international association of companies and institutes in the field of microtechnology, nanotechnology and advanced materials, IVAM's priorities are to create competitive advantages for our members. 261 member companies and institutes from 18 countries open up new markets and set standards with the support of IVAM. Companies, institutes, products, services and contact persons are listed online as well as in the printed IVAM directory. The Center for Microtechnologies is a member of the IVAM network since 5th January 2005.

Within 2007 Prof. Gessner became a member of IVAM Advisory Council. The IVAM Advisory Council helps impulses from application oriented science to be integrated into the work of the association. Apart from their consulting function, the members of the IVAM Advisory Council also represent IVAM in public.

Nanotechnology Center of Competence "Ultrathin Functional Films"

The Center of Competence "Ultrathin Functional Films" (CC-UFF) is coordinated by Fraunhofer-Institute IWS Dresden. It joins 51 enterprises, 10 university institutes, 22 research institutes, and 5 corporations into a common network. Activities within the frame of Nano-CC-UFF are subdivided into 6 working groups, every one of which is administered and coordinated by one member.

WG 1: Advanced CMOS
WG 2: Novel components
WG 3: Biomolecular films for medical and technological purposes
WG 4: Mechanical and protective film applications
WG 5: Ultrathin films for optics and photonics
WG 6: Nano-size actuators and sensors

nanotechnologie
CC "Ultradünne funktionale Schichten"

The heads of two working groups belong to the board of directors of the Center for Microtechnologies. These two working groups are described more detailed below.

Advanced CMOS

Structural widths of about 100nm are state-of-the-art in CMOS technology. A reduction down to below 50nm within 10 years, for further miniaturization, is envisaged by the International Technology Roadmap for Semiconductors ITRS (by Semiconductor Industry Association (SIA) and SEMATECH). Along with this trend, higher frequency and reliability are required. This implies novel developments in materials and processes for both the active elements and the interconnect system, including advanced equipment for larger Si-wafer production. High k dielectrics will be applied to ensure further scaling of effective gate oxide thickness. Most present-day interconnect systems are made of contacts (e.g. titanium or cobalt silicide), barrier layers (TiN, TiW), isolating interlayers (SiO2 and low-k dielectrics like FSG, OSG), interlayer connections and conducting paths (Al-alloys and Copper). Copper with its high conductivity and stability with respect to electromigration has been introduced as conductor material leading to higher frequency and reliability. This requires the availability of suitable barrier layers suppressing interdiffusion and reactions. The barrier layers must not affect the conductivity of the paths remarkably, which requires ultra-thin films. Interfaces and nanometer scale effects become increasingly important.

Head of the Working Group: Prof. Dr. Thomas Gessner, Chemnitz University of Technology

Novel components

The continuing trend towards miniaturization of integrated circuits has given rise to increasing efforts to supplement and gradually replace conventional CMOS-technologies by nanotechnologies and nanoelectronics in near future. The latter include magneto-electronics, and single electron devices, nanocluster storage elements, and resonant tunneling elements, among others.

Magnetoelectronics is based on the concept of replacing semiconductor magnetic field sensors (Hall sensors) in multi-layer systems by Giant Magneto Resistance (GMR) sensors, and CMOS memories by persistent magnetic memories (M-RAMS). For this purpose it is necessary to deposit stacks of extremely thin metallic and insulating films of about 1nm thickness with well defined interfaces.

There is a new generation of novel components based on the transfer of individual electrons in nano-scale structures. Work centers on memory elements based on the transfer of individual electrons between metal electrodes and on the memory effect of semiconductor nano-clusters in SiO2 films.

Head of the Working Group: Prof. Dr. Christian Radehaus, Chemnitz University of Technology

Network Mikro- und biosensorische Messtechnik

The Center for Microtechnologies works together with other institutes and companies within the network micro and biosensoric measuring technique. This network is a Saxon one and is focussed on new materials, surface modification, micro systems, sensor principles and peripheral devices.

Mikro- und biosensorische
Messtechnik

Equipment and service offer

The ZfM facilities include 1000m² of clean rooms (300m² of them class 10). Modern equipments were installed for processing of 100 mm, 150mm and 200 mm wafers as well as design and testing laboratories providing the basis for the following processes, partly in cooperation with the Fraunhofer Institute IZM, branch Chemnitz:

Design

- MEMS/NEMS,
- IC, ASICs and FPGAs
  - » low power and low noise, analogue-mixed signal integrated circuits
  - » integrated high-voltage circuits
- Design Support
- Optimization by means of novel approaches, methodologies and dedicated design tools
- Design for reliability

Modelling and Simulation

- Equipment and processes for micro and nanoelectronics
- Physical domains and their interaction
- Thermal simulation
- Electronic devices
- Defects and their influence

Mask fabrication

- 3" ... 7"
- Electron beam lithography
- Proximity and contact double-side

Characterization and Test

- MEMS/NEMS
- Nanoelectronic devices
- Parametric testing: Waferprober, HP Testsystem
- Characterization of analogue-mixed signal circuits up to 500 MHz
- Characterization and modelling of devices from low-voltage and high-voltage microtechnologies

Processes

- High temperature processes: Diffusion / Thermal oxidation / Annealing / RTP
- PVD (Cr, Au, Ag, Ti, TiN, Ta, TaN, Cu, Pt, Co, Al, W, TiW, $AlSi_x$, CrNi, MoNi, MOFe, Pyrex)
- Chemical vapor deposition CVD (MOCVD, PECVD, LPCVD)
  - » PECVD / LPCVD (SiO_2, Si_3N_4, Polysilicon, $Si_xO_yN_z$, SiCOH, SiCH)
  - » PECVD (diamond-like Carbon films, a-C:H)
  - » Cu-MOCVD, TiN-MOCVD
- Electroplating: Cu, Ni, Au
- Etching (dry: Plasma- and RIE-mode & wet: isotropic / anisotropic)
  - » Dry etching (Si, SiO_2, Si_3N_4, Polysilicon, Silicides, Al, refr. metals, TiN, Cr, DLC, low k dielectrics)
  - » Wet etching (SiO_2, Si_3N_4, Si, Polysilicon, Al, Cr, Au, Pt, Cu, Ti, W)
- Wafer lithography / Electron beam lithography
- Chemical mechanical polishing CMP (Copper, Silicon, SiO_2)
- Wafer bonding: silicon direct, anodic, eutectic, glass frit
- Packaging (sawing, bonding)

Analytics:

- Scanning electron microscopy SEM / EDX
- Atomic force microscopy AFM
- Variable angle spectroscopic ellipsometry
- Laser profilometry (UBM, TENCOR FLX-2900)
- Surface profilometer
- US-Microscope
- Tension/Compression testing machine Zwick 4660 universal
- Perkin-Elmer DMA 7e dynamic mechanical analyser
- Micromechanical testing instrument
- Lifetime scanner

Research activities

Research Projects

BMBF project "Active Smart ID-Label for transportation monitoring (ASIL)"
Project leader: Dr. F. Kriebel, KSW Microtec AG, Dresden
Partners: KSW Microtec AG Dresden, ELMOS Semiconductor AG Dortmund, Schenker Deutschland AG Dresden, ZfM TU Chemnitz
Project duration: 01.09.2005 - 31.08.2008
Project goal: Development, adaptation and integration of sensors for shock and tilt sensing within an active rf ID label

BMBF project „Modular Optical Analyser System (MOPAL)"
Project manager: Prof. T. Gessner
Partners: Endress+Hauser Conducta GmbH & Co. KG, COLOUR CONTROL Farbmesstechnik GmbH, SENTECH GmbH, Micro System Research Center of Chongqing University (VR China)
Project duration: 01.08.2004 - 31.07.2007 extended 31.07.2008
Project goal: Development and realization of an economical, efficient and universally applicable modular optical miniature analysis system for the spectral range from 300 nm – 10 µm.

BMBF project "Visualisierung mit halbleiterbasierten RGB Lasern im Automobil- und Consumerbereich - VISULASE"
Project leader: OSRAM Opto Semiconcuctors GmbH
Partners: FhG IZM Chemnitz, ZfM TU Chemnitz, FhG-IOF Jena, Robert Bosch GmbH, ELOVIS GmbH
Project duration: 01.10.2004 - 30.09.2007
Project goal: The goal of the project is the development of a complex micromechanical system for a head-up display in a car.

BMBF project „Technologie und Design für SOI-CMOS Bauelemente mit sub 50nm Gates (MOSTEDE)"
Project manager: Prof. C. Radehaus
Partners: AMD Saxony LLC & Co.KG, HTW Dresden
Project duration: 01.04.2004 – 31.03.2007
Project goal: Atomic scale modelling of new dielectrics for CMOS technologies
Subproject: Superrechnergestützte atomistische Modellierung neuartiger Dielektrika

BMBF project "Advanced Supercaps based on nanostructured materials (Nanocap®II)"
Project manager: Mr. P. Malcher, Brandenburgische Kondensatoren GmbH
Partners: FhG ISC Würzburg, Bosch Group, BMW Group, TU Chemnitz – Prof. Lutz
Project duration: 01.09.2005 – 31.08.2008
Project goal: Development of a new generation of supercaps with improved technical features

BMBF project "NMR Metabolic Profiling of the Stem Cell Niche (METASTEM)"
Project manager: Dr. Michael Cross, Universität Leipzig
Partners: ZfM TU Chemnitz, Universität Leipzig, Max-Planck-Institut für molekulare Genetik Berlin, NMR Service Erfurt
Project duration: 01.10.2006 - 30.09.2009
Project goal: Development of MEMS tunable capacitors for tuning and matching of highly sensitive dual channel NMR micro resonators.

BMBF project „Verdrahtungstechniken für besondere Geschwindigkeitsanforderungen in flüchtigen Speichern und Mikroprozessoren – High speed interconnects for volatile memories and microprocessors" – VERBINDEN
Project coordinator: AMD Fab36 LLC & Co. KG
Project manager: FhG-IZM: Dr. Stefan E. Schulz
Partners: AMD Fab36 LLC & Co. KG, Qimonda AG, Fraunhofer CNT
Subcontractors: Fraunhofer IZM Chemnitz / TU Chemnitz, TU Dresden, TU Berlin
Project duration: 01.04.2006 – 31.03.2009
Project goal: Subproject KUWANO (low resistivity copper interconnects): Development of processes and technology for fabrication of low resistivity Cu interconnect embedded in SiO_2 and dense low-k dielectrics for microprocessors in 45 and 32 nm technology node.

BMBF project Herkules „Hardwareentwurfstechnik für Null-Fehler-Designs"
Project manager: Prof. U. Heinkel
Partners: Lucent Technologies GmbH, Nürnberg (subprincipal)
Project duration: 01.12.2006 – 31.11.2009
Project goal: R & D work in the field of zero defect designs

BMBF project „Poröse Ultra-low-k Dielektrika: Abscheidung, Ausheilung, Strukturierung, Planarisierung und Integration – Porous ULK Dielectrics: Deposition, Patterning, Planarization and Integration“ – PULSAR
Project coordinator: AMD Fab36 LLC & Co. KG
Project manager: FhG-IZM: Dr. Stefan E. Schulz
Subcontractors: Fraunhofer IZM Chemnitz, TU Dresden
Project duration: 01.07.2006 – 30.06.2009
Project goal: Development of processes and technology for integration of porous ultra-low-k dielectrics into Cu interconnect systems for microprocessors in 45 and 32 nm technology node.

BMBF project Innoprofile „Generalisierte Plattform zur Sensordaten-Verarbeitung GPSV“
Project manager: Prof. U. Heinkel
Partners: Agilion GmbH; Gesellschaft für Mikroelektronik Anwendung Chemnitz mbH; Intelligente Sensorsysteme Dresden GmbH; Neumann Elektrotechnik GmbH; PANTA GmbH; Peppercon AG; PRETTL Elektronik Radeberg GmbH; Unicontrol Systemtechnik GmbH
Project duration: 01.04.2006 – 31.03.2011
Project goal: Development of a central universal control platform with standardized interfaces for sensor data processing, flexible solution for connecting sensors to the platform

BMBF project „Mx Mobile „Multi-Standard Mobile Platform“ Phase 1“
Project manager: Prof. U. Heinkel
Partners: Alcatel-Lucent Technologies GmbH, Nürnberg
Project duration: 01.03.2006 – 28.02.2009
Project goal: Development of a multi-standard mobile platform (mobile communication), modeling and verification of the system function, generation of program code, methods and platform of simulation

BMBF project URANOS „Analysemethoden für den Entwurf anwendungs-robuster nanoelektronischer Systeme“
Project manager: Prof. U. Heinkel
Partners: AMD Saxony LLC&Co.KG, Dresden (subprincipal)
Project duration: 01.07.2005 – 30.06.2008
Project goal: Development of methods for analysing application-robust nanoelectronical systems

Sub-project: “Supercomputer supported atomic scale modeling of new gate dielectric materials for sub 50 nm SOI-CMOS devices” – (SUGAMOND) of the BMBF-Project „Technologie und Design für SOI-CMOS Bauelemente mit sub 50nm Gates (MOSTEDE/SUGAMOND)”
Coordinators: Prof. Dr. rer. nat. C. Radehaus
Partners: AMD Fab36 LLC & Co., Dresden
Project duration: 01.04.2004 – 31.03.2007
Project goal: The main goal of this project was to develop methods for the application of first principle atomic scale calculations to the calculation of electronic properties of gate dielectric materials used in sub 50nm SOI-CMOS technologies. The main focus was on silicon oxynitrides (with different nitrogen concentrations) as a state-of-the-art gate dielectric material. The bulk properties (such as band gap, dielectric function) as well as the properties of Si/SiOxNy (valence and conduction band offset, density of the interface states) are investigated on an atomic scale. Finding an optimal tradeoff between gate capacitance and gate tunneling current is a major concern in designing gate dielectric of nano-MOSFETs. The implementation of a quantum mechanical model for the gate tunneling current was also one of the achieved goals of this project.

BMBF project Netz der Zukunft - Mx Mobile „Multi-Standard Mobile Platform“
(subprojct: Kostenmodellierung zur verbesserten Design Space Exploration)
Project manager: Prof. U. Heinkel
Partners: Alcatel SEL AG, Stuttgart; AMD DDC, Dresden; FhG-HHI Berlin; IHP, Frankfurt/Oder; IMST; Infineon, München; Alcatel-Lucent; Nokia; Philips Semiconductors Dresden; Siemens AG, München; Signalion GmbH; TU Dresden
Project duration: 01.03.2006 – 28.02.2009
Project goal: Cost modeling for improving design space exploration

BMBF program: “Micro-Nano-Integration für die Mikrosystemtechnik MNI-mst“
Project coordinator: Prof. Mehner
Partner: TU Berlin
Project duration: 01.04.2007 – 31.03.2008
Project goal: Development of movable micro and nano structures for low-cost sensors and actuators based on organic substrate materials.

BMBF project "Simulationskonzept für 32 nm-CMOS-Technologie - Simulation concept for 32 nm CMOS technologies" - SIMKON
Project coordinator: AMD Fab36 LLC & Co. KG
Project manager: FhG-IZM: Dr. Reinhard Streiter
Subcontractors: Fraunhofer IZM Chemnitz, TU Dresden
Project duration: 01.07.2007 – 31.12.2008
Project goal: PVD Simulation in sub 100 nm high aspect ratio features; Calculation and modelling of the line resistance for nanoscale Copper interconnects; Modeling of dielectric reliability in advanced interconnect systems

BWMI project „Super-Low-Temperature-Bonding für die Mikrosystemtechnik"
Project manager: M. Eichler, Fraunhofer IST
Partners: Zentrum für Mikrotechnologien Chemnitz, Aktiv Sensor GmbH, CiS GmbH, First Sensor Technology GmbH, Hellma GmbH & Co.KG, mikroglas chemtech GmbH, Planoptik AG, Siegert TFT GmbH, Softal electronic GmbH, Süss MicroTec AG
Project duration: 01.10.2007 – 30.09.2010
Project goal: Development and characterization of very low temperature bonding processes based on plasmamodified substrate surfaces

DFG Internationales Graduiertenkolleg – International Research Training Group (IRTG) "Materials and Concepts for Advanced Interconnects"
Project coordinators: Prof. T. Gessner (TU Chemnitz), Prof. Ran Liu (Fudan University, Shanghai, China)
Partners: TU Chemnitz, TU Berlin, Fraunhofer IZM, Fudan University Shanghai, Shanghai Jiao Tong University
Project duration: 01.04.2006 – 30.09.2010
Project goal: The IRTG is working to develop novel materials and processes as well as new concepts for connecting the devices within integrated microelectronic circuits. Smaller contributions are being made in the field of device packaging and silicides for device fabrication.

DFG project "Hotpressing of multifunctional standards for image processing microscopes for measurements on microsystems and nanostructures"
Project manager: Prof. J. Frühauf
Partner: Prof. E. Reithmeier, University of Hannover
Project duration: 01.04.2005 - 31.03.2007
Project goal: Development of pressing tools made out of silicon

DFG focus program: "Neue Strategien der Mess- und Prüftechnik für die Produktion von Mikrosystemen und Nanostrukturen SPP 1159/1"
Project coordinators: Prof. Mehner, Prof. Dötzel
Partners: University Bremen, University Erlangen, TU Braunschweig
Project duration: 01.10.2006 – 30.09.2008
Project goal: Development of methodologies for in-line measurement of dimensional and material properties of Si-microsystems based on teststructures.

DFG project "Development of X-ray optics from elements made by silicon microtechnology"
Project manager: Prof. J. Frühauf
Partner: Prof. B. Michel, FhG IZM Berlin
Project duration: 01.04.2006 - 31.03.2008
Project goal: Development of collimation slit systems made out of silicon

EFRE project „NMR-Mikroresonatoren zur Erstellung von Metabolit-Profilen hämatopoetischer Stammzellen"
Project manager: Dr. T. Riemer, Interdisziplinäres Zentrum für Klinische Forschung Leipzig
Partners: Zentrum für Mikrotechnologien Chemnitz, Universität Leipzig
Project duration: 01.07.2005 - 31.06.2007
Project goal: The goal of the project is the development of a nuclear magnetic resonance detector with very high sensitivity, suitable for analyzing small amounts of biological sample material.

EU project MORPHEUS: Multipurpose Dynamically Reconfigurable Platform for Intensive and Flexible Heterogenous Processing
Project manager (local): Prof. U. Heinkel
Project coordinator: Alcatel-Lucent Deutschland AG
Partner: ARTTIC, Paris, (France)
Project duration: 01.01.2006 – 31.12.2008
Project goal: Development of modular system-on-chip solutions, consisting of reconfigurable architectures and a software-based designflow

EU project "Surface Enhanced Micro Optical Fluidic Systems – SEMOFS"
Project manager: Dr. K. Hiller
Partners: CSEM (Switzerland), CEA (France), Cardiff University (UK), Bayer (Schweiz) AG (Switzerland), Eurogentec (Belgium), CHR Citadelle (Belgium), ALMA Consulting (France)
Project duration: 01.09.2005 – 31.08.2008
Project goal: Development of polymer based integrated probecards (including microfluidic and micro optical parts) for health diagnoses

Integrated project (IST) "PULLNANO": PULLing the limits of NANOcmos electronics
Project leader: ST Microelectronics SA (F)
Project manager: Prof. T. Gessner, Dr. S. E. Schulz
Partners: 35 partners involving main European IC manufacturers, research institutes, universities and SME's, e.g. Freescale Semiconductor (F), Infineon Technologies AG (D), NXP founded by Philips (NL, F), ST Microelectronics (F, I), IMEC Leuven (B), CNRS (F), CEA-LETI Grenoble (F), Fraunhofer (D), ACIES Europe (F)
Project duration: 01.06.2006 – 30.11.2008
Project goal: PULLNANO is a 30-month Integrated Project (IP) proposal for a powerful project focused on advanced RTD activities to push forward the limits of CMOS technologies. PULLNANO focuses on the development of 32 and 22nm CMOS technology nodes opening the way to the long term future of these technologies. The 1st objective of the project is the feasibility demonstration of 32nm node Front-End and Back-End process modules through a very aggressive SRAM chip and a multilevel metal stack structure. The 2nd objective is to realize research on the materials, devices, architectures, interconnects modelling and characterization to prepare the future 22nm node. The 3rd objective is to establish a common action between technology and design people in order to assess the technologies in terms of performances and power consumption. The 4th objective is to define, through a forum of European equipment suppliers, the specifications of future advanced process, characterization and metrology equipments. PULLNANO starts from the very successful NANOCMOS project focused on the 45nm technology.

SAB project „Entwicklung eines integrierten digitalen Sensors zur berührungslosen Längen- und Geschwindigkeitsmessung an bewegten nichtleitenden Materialien", Teilthema „Entwicklung einer digitalen Sensorsignalverarbeitung"
Project manager: Prof. U. Heinkel
Partner: Neumann Elektrotechnik GmbH, Chemnitz
Project duration: 01.06.2006 – 30.09.2007
Project goal: Development of a digital sensor signal processing

SAB compound project GEMO, part "Silicon basic components for instruments for the measurement of mechanical surface properties in the micro-nano region"
Project manager: Prof. J. Frühauf
Partners: Institut für Physik, Prof. F. Richter, TU Chemnitz, ASMEC Advanced Surface Mechanics GmbH Radeberg, Anfatec Instruments AG Oelsnitz, IMA Materialforschung und Anwendungstechnik GmbH
Project duration: 01.08.2005 – 30.09.2007
Project goal: Development of systems of springs and tips made by the silicon microtechnologies

SAB project „Verfahren und Einrichtung zum flächigen Laserabtragen auf der Basis stressfrei beschichteter 2D-Mikrospiegel"
Project manager: Prof. T. Gessner
Partners: IOM Leipzig,
ITW, Chemnitz,
IMM Holding GmbH,
Acsys Lasertechnik GmbH
Project duration: 01.11.2005 - 30.09.2007
Project goal:Development of nearly stress free silicon micro mirrors for medical applications

SAB project PRIMER
Project coordinator: AMD Fab36 LLC & Co. KG
Project manager: FhG-IZM: Dr. Stefan E. Schulz, TU Chemnitz / ZfM: Prof. Thomas Gessner
Subcontractors: Fraunhofer IISB, Fraunhofer IZM Chemnitz, TU Chemnitz
Project duration: 01.01.2007 – 31.12.2008

Industrial research cooperation
“Development of micromachined gyroscopes”
Project manager: Prof. T. Gessner
Partner: Gyrooptics company limited, St. Petersburg, Russia
Project duration: since 01.01.2006
Project goal: Development of technology and fabrication of prototypes of high precision angular rate sensors

Industrial research contract
“Fabrication of tunable Fabry-Perot filters”
Project manager: Prof. T. Gessner
Partner: InfraTec GmbH Dresden
Project duration: since 01.05.2006
Project goal: Fabrication of prototypes for a micromachined Fabry-Perot-Interferometer

Industrial research contract “Development of multi-use acceleration sensors”
Project manager: Prof. T. Gessner
Partners: Fara New Technologies, Xi´an, China, Memsfab GmbH, Chemnitz
Project duration: 01.09.2006 – 31.08.2008
Project goal: Support for development of a high precision acceleration sensor

Industrial research contract
„Charakterisierung der dielektrischen Isolation eines Hochvoltprozesses“
Project manager: Prof. Dr.-Ing. habil. J. Horstmann
Partner: X-FAB Semiconductor Foundries AG, Erfurt, Germany
Projekt duration: 01.09.2005 – 30.11.2007
Project goal: Research of trench isolation

Industrial education cooperation
„A/MS-Designprojekt”
Project manager: Prof. Dr.-Ing. habil. J. Horstmann
Partner: alpha microelectronics GmbH, Frankfurt(Oder), Germany
Project duration: since 01.01.2007
Project goal: Design and fabrication of analog and mixed-signal integrated circuits

Industrial research cooperation
„Elektrostatischer Bewegungssensor”
Project manager: Prof. Dr.-Ing. habil. J. Horstmann
Partner: Neumann Elektrotechnik GmbH, Chemnitz, Germany
Project duration: since 01.03.2007
Project goal: Optimization of a movement detection system based on electrostatic spatial sensors

Industrial research cooperation
„Industrielle Steuerelektronik”
Project manager: Prof. Dr.-Ing. habil. J. Horstmann
Partner: TEKA Absaug- und Entsorgungstechnologie GmbH, Velen, Germany
Project duration: since 01.08.2007
Project goal: Analysis and optimization of industrial electronics.

Industrial research cooperation
„Modellierung von MOS-Transitoren im Subthreshold-Bereich“
Project manager: Prof. Dr.-Ing. habil. J. Horstmann
Partner: X-FAB Semiconductor Foundries AG, Erfurt, Germany
Projekt duration: since 01.08.2007
Project goal: Characterization and modelling of MOS-transistors in the subthreshold region

Industrial research cooperation
„A/MS-Entwurf für MEMS-Sensoren“
Project manager: Prof. Dr.-Ing. habil. J.Horstmann
Partner: X-FAB Semiconductor Foundries AG, Erfurt, Germany
Projekt duration: since 01.11.2007
Project goal: Design of analog/mixed-signal integrated frontend circuits for MEMS pressure sensors.

Industrial research cooperation
“Design and Evaluation of MEMS“
Project coordinator: Prof. Mehner
Partners: Bosch GmbH
Project duration: 01.01.2007 – 31.12.2007
Project goal: Development of methodologies and tools for design of MEMS.

Project „ASIC-Baustein“
Project manager: Prof. U. Heinkel
Partner: Bosch GmbH, Center for Microtechnologies
Project duration: 01.10.2006 – 28.02.2007
Project goal: hip analysis

Robo tool „Entwicklung einer funkbasierten Kontroll- und Steuereinheit von Robotern zur Fernwartung“
Project manager: Prof. U. Heinkel
Partner: Agilion GmbH, Chemnitz
Project duration: 01.06.2006 – 30.04.2008
Project goal: Development and evaluation of mobile and stationary RF-communication modules

Industrial project “Feasibility study for the calculation of wetting properties in sub 100 nm high-aspect ration structures” – (PRIMER)
Coordinators: Prof. Dr. rer. nat. C. Radehaus
Partners: AMD Fab36 LLC & Co., Dresden
Project duration:01.01.2007 – 31.12.2007
Project goal: The ongoing downscaling of semiconductor processes to sub-100nm structures leads also to new challenges for the involved cleaning procedures. The aim of this study was to seek out opportunities of ab initio calculations to be helpful for the guidance of such cleaning procedures. Besides a literature overview available calculation packages were checked out and some preliminary calculations with the focus on interaction of etching chemicals with semiconductor surfaces have been done.

Industrial project “Atomic scale modeling of stacked gate dielectric for 32 nm CMOS Technology” – (AMIGAS)
Coordinators: Prof. Dr. rer. nat. C. Radehaus
Partners: GWT – TUC GmbH, Dresden
Project duration:01.06.2007 – 31.03.2008
Project goal: This project is a successor of the SUGAMOND project. The main goal is to use the knowledge and experiences gained in SUGAMOND to the modeling of new generation of gate dielectrics. The focus will be on the multi layer stack gate structures including high-K dielectric materials.

Industrial project “ab initio calculation of defect energies at equilibrium defect concentration in GaAs”
Coordinators: Prof. Dr. rer. nat. C. Radehaus
Partners: GWT – TUC GmbH, Dresden
Project duration:01.03.2007 – 30.06.2007
Project goal: Our work with Freiberg Compound Materials Company served two purposes: in addition to provide a consistent physical picture of the structure and energetic of a variety of point defects in GaAs, our calculations have been also used to asses the validity of the impurities in this material. Thus we used first principle methods (CPMD code) to investigate single vacancies and antisites in GaAs, taking into account the full relaxation of atoms, as well as electron and atomic chemical potential contributions to the total energy. Our calculations further extended to the existence of defect impurities like Boron and Silicon in GaAs. We have found industrial interesting results of Silicon impurities and Boron-impurities, as well as complex defects of these impurities in GaAs.

Highly reflective MEMS micro mirror

Dual axes scanner for material treatment and medical applications

Dipl.-Ing. Jens Bonitz; Dr.-Ing. Christian Kaufmann
Faculty of Electrical Engineering and Information Technology,
Chemnitz University of Technology, Chemnitz, Germany

1 Motivation

MEMS micro mirrors have a wide range of applications. They are commonly used for projection displays, spectroscopy, in microscopes or in endoscopes. For medical applications and laser material treatment special requirements must be fulfilled. For the medical field, an accurate beam steering is necessary, which requires a very high flatness of the micro mirror. For material treatment, a higher laser power is needed, which results in an increased heat introduction. The resulting high temperature can distort the reflective surfaces, reduce the optical efficiency, ablate surfaces und melt supporting flexures and can generate changes in layer stress, which can lead to warping of the mirror.

To overcome these problems, a micro mirror with following properties was developed:

- special design to minimize the warping
- highly-reflective coating to minimize the heat introduction
- special deposition process of the coating to minimize the layer stress

The micro mirror was developed in the context of a funded project by the Sächsische Aufbaubank GmbH. The project partner was the Leibniz-Institute for Surface Modification in Leipzig (IOM), Acsys Laser Technology GmbH in Mittweida, the IMM Group in Mittweida and the Institute for Innovative Technologies (ITW e. V.) in Chemnitz.

2 Mirror Design

The mirror is an electrostatically driven dual axes scanner, fabricated by silicon bulk technology with wet and dry etching steps. The design features are a round, relatively thick mirror plate (75/100 µm) and special torsion beams. The beams run 270° around the mirror plate and have the same height as the mirror plate at a small width of about 10 µm, Fig. 1.

This high aspect ratio leads to robust beams which allow only rotation whereas bending is scarcely possible. Because of these properties nearly no warping occurs and a very high flatness can be obtained.

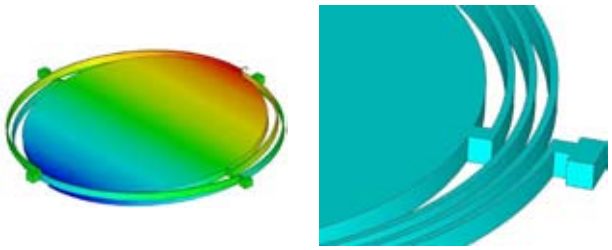


Fig.1: Simulated oscillation of the mirror and detailed view of the torsion beams

3 Mirror Reflectivity

The mirror is available with Au reflection coating. This coating offers a high reflectivity of approximately 96 % for the wavelength sector from 900 nm to 2250 nm, Fig. 2.

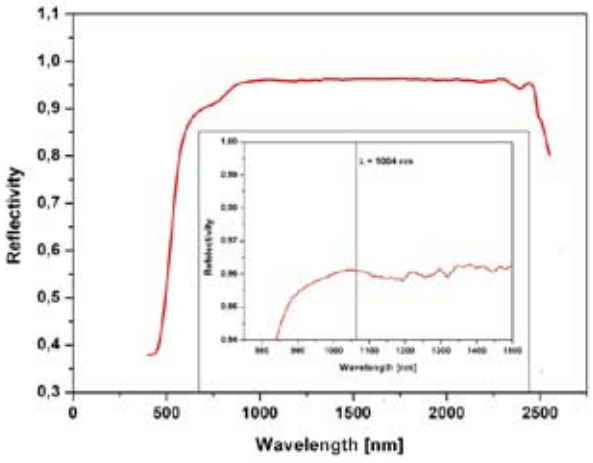


Fig.2: Reflectivity for Au coated mirrors

A higher reflectivity is achieved by a highly-reflective coating which is a combination of a metal layer and a dielectric multilayer stack (Bragg mirror), consisting of SiO_2 and TiO_2 layers, Fig. 3 and 4. The total layer thickness is less than 2 µm.

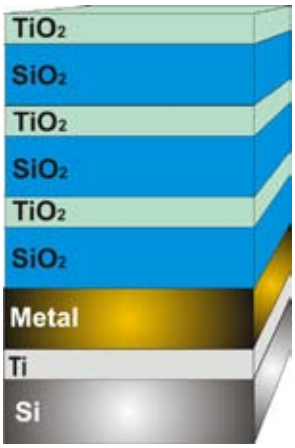


Fig.3: Assembly of the dielectric multilayer stack

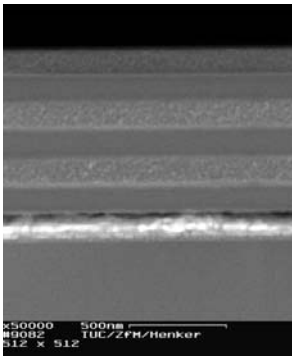


Fig.4: SEM image of a deposited layer stack

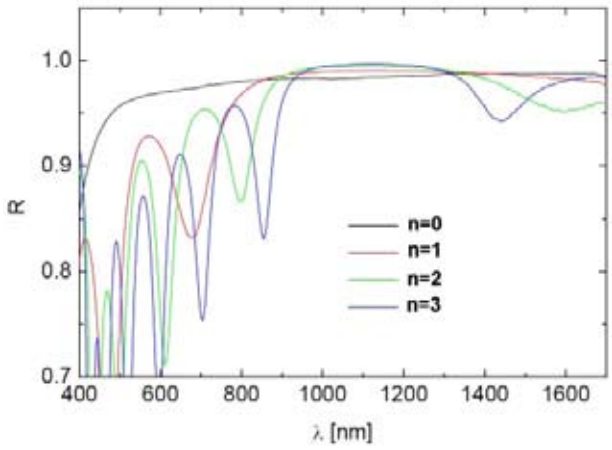


Fig.5: Reflectivity for mirrors coated with Bragg reflector (source: IOM)

This coating offers a high reflectivity of approximately 99.2 % for the wavelength sector from 950 nm to 1200 nm. Figure 5 shows the mirror reflectivity depending on the number of layer stacks (n in the figure).

The stress of the dielectric multilayer stack is minimized by a special deposition process with two ion beams. The first ion beam sputters the target atoms, which condense on the substrate. The second ion beam is directed onto the substrate and introduces an additional non-thermal energy contribution to the growing layer. By that, the stress of the dielectric layers can be reduced considerably.

4 Scanner system

The scanner system, Fig. 6, realizes a 2-dimensional material removal from a surface. Therefore, Lissajous patterns, Fig. 7, written by the scanner, are suitable for this approach.

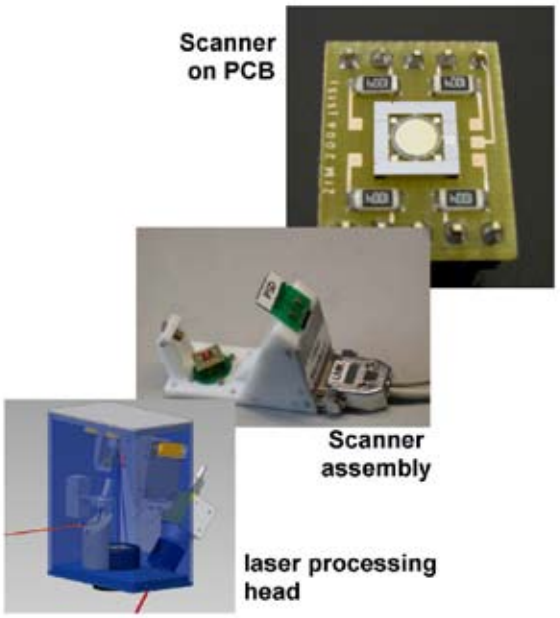


Fig.6: Scanner system

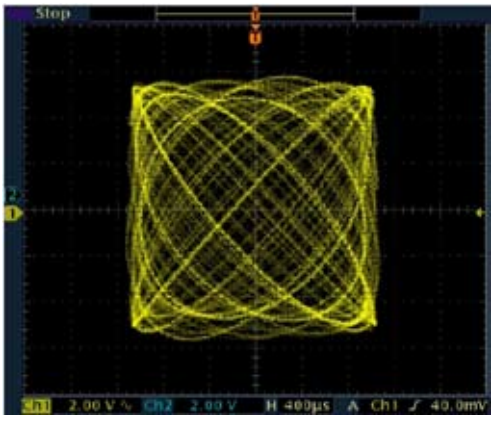


Fig.7: Lissajous pattern generated by the scanner

5 General Scanner Features

- Dual axes scanner
- Suitable for static analogous beam steering and resonance operation
- Au reflector and Bragg reflector
- Evaluation module (scanner and driving circuit) available
- Electric connection by wire bonding

6 Applications

- Barcode reading
- Optical screening
- Medical applications
- Material treatment

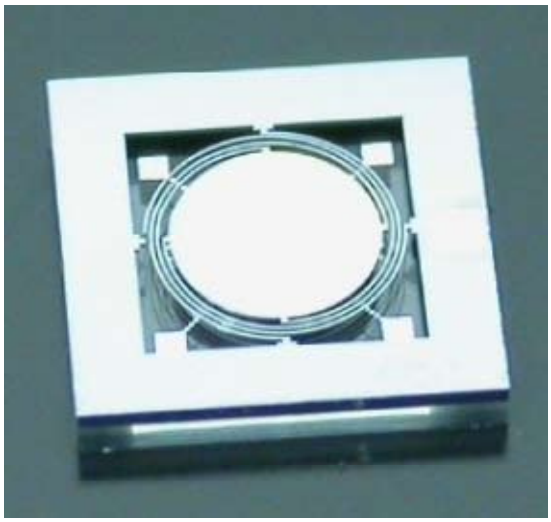


Fig.8: Micro mirror chip

7 Overview of properties

parameter \ type	1	2	Unit
Mirror diameter	3	2-Feb	mm
Resonant frequency	950	850	Hz
Scan angle at resonant frequency	12	20	Degree
Surface flatness with Au reflection coating	50	30	nm
Surface roughness R_a	< 10		nm
Surface coating	Au / Bragg-reflector		
Reflectivity @ 1064 nm	96 / 99.2		%
Laser flux density (Au, pulsed wave)	< 2,5	< 0,4	W/mm²
Operation Voltage V_o	400		V
Chip size	6,25 x 6,25		mm²

8 Contact

Dipl.-Ing. Jens Bonitz
Tel.: +49 (0)371 531 33608
Fax: +49 (0)371 531 833608
jens.bonitz@zfm.tu-chemnitz.de

Dr. Ing. Christian Kaufmann
Tel.: +49 (0)371 531 35096
Fax: +49 (0)371 531 835096
christian.kaufmann@zfm.tu-chemnitz.de

Specimen and comb drive actuators for a novel micro tensile test

Karla Hiller[1], Thomas Gessner[1], Hendrik Specht[2], Jan Mehner[2], Sai Gao[3], Konrad Herrmann[3], Matthias Küchler[1]

[1]Center for Microtechnologies, Faculty of Electrical Engineering and Information Technology, Chemnitz University of Technology, Chemnitz, Germany

[2]Chair Microsystems and Precision Engineering, Chemnitz University of Technology, Chemnitz, Germany

[3]Physikalisch-Technische Bundesanstalt, Braunschweig, Germany

1 Introduction

With shrinking dimensions of functional layers and elements in micro and nano technologies, it is essential to develop the adequate material test methods. For instance, the tensile stress of thin metal layers, fabricated by means of thin film deposition processes like PVD and CVD, will differ from bulk material parameters, and cannot be measured with the conventional standardized methods due to their nano and micro dimensions.

Therefore, the Physikalisch-Technische Bundesanstalt is developing novel test methods, whereby both the specimen and the elements necessary for the test are fabricated with micro technologies. Thus, the specimen can be fabricated with micro and nano dimensions similar to the application, and all elements can be integrated in one process flow and on one (Si) substrate. With this new approach, the influence of deposition method and process parameters on material characteristics of the metal layers can be studied and optimized.

2 Concept of the micro tensile test

The concept of such a micro tensile test is shown in figure 1. The specimen to be tested (thin metal layer, e.g. Aluminium) is fixed on the Si substrate on one side and connected to a gripper (free standing or supported by a spring) on the other side. The gripper can be moved by means of an electrostatic comb drive. Thus, a tensile force is applied on the gripper and further to the specimen, which will strain the thin layer and finally tear it. The strain can be measured e.g. by optical means or with an SPM (markers on top of the specimen) and can be correlated to the pulling force of the actuator. Both the gripper and comb drive actuator are fabricated by dry etching of Silicon.

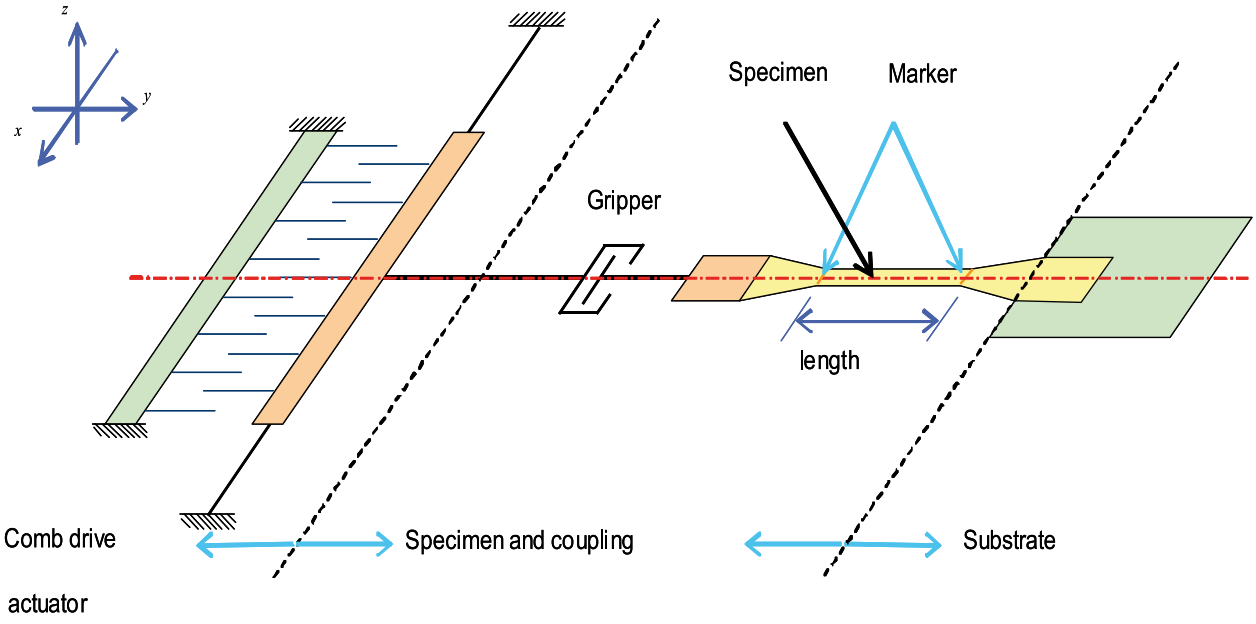


Fig.1: Illustration of the test concept

Although an integrated solution of comb drive with gripper and specimen with T-shaped handle is finally desirable, it was decided in a very first approach to fabricate and test them separately. As technology base, the well established BDRIE (bonding and Deep RIE) technology (see [1]) has been chosen. For the fabrication of specimen, additional metallisation steps and lateral underetch steps have been included. The structure height of the comb drive actuators is 50 µm and 30 µm for the T-shaped handle of the specimen. The small trenches of 3 µm in the actuator combs allow high actuation forces.

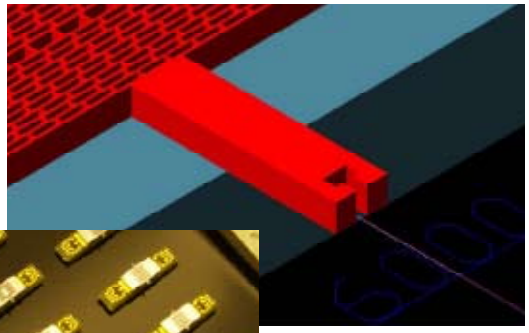


Fig.2: Detail of gripper fixed to the movable part of comb drive

Fig.3: Comb drive actuators with out standing tips and grippers mounted on PCB

A big challenge of this two-part approach is to separate the wafers in order to get actuators with grippers overhanging the substrate, see Fig. 2 and 3. This is done by a combination of dicing and breaking.

3 Comb drive actuators with grippers

The PTB has provided 4 different designs for the comb actuators with different shapes of the gripper. One of them is shown in figure 2. The gripper is designed to stand out about 600 µm with regard to the chip frame. Figure 3 shows a photograph of actuator chips mounted on PCBs.

4 Specimen with T-shaped handle

Two different designs in combination with varying length and thickness of Al specimen have been designed and fabricated. Design A offers a free-standing handle, Fig. 4, whereas in design B the handle is suspended by a spring, Fig. 5. The stiffness of the spring has been chosen so that it is smaller than the expected stiffness of the specimen. The width of the specimen is 3 µm, the length varies between 30 µm and 180 µm and the thickness has been chosen to 100 nm, 200 nm and 500 nm.

For both design A and B, all 15 variants were fabricated successfully. However, the free-standing specimen with 100 nm and 200 nm thickness bend down about 5 µm to the underlying substrate and probably stick there. This can be seen in figure 4. Therefore it is recommended to work with the spring suspension variant for further investigations. Furthermore, the problem of separation of the highly sensitive specimen must be solved.

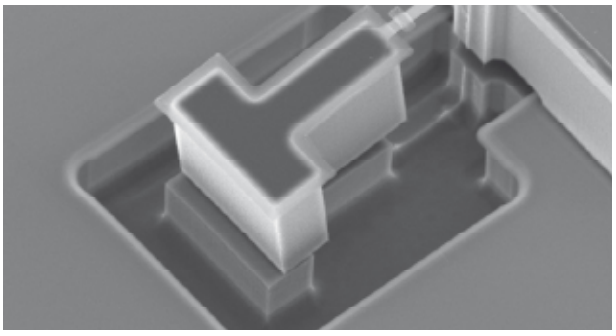


Fig.4: Free-standing specimen (shortest length) with T-shaped handle (design A)

On the other hand, the integrated version can now be fabricated, which would avoid the problems of separation and mounting.

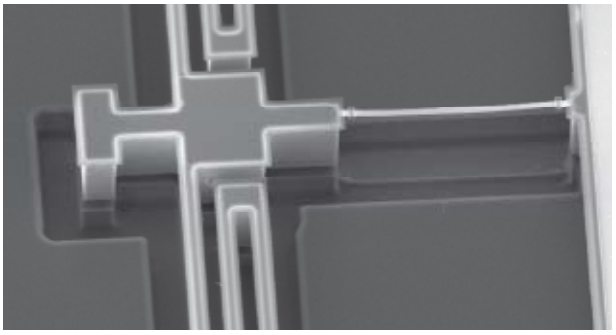


Fig.5: Specimen (larger length) with folded spring suspension (design B)

5 References

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Fabrication of a Low-Frequency Ultrasonic Transducer

Chenping Jia[1], Maik Wiemer[2], Karla Hiller[1], Thomas Otto[2], Thomas Gessner[1,2]

[1]Centre for Microtechnologies, Chemnitz University of Technology, Chemnitz, Germany

[2]Fraunhofer IZM Chemnitz Branch, Chemnitz, Germany

1 Introduction

Ultrasonic transducer is a special kind of acoustic sensor. It can be used to detect and emit ultrasound. Most current ultrasonic transducers are made from piezoelectric ceramics, which can couple sound wave efficiently into solid materials, and detect cracks in them. However, because the impedance mismatch between ceramic and fluid is large, ceramic transducers become less effective in airborne and immersion applications. In order to improve the energy conversion efficiency in these situations, many efforts have been made [1, 2], but these improvements are mainly airborne-oriented. In this paper, we will investigate the feasibility of capacitive transducer for immersion applications.

2 Experiment Investigation

Figure 1 shows the fabrication steps of the proposed transducer. It consists of a membrane carrier and a back plate. Preparation of the membrane carrier starts from double side polished Si wafer. First, 500nm thermal oxide and 300nm LP-SiN are grown on the wafer surface. After that, 600nm Al is deposited and subsequently patterned. Before Al deposition, some via are opened in the oxide/nitride composite layer, so that electrical connection can be realized in the future. In following steps, 2µm PE-SiO2 is deposited on the Al electrodes. This layer acts as passive layer, and it is then patterned to provide access windows for bottom electrode.

Fabrication of the back plate is relative simple. Altogether only 3 masks are used. First, 500nm thermal oxide is grown on (111)-type silicon wafer and sequentially patterned to act as etch mask. The wafer is then dipped in KOH solution to remove a thin silicon layer. Because surfaces exposed by KOH etching is very rough, these recesses have an inherent anti-stiction ability. The depth of the recesses is determined by etching time, and can be varied between 2 to 7 µm. After KOH etching, the mask oxide is stripped off and a new oxide layer is grown on the wafer. In following step, 600 nm Al and 2 µm PE-oxide are sequentially deposited and patterned to form bottom electrodes. Finally, access windows are opened in the PE-oxide layer to expose contact pads.

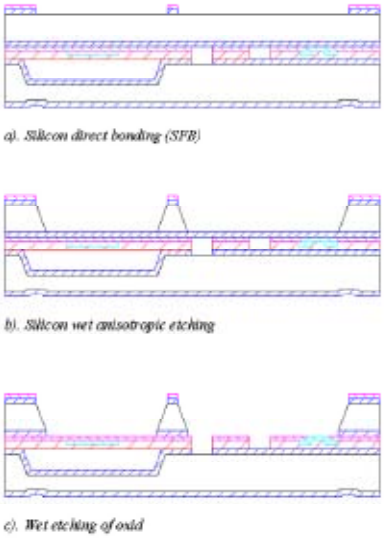

Fig.1: Fabrication process

When both components are ready, they are assembled together through direct bonding. Since direct bonding requires smooth surface finish, before bonding, a polish step may be necessary to eliminate protrusions and improve surface smoothness. After that, the wafer stack is dipped in KOH solution to remove bulk silicon above the composite membrane. Finally, an oxide etching process is carried out to remove the protective oxide above the Al pads, so that electric connection can be established.

3 Initial Characterisation

Figure 2 shows a microscopic photo of the proposed ultrasonic transducer. It has 7 identical cells. To facilitate future packaging process, contact pads are arranged in a seperate region beside the active cells. In Figure 2, one

can also see an extra pad for ground electrode. Together with the bottom electrode, this pad provides a simple method for the formation of a matched capacitor.

Fig. 3 shows the static deformation of the membrane under the load of normal air pressure. Through

Fig.2: Silicon micro-machined ultrasonic transducer

the interference rings, one can infer that the surface of the membrane is not flat. Further calculation indicates that the maximal deformation of the membrane at the center is more than 500nm, This means that her-

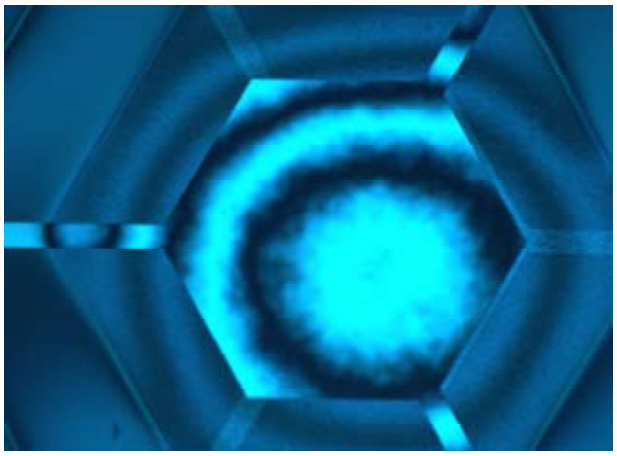

Fig.3: Membrane static deformation

metic sealing has been realized during bonding, and the inner side of the membane is under vaccum condition. Note that due to bonding mis-alignment, the top and the bottom electrodes do not coincide fully with each other.

The dynamic property of the transducer is measured with a laser Doppler vibrometer. According to this measurement, the resonant frequency of the transducer is 570kHz, and the maximal vibrating amplitude at resonance is 1nm, with 10Vpp stimulus and 5Vdc bias. By changing the dimension, thickness, as well as the material composition of the membane, it is possible to extend the resonant frequency to 100kHz range. Similiarly, if large vibration amplitude is required, one can use larger stimulus signals.

4 Summary

In this paper, an improved process for the fabrication of capacitive ultrasonic transducer is proposed. Benefited from the separate preparation steps, low

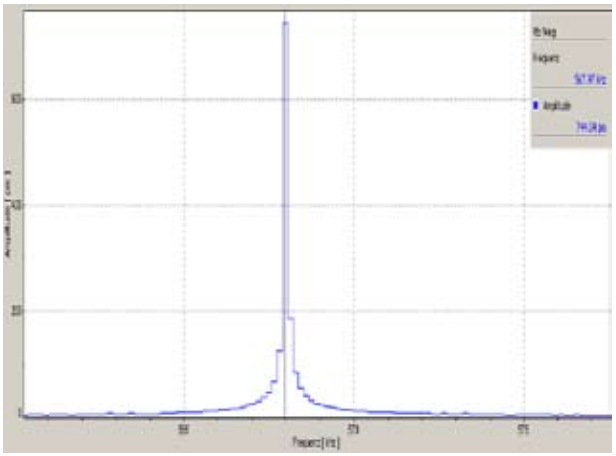

Fig.4: Amplitude-Frequency response

frequency transducers of 100 to 500 kHz can be produced without resorts to sacrifice etching. Two major aims were realized in this investigation. First, both top and bottom electrodes are arranged on the same side of the device. Therefore, no vertical via is required to address the bottom electrode. By employment of metal electrodes, instead of bulk substrate electrode, contact resistance and parasitic capacitance are greatly reduced. Besides, single side layout also facilitates future packaging and integration with electronics. Second, a self-stop etching scheme was proposed and successfully implemented. With this method, regular recesses of 2 to 7 microns depth can be produced on the surface of a standard (111) Si wafer. Moreover, since the bottom surface of these recesses is rough and uneven, it has inherent anti-stiction ability. For capacitive transducer that requires small and controllable

electrode gap, this method is especially valuable. In comparison with conventional surface processes for capacitive transducer, this method is simple, reliable and tolerable to process-parameter variances. It can be a potential method for the fabrication of underwater ultrasonic transducers.

5 Acknowledgement

The authors would like to express their appreciations to Mr. J. Grunert and S. Uhlig for their dedications in this work, and Mrs. M. Henker and I. Hoebelt for sample inspection. The supports of the colleagues in the Center for Microtechnologies (ZfM) at TU Chemnitz are also acknowledged.

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MICROFLUIDIC LOW-COST PUMPS BASED ON ELECTROLYSIS WITHIN HYDROGELS

Joerg Nestler[1], Karla Hiller[1], Thomas Otto[2], Thomas Gessner[1,2]

[1] Center for Microtechnologies, Chemnitz University of Technology, Chemnitz, Germany

[2] Fraunhofer IZM Chemnitz Branch, Dept. Multi Device Integration, Chemnitz, Germany

1 Introduction

A fully-integrated injection-moulded thermoplastic microfluidic system complete with active pumps, sealing and controlled surface modification suitable for protein applications has been developed within the European research project SEMOFS. Microfluidic flow control in this system is realized by low-cost, low temperature, one-shot micropumps based on electrochemical gas generation by electrolysis inside a hydrogel. As almost no heat is generated by this actuation principle, it is well suited for protein-sensing applications.

2 Electrolysis and Hydrogels

The electrolysis of water is the dissociation of water molecules into oxygen and hydrogen gas by means of an electric voltage. The (net) reaction is given by:

Anode: $2H_2O \rightarrow 4H^+ + 4e^- + O_2$ (gas)
Cathode: $2H_2O + 2e^- \rightarrow 2OH^- + H_2$ (gas)

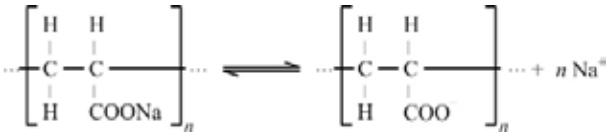
The amount of generated gas molecules is directly proportional to the current flowing through the electrolytic cell. The generated gas can be either used to deflect a membrane or to drive a fluid by directly applying the gas pressure to a fluid plug without an intermediate membrane.

Bubble actuators based on electrolysis have already been successfully demonstrated for microfluidics. All these works have in common that a liquid (usually water or a water based liquid) has been used as electrolyte. Thus, an "actuation liquid" has to be integrated into the system. However, the integration of a liquid can be a critical factor for mass production and may also cause problems concerning long-term stability.

Therefore, in this work a (water-containing) hydrogel is used as electrolyte instead of a liquid. By the usage of stencil printing, such a gel proved to be easy to integrate and thus highly suitable for mass fabrication.

Non-toxic and available at very low cost, a hydrogel based on poly (acrylic acid) sodium salt (PAAS) was used.

Crosslinked PAAS is a so-called super absorbing polymer which is able to dramatically swell in water. The swollen state is referred to as a hydrogel, which mainly consists of up to 99 wt% of water, but has a very high viscosity. When PAAS is brought in contact with water, the weakly bonded sodium is split off, leaving negatively charged polymer chains and movable sodium ions:



3 Integration of active and passive microfluidics

The whole microfluidic system consists of a passive microfluidic substrate and an electrode substrate as the actuator part.

As shown in Fig.1, the PAAS gel is placed directly on electrodes on the electrode substrate. Applying a voltage over the electrodes leads to a gas generation due to electrolysis. The generated gas can then directly be

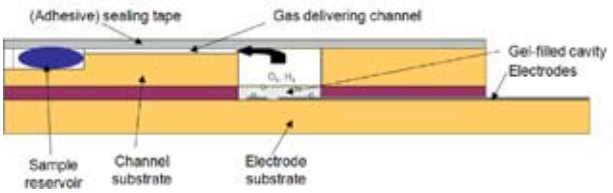


Fig.1: Principle of the used electrolysis-gel pump. The gas generated by electrolysis is used to directly drive the fluid through the channel system

used to drive liquids through the channel system in a fluidic substrate.

In the passive microfluidic substrate, Fig. 2, each inlet reservoir is connected to the pump region by a thin hydrophobic channel ("gas delivering channel") of a cross

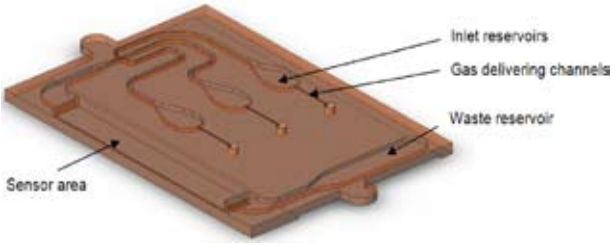


Fig.2: Passive microfluidic substrate

section of 100x100 µm², Fig. 2 & 3. The pump region mainly consists of the gel reservoirs on top of the electrode substrate.

After joining active and passive microfluidic parts, the inlet reservoirs can be filled by a syringe or a dispenser.

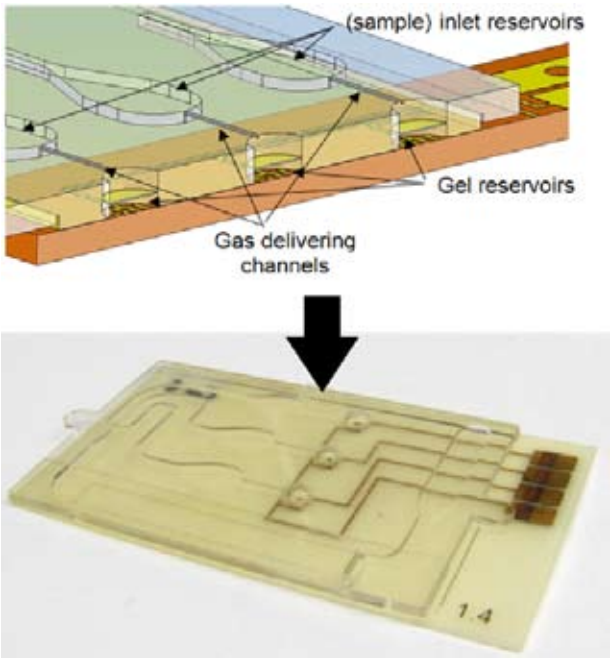


Fig.3: Assembly of active and passive micro-fluidics (top: principle, bottom: assembled device)

4 Results

The pumps prepared as described above allow a backpressure of more than 1 bar, flow rates in a typical range between 1 and 40 µl/min, and are able to deliver volumes of several 100µl. In Table 1 the characteristics of the low-cost pumps are summarized.

Parameter	Value	Unit
Flow Rate:	5 - 100 (typ. 1 - 40)	µl/min
Max. Backpressure:	1..2	bar
Operating Current	0.5 - 10 (typ. 4)	mA
Operating Voltage:	< 15 (typ. 5)	V
Actuator Size (typ.):	(3x3x0.2)	mm^3
Operating Time (per pump)	<10	min

Table1: Performance of the integrated micropumps

Fig. 4 shows the emptying sequence of the middle of the three reservoirs.

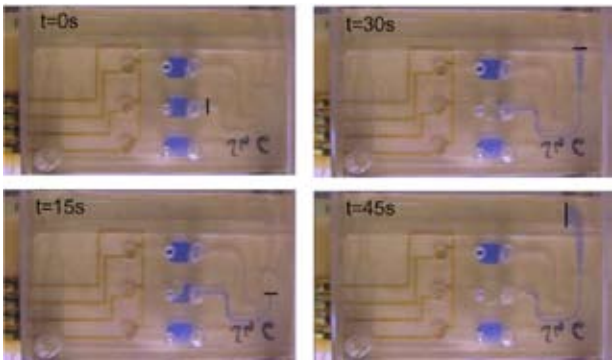


Fig.4: Emptying sequence of a reservoir by an electrolysis-gel pump. The small line in each picture marks the front of the colored liquid plug inside the channel.

5 Acknowledgements

This work has been founded by the European Commission under contract number IST-FP6-016768 and is part of the European research project SEMOFS (Surface Enhanced Micro Optical Fluidic Systems, www.semofs.com).

Adjustable Force Coupled Sensor-Actuator System for Low Frequency Resonant Vibration Detection

Roman Forke[1]; Dirk Scheibner[2]; Thomas Gessner[3]; Wolfram Dötzel[1]; Jan Mehner[1]

[1]Department of Microsystems and Precision Engineering, Chemnitz University of Technology, Chemnitz, Germany,
[2]Siemens Automation and Drives, Advanced Technologies and Standards, Nuremburg, Germany
[3]Center for Microtechnologies, Chemnitz University of Technology, Chemnitz, Germany

1 Introduction

Detection of mechanical vibration is an important means for condition monitoring at industrial machinery for instance at gears, bearings, drives, engines and other highly stressed machine components [1]. Changes e.g. in amplitude, frequency or both are indices of increasing wear. By observing these changes, maintenance can be scheduled and consequences of the machine failure are avoided.

Commonly, precision engineered wideband transducers or wideband MEMS sensor elements are used for vibration detection. Together with signal analyzing electronics the spectral data of the time series is acquired. But, the high costs of these systems make permanent monitoring only reasonable for expensive equipment or in safety related applications.

In most instances it is sufficient to observe only a few spectral lines for extracting the relevant information. Combining the frequency selectivity and the expected low manufacturing costs, micromechanical resonant vibration sensors are powerful means for this type of application [2]. The main drawback of the resonant sensors is that monitoring of the low frequencies requires either an extremely large chip area or a weak suspension to reduce the stiffness to mass ratio for applications well below 1 kHz.

The new approach makes use of the superheterodyne principle to transform the information of low frequency into an acceptable frequency range for resonant detection, Fig. 1. The interaction of a wideband oscillator and a resonator makes it possible to detect low frequency vibration with a resonant principle. Simultaneously, it allows simple tuning of the detection frequency.

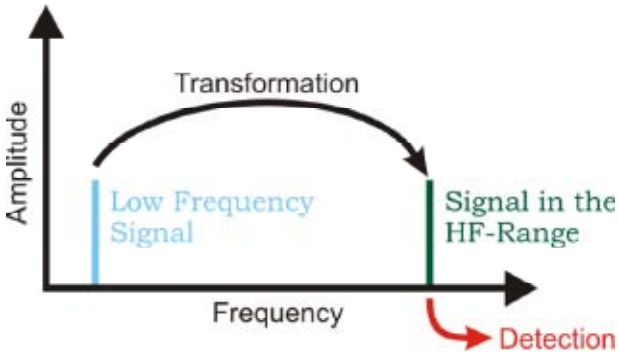


Fig.1: Basic principle

2 Principle of Operation

The new sensor system consists of two separated micromechanical oscillators and is operated at standard pressure. Electrostatic forces are used to couple the two oscillators, see Fig. 2.

One of the oscillators is used as a wideband detector for mechanical vibration. It is passively damped with

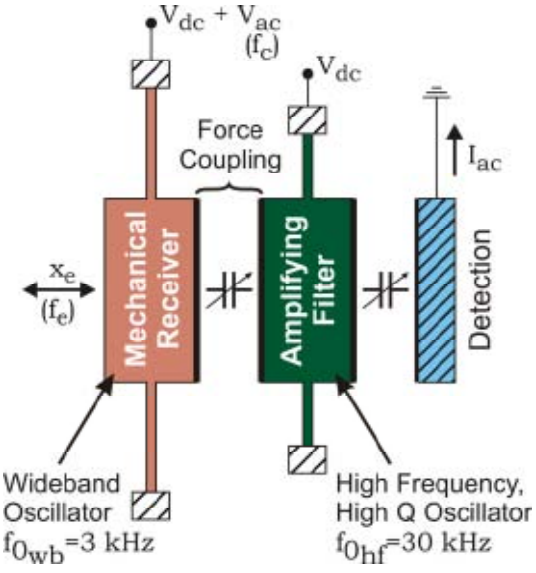


Fig.2: Basic structure of the force coupled oscillator system

fluidic damping structures. The second oscillator is a resonator with its eigenfrequency set to one decade above the latter. The principle can be summarized by the following three main steps [3]:

- The mechanical signal of low frequency (up to 1 kHz) is detected with a wideband, optimally damped oscillator.
- The motion of this oscillator is used to modulate the existing electrostatic force (carrier) between the two force coupled oscillators. Thus the low frequency information is transformed into a higher frequency range.
- The carrier can be adjusted so that the resonator is excited at its resonance frequency. This allows a frequency selective detection of low frequency mechanical vibration, Fig. 3.

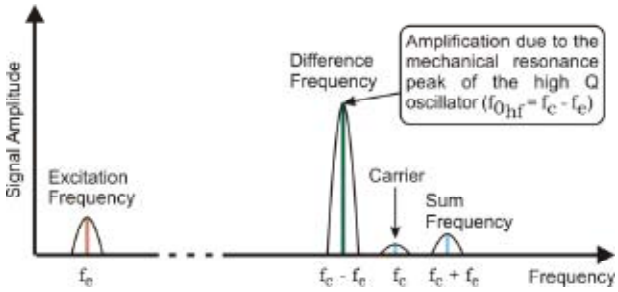


Fig.3: Principle of operation

3 Fabricated Silicon Structure

The micromechanical system is fabricated with the BDRIE (Bonding and Deep Reactive Ion Etching) silicon technology which allows aspect ratios of more than 25:1 and thus belongs to the HAR (High Aspect Ratio) technologies [4]. The single crystalline active wafer contains the mechanical elements as well as the drive and detection electrodes for lateral movement. Thick thermal oxide layers are used for vertical insulation. The lateral insulation is achieved by air gaps.

Fig. 4 shows a scanning electron microscopy (SEM) image of the fabricated silicon structure.

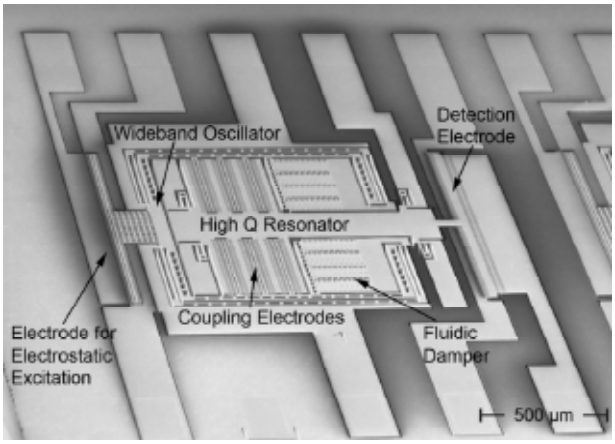


Fig.4: SEM view of the force coupled oscillator system

4 Results

To be free of any distracting mechanical coupling, the sensor system is tested using electrostatic excitation of the wideband oscillator. Fig. 5 shows the graph of a measurement taken with electrostatic excitation at 400 Hz and capacitive pick-off. For the high Q resonator, the measured eigenfrequency is f0=29.87 kHz. By setting the carrier frequency to fc=30.27 kHz the 400 Hz excitation can be monitored.

The graph in Fig. 6 shows the linear dependence of sensor excitation and voltage output. The drive electrode of the mechanical receiver drives this oscillator with different voltages from 0 to 10 Vpp and at a frequency of 400 Hz.

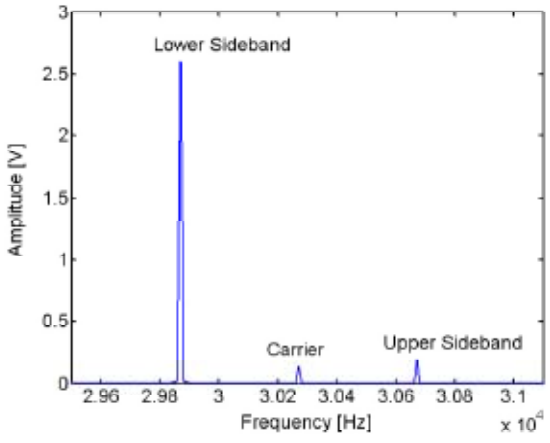


Fig.5: Frequency domain of the sensor output

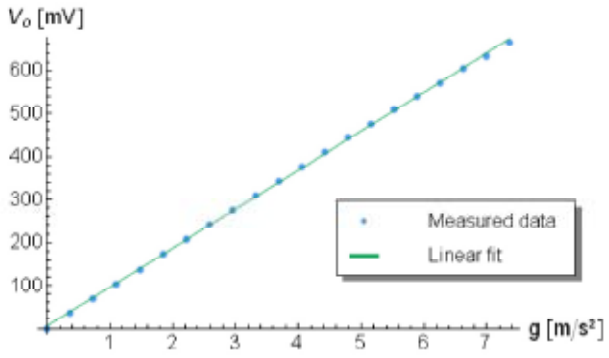


Fig.6: Voltage output vs. excitation

5 Conclusion

The presented micromachined force coupled oscillator system shows a novel operating principle to detect mechanical vibration of low frequency (< 1 kHz) without a subsequent Fourier transformation. The principle is based on amplitude modulation and selective filtering at one specific frequency as known from the superheterodyne principle. The sense frequency is acquired by simple frequency tuning.

The sensor system operates at standard pressure and does not need any vacuum packaging. Thus, the presented MEM system is a base for a low cost alternative for vibration detectors.

6 Acknowledgements

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A MEMS friction vacuum gauge

Dirk Tenholte[1]; Steffen Kurth[2]; Karla Hiller[1]; Christian Kaufmann[1]; Thomas Gessner[1,2]; Wolfram Dötzel[1]; Jan Mehner[1]

[1]Faculty of Electrical Engineering and Information Technology, Chemnitz University of Technology, Chemnitz, Germany

[2]Fraunhofer IZM, Dep. Multi Device Integration, Chemnitz, Germany

1 Introduction

Vacuum technology has become more and more important for industrial production during the last years, particularly for surface coating and refinement. These applications require measurement systems with short measurement time and a measurement range of more than five decades. To control the charging of the recipients, sensitivity of the sensors up to ambient pressure (10^3 mbar) is desired.

Actual development of vacuum gauges considers these requirements by minimizing conventional gauges like Pirani and Cathode Manometers [1-2]. Some of these new sensors are already commercially available.

Friction gauges are used in high and fine vacuum as reference and calibration sensors. They utilize the damping of an oscillator by energy emission to the surrounding gas as a measure oft the pressure. Suggestions for MEMS friction gauges are described by Kurth [3] and Bianco [4].

In this work we present a new MEMS friction vacuum gauge which expands the advantages of common friction gauges to a larger measurement range and a short measurement time. The sensor can be used for measurements in high temperature environments up to 350° C.

2 Assembly and working principle

The working principle of the sensor is based on the pressure dependent gas friction. The essential part of the sensor is a torsional oscillating plate with a nearby wall. The structure of the sensor is shown in Figure 1. It consists of a 25 µm thick, 3x3 mm² oscillating plate which is mounted in the centre of the chipframe by two 325 µm long torsional springs. The gap between oscillator and the electrodes on the carrier is 5 µm.

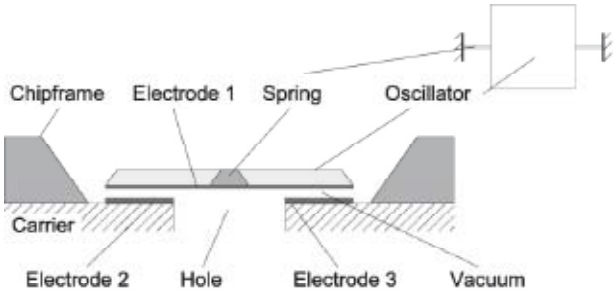

Fig.1: Cross sectional view of the sensor

For detecting the vacuum pressure, we utilise two different kinds of pressure depending damping: For low pressures, where the gas can not be considered as a continuum, the molecular damping is pressure dependent. For higher pressures, where the gas can be considered as a continuum, the squeeze damping is the pressure dependent one.

Below the oscillating plate is a hole in the carrier wafer for reducing the damping at higher pressures, so the plate will oscillate and not be overdamped at any pressure. At low pressures, the hole has no effect on the molecular damping.

Due to a driving voltage between the oscillator (Electrode 1) and one of the ground electrodes (Electrode 2, resp. Electrode 3), the oscillator plate tilts around its rotation axis.

3 Simulation of the sensor

The sensor can be considered as a system with one degree of freedom, because only the gyratory mode is of interest. The static and dynamic behaviour can be described by the differential equation

$$\ddot{y} + \frac{\hat{a}}{m}\dot{y} + \frac{k}{m}y = 0 \qquad (1)$$

The damping β consists of several components:

Above 1 mbar the gas around the oscillator can be treated as a continuum. In this pressure range, up to ambient pressure, the effective viscosity of the gas in

the narrow gap of 5 µm between oscillator and electrodes depends on the pressure. Due to the hole under the oscillator, only a narrow area at the two opposite ends of the oscillating plate parallel to the vibration axis, where oscillator and ground electrodes overlap, leads to the squeeze damping. Due to the small amplitude of oscillation, the motion of the plate towards the electrodes has to be regarded as translational. Methods for numerical analysis of the squeeze damping for two parallel, towards moving plates are presented by van Kampen [5].

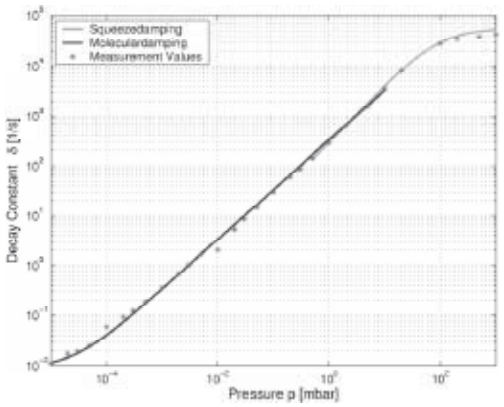

Fig.2: Simulated and measured decay constant depending on pressure

For pressures below 1 mbar, the mean free path of the gas molecules becomes much larger than the gap between oscillator and electrodes. In this pressure area the molecular damping occurs. We use the equations derived by Li [6] for calculating the molecular damping. They refer to a paddle formed structure, considered as a mathematical pendulum with lateral dimensions. The oscillator plate of our sensor can be approximated as two on their hinge concatenated paddles.

At the pressure range below 10^{-5} mbar, pressure independent kinds of damping like intrinsic and thermo compression damping reach the magnitude of the molecular damping and limit the lower measurement range.

On the basis of the developed simulation model the sensor geometry has been optimized, so that the measurement range is as wide as possible and the sensor is sensitive up to ambient pressure (10^3 mbar).

Simulated and measured decay constant of the optimized sensor is shown in Figure 2 depending on pressure. As one can see, simulation and measured values match very well. The sensor has a total measurement range over 8 decades from 10^{-5} mbar to 10^3 mbar.

4 Detection of the damping

There exist two different ways to detect the pressure dependent damping of the sensor.

4.1 Determining the Decay Constant

One option of determining the damping is to evaluate the damped oscillation. After switching off the driving voltage between oscillator and one of the ground electrodes, the damped oscillation

$$\phi(t) = \hat{\phi} e^{-\delta t} \cdot \cos(\omega_d t) \qquad (2)$$

is measured. The decay constant δ is determined by detecting the maxima of the oscillation and calculating their logarithm. These values result in a straight line which gradient is the decay constant:

$$\ln\phi(t) = \ln\hat{\phi} - \delta t \qquad (3)$$

To reduce the response time of the sensor, the measurement is stopped after 100 ms. If the oscillation amplitude is above a given value after calculating the decay constant, another measurement is started without exiting the oscillator again. At pressures below 10^{-3} mbar, the decay constant has to be calculated by averaging from several 1000 measured values to reduce the influence of noise. So a measurement time of several seconds result, which is not acceptable for an industrial operation.

4.2 Controlled sensor operation

Another way to detect the pressure dependent damping is the controlled operation of the sensor. The oscillation amplitude is adjusted to a constant value by controlling the amplitude of the sinusoidal driving voltage. The block diagram of the controlled sensor system is shown in Figure 3. If the driving voltage is connected to the oscillator and the ground electrodes, the damping and therefore the pressure is proportional to the squared driving voltage:

$$ä \sim p \sim U_e^2 \qquad (4)$$

So the variation of δ over 7 decades, as shown in Figure 2, results in a variation of the driving voltage over 3.5 decades in the Range of 1 mV to 10 V.

To get a pressure dependency of the driving voltage over the whole measurement range of the sensor, the oscillator has to be driven exact on its resonance frequency. The phase shift shown in Figure 3 corrects the phase error inducted by the measurement electron-

ics so that the oscillator is self-controlled and therefore oscillates on its resonance frequency.

As a measure of the pressure, the control variable U_R is used. Its overshooting in case of pressure variations at low pressures can not be avoided, but it can be filtered by a low pass 2nd order. In this case, the response and measurement time only depends on the low pass. It is possible to realize a response time of

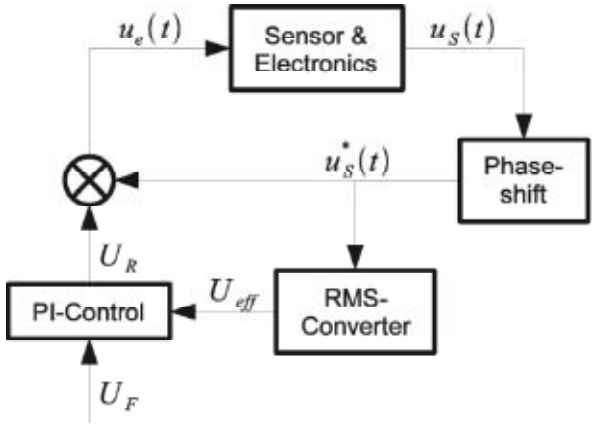

Fig.3: Block diagram of the controlled sensor system

10 ms and a measurement time of less than 150 ms for large pressure variations. For continuous and steady pressure variations the measurement time is conspicuously less.

5 Measurement results

The sensor has been installed inside a vacuum system and the damping of the oscillator as well as the control variable have been measured as a function of the ambient pressure.

The measurement results are shown in Figure 4. Based on the scaling of the graphs, one can see that the gradient of the decay constant is twice the one of the control variable. The measurement range of the sensor reaches pressures below 10^{-5} mbar.

The sensor consists only of glas, silicon and aluminium. These materials are temperature stable up to 400° C. Because the sensor electronics is connected to the sensor by an 1 m long cable, the sensor can be used for measurements at high temperatures. Investigations have shown that it is possible to use the sensor for pressure measurement at temperatures up to 350° C.

6 Conclusions

In this paper we have presented a new MEMS friction vacuum gauge. It has a measurement range of over 8 decades from 10^{-5} mbar up to ambient pressure (10^3 mbar). By using the controlled sensor operation, the response and measurement time can be lowered significantly

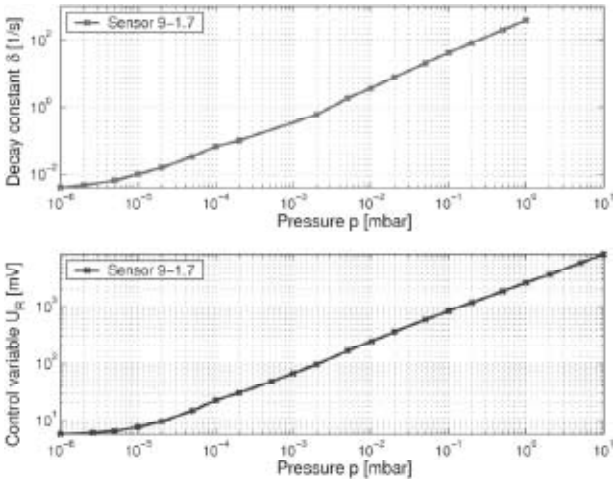

Fig.4: Comparison of pressure dependent decay constant and control variable

compared to the detection of damping by the damped oscillation. A response time of 10 ms and a measurement time of less than 150 ms can be realized.

The voltages used for sensor operation are ±12 V, so no electric or magnetic field is inducted to the ambient. The overall dimensions of the sensor are 8.5 mm x 9 mm x 1.5 mm; this complies with a volume of 115 mm³.

The sensor consists of silicon, glas and aluminium and can therefore be used for pressure measurement at high temperatures up to 350° C without any restrictions. Unlike Pirani sensors it has no thermal affect to its ambient, but adopts the ambient temperature.

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Electronic transport properties in copper nanowire

Saeideh Mohammadzadeh[1,*], Davoud Pouladsaz[2], Reinhard Streiter[1,3], Thomas Gessner[1,3]

[1]Center for Microtechnologies, Chemnitz University of Technology, Chemnitz, Germany

[2]Department of Physics, Chemnitz University of Technology, Chemnitz, Germany

[3] Fraunhofer IZM Chemnitz Branch, Chemnitz, Germany

1 Introduction

In recent years, a worldwide effort has been devoted to nanoelectronic devices transport properties both experimentally and theoretically [1] as the nanoscaled electronic systems represent ultimate the size limit of functional devices. Although copper is a commonly used interconnect metal, fewer efforts have been devoted on copper nanowires.

In this paper, the theoretical analysis has been performed on electronic transport properties of the copper and gold nanowires attached to the cognate (100) electrodes.

2 Method of calculation

In order to study the electron transport properties, the copper nanoscale wire sandwiched between crystalline electrodes in (100) direction, is considered. The schematic view of the system under study can be represented in the Fig. 1, is partitioned into three parts: two contacts, and the scattering region. The contacts are semi-infinite leads and it is assumed that their properties coincide with those of bulk system. The more realistic nanowire model is obtained by considering a part of the electrodes with several atomic layers in scattering region.

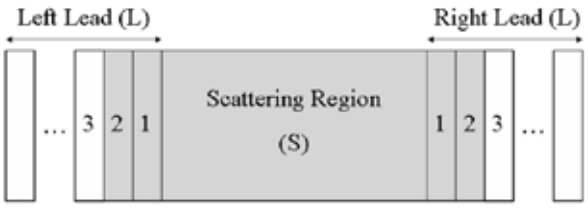

Fig.1: Schematic setup of the system. It is divided into three regions: the scattering region (S), and the left (L) and the right lead (R). The numbering of the leads refers to the atomic layers considered into scattering region

Calculations are performed using the non-equilibrium Green's function within the density functional tight binding method [2-5] and the Landauer-Büttiker theory [6,7] to obtain the differential conductance of the system. Interaction between the valence electrons is treated in the local density approximation (LDA) [8].

The tight binding Hamiltonian of the entire system takes the form:

$$H^0_{\mu\nu} = \begin{cases} \epsilon^{\text{free-atom}}_{\mu}, & \mu = \nu \\ < \phi_\mu \left| T + \nu_{\text{eff}}(n^0_i + n^0_j) \right| \phi_\nu >, & \mu \in i, \nu \in j \end{cases} \quad (1)$$

where ϕ_μ and ϕ_ν are the atomic orbitals localized around the atomic centers i and j; T is the kinetic energy operator, and ν_{eff} is the effective one-particle potential which depends on the density of the two atomic centers i and j.

In experiments, the transport properties are measured by applying finite bias voltages between the electrodes. Since the applied bias changes the transport properties from those at the zero-bias limit, it is important to consider the effect of the applied bias in the theoretical studies. This is provided by the NEGF method introduced by Keldysh [9] to deal with non equilibrium situation.

The density matrix needed for the density functional Hamiltonian can be described in terms of the NEGF:

$$\rho = \frac{1}{2\pi i}\int_{-\infty}^{+\infty} dE G^<(E) \quad (2)$$

the Keldysh Green's functions, $G^<(E)$ and $G^>(E)$, are defined in terms of the retarded, the advanced Green's functions and the non-equilibrium self energies $\Sigma^<$ and $\Sigma^>$.

$$G^{<,>} = G^r \sum^{<,>} G^a \quad (3)$$

Within this formalism the current can be written with an expression formally equivalent to that of scattering theory by treating the coupling between the scattering region and the leads at perturbation [10-12].

$$I(V) = \frac{2e}{h}\int_{\mu_1}^{\mu_2} \text{Tr}\left[\sum\nolimits_L^< G^> - \sum\nolimits_L^> G^<\right] dE \quad (4)$$

where $\Sigma_L^{<>}$ are the self energy functions for the left contact. The limits of the integration, μ_1 and μ_2, are the electrodes chemical potentials.

It is assumed that the voltage drops across the scattering region, this assumption results in the contact self-energies $\Sigma_{L(R)}^{<(>)}$ reducing to

$$\sum_{L(R)}^{<} = -2if_{L(R)}\,\mathrm{Im}(\sum_{L(R)}^{r})$$
$$\sum_{L(R)}^{>} = 2i(1-f_{L(R)})\,\mathrm{Im}(\sum_{L(R)}^{r}) \quad (5)$$

where $f_{L(R)}$ is the Fermi distribution function and $\mathrm{Im}(\sum_{L(R)}^{r})$ is the imaginary component of the retarded self–energy in the contact.

Based on the Landauer's scattering approach to electron transport, and assuming that transport is ballistic for finite bias voltages, the current can be established by noting that the transmission matrix t(ε) as

$$t(\varepsilon) = \left[\Gamma_R(\varepsilon)\right]^{1/2} G^r(\varepsilon)\left[\Gamma_L(\varepsilon)\right]^{1/2} \quad (6)$$

where the $\Gamma_{L(R)}(\varepsilon)$ is given by

$$\Gamma_{L(R)}(\varepsilon) = i(\sum_{L(R)}^{r}(\varepsilon) - \left[\sum_{L(R)}^{r}(\varepsilon)\right]^{\dagger}) \quad (7)$$

By substituting the transmission matrix into equation (4) the current is obtained as follows

$$I(V) = \frac{2e}{h}\int \mathrm{Tr}\left[\Gamma_R G^r \Gamma_L G^a\right](f_R(E) - f_L(E))dE \quad (8)$$

where $\mathrm{Tr}[\Gamma_R G^r \Gamma_L G^a]$ gives the transmission coefficients.

The differential conductance can be obtained from the current flowing through the system by taking the derivative of current with respect to V [13-15].

In the adiabatic approximation, the zero bias voltage conductance at zero temperature can be written as $G=G_0T$, where $G_0=2e^2/h$ is quantum conductance and the factor T represents the average probability that an electron injected at one end of the conductor will transmit to the other end.

3 Results and Discussion

The transmission coefficients of the copper nanowire depicted in Fig. 1 for external bias voltages of 0-2 V have been calculated. The total transmission spectra as a function of the electron incident energy for zero and 1.0 bias voltages applied to the system are shown in Figs. 2(a) and 2(b), respectively. The results indicate that the fluctuation amplitudes of transmission spectra decrease by increasing the applied bias voltage, and the whole transmission spectra shift to lower energies in the presence of the applied bias voltage.

The electronic transport properties of gold nanowire with the structure similar to copper nanowire are presented to compare. The calculated I - V characteristics of each nanowire up to a bias voltage of 2.0 V as non-linear behaviour are shown in Fig. 3. One can see that the theoretical data of the current can be approximately fit into a cubic function of bias voltage drown with dotted lines in Fig. 3.

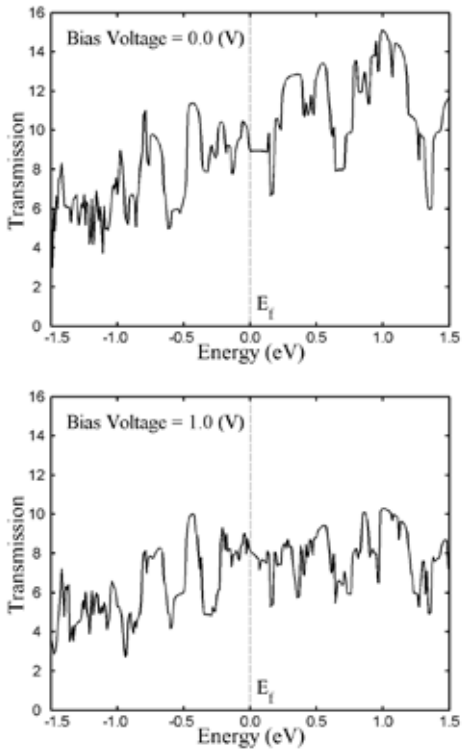

Fig.2: Transmission spectra as a function of incident electron energy. Diagrams (a) and (b) show the total transmission spectra at the biases 0 and 1 V, for copper nanowire, respectively. The Fermi energy is set to be 0 eV.

The numerical integration of equation (8), giving the total current, is carried out in order to obtain the differential conductance by taking the integration step ΔE = 0.01. Based on these calculations, the conductance of Cu and Au nanowires shown in Fig. 4 depends on the applied bias voltage and exhibits non-linearity response for both Cu and Au nanowires. The variation of the conductance is different for the two elements, which in Cu, G(V) varies by 9.24-5.64 and in Au varies by 5.68–3.62 in units of quantum conductance when the bias voltage increases.

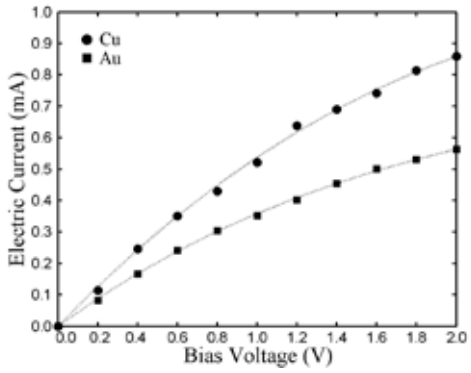

Fig.3: Total current as a function of the applied bias voltage. Dotted lines are the fitting characteristics.

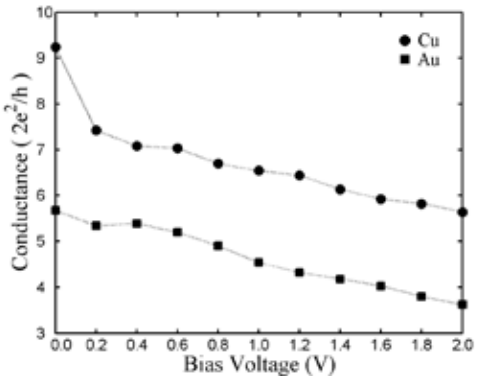

Fig.4: Conductance as a function of external bias voltage for Cu and Au nanowires.

4 Conclusions

In summary, a theoretical analysis of the electronic transport properties of copper and gold nanowires sandwiched between crystalline electrodes in (100) directions has been performed by applying finite voltages, based on the non-equilibrium Green's function within the density functional tight binding calculations. We have shown the dependency of the total transmission fluctuations on the incident electron energy and applied bias voltages. The current-voltage characteristics of each system could be explained as a non-linear function and for the differential conductance in terms of the applied bias voltage the linear response is not valid. In comparison with copper nanowire, gold nanowire exhibits smaller electron conduction.

5 Acknowledgements

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Lithography Independent Fabrication of Nano-MOS-Transistors with Channel Width and Length in the Sub-20 nm-Region

Prof. Dr.-Ing. habil. John Thomas Horstmann
Chair Electronic Devices of Micro and Nano Technique, Faculty for Electrical Engineering and Information Technologies, Chemnitz University of Technology, Chemnitz, Germany

1 Introduction

Regarding the International Technology Roadmap for Semiconductors [1], the down-scaling of the lateral feature size of integrated MOS-transistors will continue for the next 15 years and reach a value below 10 nm. Although the resolution of optical lithography continually increases, up to now, no solutions for mass production of transistors with structure sizes below 40 nm with the needed accuracy and reproducibility exist.

In previous publications we already demonstrated a novel deposition and etchback technique which made it possible to produce transistors with a channel length down to 30 nm with excellent homogeneity and reproducibility and low demands to the used lithography [2-4]. With that technique only the channel length was manufacturable in the sub-100 nm-region, not the channel width. We now modified and expanded the technique to generate transistors with channel length L and channel width W in the sub-20 nm-region.

2 Structure Definition Process

Fig. 1 shows the significant steps of the structure definition of the MOS-transistor's active area, which defines the channel width of the transistor. The cross sections were generated with the technology simulation software DIOS from ISE Integrated Systems Engineering Inc. [5]. First a pad-oxide is thermally grown and a nitride layer is deposited by LPCVD (Low Pressure Chemical Vapour Deposition) for the LOCOS technique (Local Oxidation of Silicon). On top of these layers a sacrificial polysilicon layer is deposited and structured by conventional optical lithography, Fig. 1a. The resolution of the applied lithography process is not important, because the resist mask only defines the local position of the transistor's channel area, but not the geometrical size (in this case channel width) of the transistor.

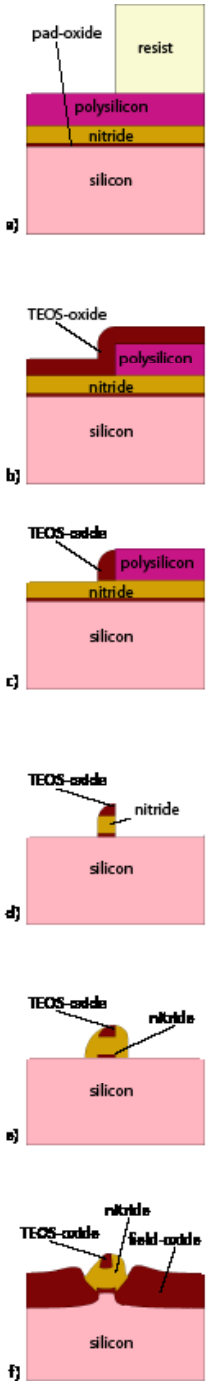

Fig.1: Process steps of the deposition and etchback technique to define the transistor's channel width (simulation results)

After the removal of the resist mask a TEOS-oxide layer is deposited conformally, Fig. 1b, by LPCVD and etched back anisotropically in a special RIE-Process (Reactive Ion Etching) until a spacer surrounding the sacrificial oxide layer appears, Fig. 1c. The next step is the removal of the sacrificial polysilicon layer in an SF6-Plasma with high selectivity to all other layers followed by the transfer of the TEOS-nanostructure into the nitride and oxide layer by a high anisotropic RIE-process, Fig. 1d.

If the deposition process for the TEOS-oxide is absolutely conformal and the etchback process is ideal anisotropic, the linewidth is identical to the thickness of the prior deposited TEOS-oxide layer. However, if the real processes are not absolutely conformal respectively anisotropic, the linewidth is thinner but still reproducible and exactly determined by the TEOS-oxide thickness. The accuracy and homogeneity of the linewidth is due to the well controllable layer deposition and etchback techniques very high compared to other lithography techniques for such small structures. We achieve a uniformity of ± 1.5 % over a whole 4 inch wafer and of ± 3 % from wafer to wafer.

To prevent the lateral oxidation under the nitride mask (birds beak), a nitride spacer is formed on the vertical sidewalls of the masking layers by deposition and etchback of a second nitride layer, Fig. 1e. This complete structure is used as mask for the local field oxidation, Fig. 1f. The width of the active area is defined by the thickness of the TEOS-oxide and by the thickness of the second nitride layer, not by any lithography. Due to the high accuracy of layer deposition techniques, sub-100 nm feature sizes with high precision and homogeneity are producible.

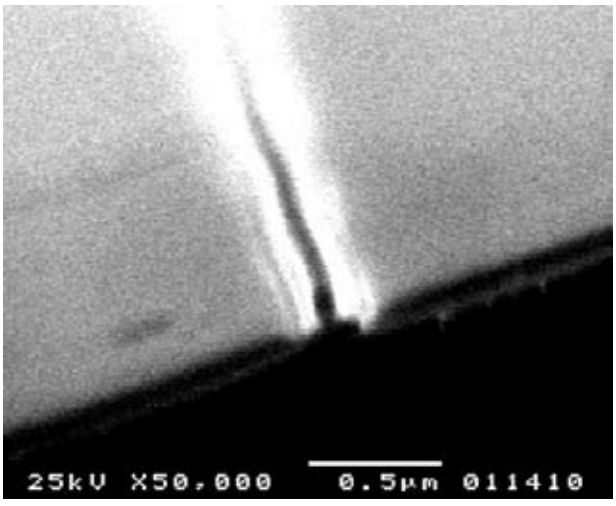

Fig.2: Cross section of a 100 nm wide active area, fabricated with the modified deposition and etchback technique

To generate active area structures with standard dimensions, which are needed for larger transistors or for the contact regions of the Nano-Transistors, a resists mask is structured by normal lithography before the TEOS is etched back.

Figure 2 shows a SEM-photo (Scanning Electron Microscope) of the cross section of an early sample after the local oxidation. In the center the active area surrounded by the field-oxide can be seen. The nitride layer for the masking during the local field oxidation is still on top of the active area.

After the removal of the masking layers by wet etching in hot phosphoric acid and HF-solution the gate- oxide is formed by thermal oxidation and the polysilicon layer is deposited by LPCVD. For the nano-MOS-transistors this polysilicon layer is structured with a similar deposition and etchback technique, while larger structures are masked by a normal optical lithography.

We already presented the deposition and etchback technique for the polysilicon gate electrode before [2-4].

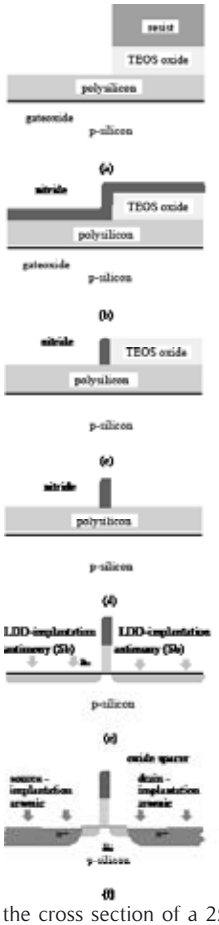

Fig.3: SEM photo of the cross section of a 25 nm wide polysilicon line fabricated with the presented deposition and etchback technique

In this case TEOS-oxide is used as sacrificial layer and nitride is used as masking layer. With the materials of the first deposition and etchback technique masking of a polysilicon layer would not be possible.

Figure 3 presents the significant steps of that structure definition technique, which defines the channel length of the MOS transistor with sizes in the deep-sub-100 nm-region and high accuracy of the line width.

Figure 4 shows a SEM-photo of a 25 nm wide polysilicon line which was structured by the presented deposition and etchback technique.

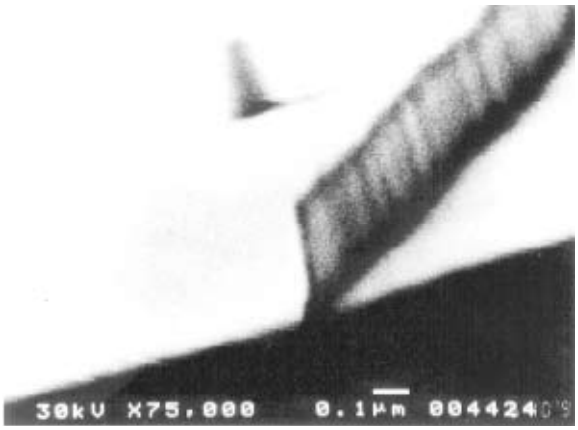

Fig.4: Significant steps of the deposition and etchback technique for the gate definition

The deposition and etchback technique can only generate closed loops of sub-100 nm-wide lines. So additionally to the wanted sub-100 nm-features unwanted parasitic lines occur and cannot be avoided directly. The red arrow in Figure 5 indicates the location of the wanted active channel region.

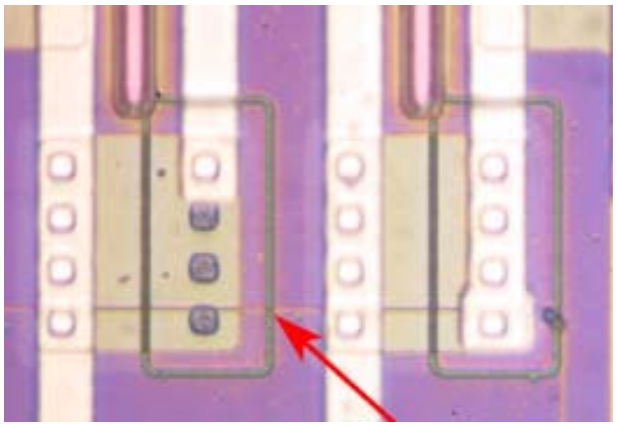

Fig.5: Microscopic photo of an MOS-transistor with W and L in the sub-50 nm-region, the arrow indicates the active channel region

The parasitic polysilicon line has no significant negative influence. The capacity of this line is very low compared to the gate electrode due to the thick field oxide between the line and the substrate.

3 Conclusion

A technique to fabricate real "Nano-Transistors" – MOS transistors with the channel length and the channel width in the sub-50 nm-region – with low demands to the used lithography has been developed. Main idea of this technique is to use optical lithography only to define the local placement of the transistor, while the channel length and width are both defined by deposition and by etching processes with a high precision in the sub-50 nm region. The standard deviation of the linewidth is about 1.5 % on a 4 inch wafer, and around 3 % from wafer to wafer. Only standard CMOS process equipment is used and only a few additional process steps compared to a standard CMOS process are necessary, so the technique is easily transferable to any other CMOS process line.

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First principle approach to the calculation of tunneling current in MOS Structures in the presence of oxygen vacancies

Ebrahim Nadimi[1], Rebecca Janisch[2], Enver Nakhmedov[1], Philipp Plänitz[1], Rolf Öttking[1], Fafa Chiker[1], Frank Thunecke[1], Martin Trentzsch[3], Karsten Wieczorek[3], Christian Radehaus[1]

[1] Opto- and solid state electronics, Faculty for Electrical Engineeringand Information Technologies, Chemnitz University of Technology, Chemnitz, Germany

[2] Department of Materials Science and Engineering, Friedrich-Alexander-University Erlangen-Nuremberg, Germany

[3]AMD Saxony LLC & Co. KG, Dresden, Germany

1 Introduction

Improving the performance of metal-oxide-semiconductor field effect transistor (MOSFET) devices in terms of a higher degree of integration and faster devices has required a larger gate capacitance for each new technology generation. To date, this has been achieved mainly by decreasing the gate oxide thickness, which has reached values as small as 1.5 nm. Gate tunneling current is a major problem at this thickness limit. Such ultrathin layers consist of few atomic layers and therefore within the scope of first principle atomic-scale models. Furthermore, applying an atomic-scale approach provides a method to investigate atomic scale bonding, dislocations and vacancies, as well as their influence on the tunneling current.

In the following report, a combination of density functional theory (DFT) and ballistic transport theory within the non-equilibrium Green's function formalism is applied to the calculation of a Si/SiO_2/Si model interface and the tunneling current through this structure, containing different oxygen vacancies.

2 Atomistic structural model

In most electronic structure calculations different phases of crystalline SiO_2 have so far been employed to generate model interfaces, mainly β-quartz, β-cristobalite and tridymite. We started with crystalline SiO_2 β-cristobalite to model the gate oxide. SiO_2 β-cristobalite has a slightly larger lattice mismatch (about 6%) to Si (001) than tridymite, however, cubic cristobalite has a lot of polymorphs that are almost energetically degenerate and differ only by relative rotations of the SiO_4 tetrahedral units. Thus it can adjust easily to stress and to local distortions e.g. due to a vacancy. The mismatch is minimized if the SiO_2 crystal is rotated by 45° around its c axis. Thus, the lateral lattice constant of SiO_2 was fixed (expanded) to the value of $\sqrt{2}\times a^{Si}$ and the cristobalite cell was relaxed along its c direction. From the "tetragonal" β-cristobalite bulk structure that was produced by this procedure, a slab consisting of seven layers of SiO_2 was composed and put on the Si substrate consisting of nine layers of Si, as shown in Fig. 1. These numbers of atomic layers ensure that bulk properties are recovered in the respective slabs and that the interface does not interact with its periodic image. Note that the interface at the right hand side of the supercell is equivalent to the one in the left hand side, but rotated by 90° around the z direction of the supercell (the direction perpendicular to the interface).

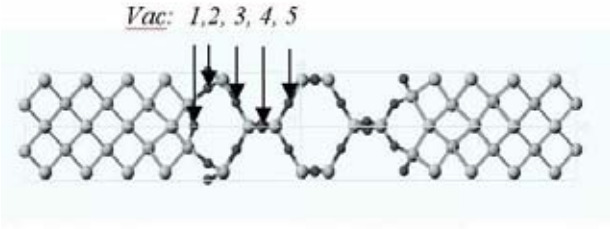

Fig.1: Interface structure model of Si/SiO_2/Si system and the positions of five different oxygen (dark balls) vacancies

To make up for the undercoordination of Si at the interface to SiO_2, extra bridging oxygen atoms were added, completing the coordination. As pointed out in reference [1] by ensuring the preferred coordination number for each Si atom the interface energy is minimized. In this case this also leads to a formal oxidation state +2 of Si at the interface, which is one of the intermediate oxidation states that have been observed experimentally [2].

Different initial separations between the last layer of Si in the substrate and the first layer of Si in SiO_2 were chosen. For all the different configurations the atomic positions were relaxed. In the minimum energy configuration the separation between the last layer of Si in Si

and the first layer of Si in SiO_2 is 2.32 Å. This means an expansion of almost 73% compared to the lattice spacing along [001] in bulk Si (1.34 Å), and of 32% compared to the separation of the Si planes along [001] in bulk SiO_2 (1.76 Å). However, the Si-O bond lengths at the interface are 1.67 Å from the Si substrate to the oxygen layer, and 1.65 Å from the first layer of Si in SiO_2 to the oxygen layer. This represents only a slight extension of less than 2.5% compared to the Si-O bond length of 1.63 Å in the SiO_2 bulk region.

3 Results and discussions

Tunneling is the dominant leakage current mechanism in ultra-thin oxide layers at low bias and can be evaluated using a simple scattering theory approach. The scattering region (thin dielectric layer) is sandwiched between two semi-infinite degenerate (metallic) Si contacts.

We applied the local density approximation (LDA) within the density functional theory (DFT) and the non-equilibrium Green's function formalism (NEGF) as it implemented in the Transiesta [3] code. Norm-conserving non-local pseudopotentials of the Troullier-Martin type were used for all elements. A single-ζ plus polarization (SZP) basis set, which has been shown to produce reasonable results, was used with a cut off energy of 150 Ry in construction of interface model as well as the calculation of I-V characteristics. A 4x4x1 Monhkhorst-Pack k-point mesh is employed during the relaxation of interface and vacancies, while a much denser k-point sampling of 6400 k-points is used in the calculation of current.

The Si electrodes at the left/right side of the oxide layer are doped by substituting one Si atom with P. Because of the small number of atoms constituting the electrode, this substitution corresponds to a very high doping concentration and the Fermi energy is pushed into the conduction band. Alternatively, other authors [4] use an intrinsic Si electrode and artificially adjust the Fermi level at the conduction band edge.

The tunneling current has been calculated, Fig. 2, for oxide without any vacancy as well as oxide with five differently-positioned oxygen vacancies Vac1-Vac5, Fig. 1. Vacancies are built in by removing one oxygen atom and relaxing the atomic coordinate of the supercell.

Vac1 is the so called bridge vacancy and can be considered as an interface defect. Fig. 3 shows two peaks in the density of states at the valence band edge of Si as well as around 0.6 eV above the Fermi energy, due to Si-Si bond at interface. Vac2, the so called arm vacancy, as well as other oxide vacancies (Vac3-Vac5) cause a defect state around 0.2 eV above the valence band of SiO2 in agreement with [5]. Fig. 4 shows the transmission probability of different samples. The very small transmission probabilities around -1 eV represent the band gap of doped Si (≈0.51 eV), while the small transmission probabilities between -4 and 2 eV correspond to the SiO_2 band gap (≈5.85 eV).

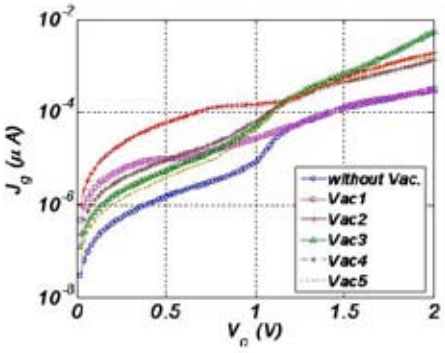

Fig.2: Calculated tunneling current for $Si/SiO_2/Si$ interface model, without and with vacancies

Fig. 2 indicates that the bridge vacancy caused a higher tunneling current at small applied voltages (Vg≤1.2 V) compared to the ideal system. At lower voltages the main contribution to the tunneling current comes from the conduction band electrons of the degenerate Si electrode with energies around the Fermi level. A peak in DOS around 0.6 eV above the Fermi energy in Vac1 provides a high density of empty states and leads to an increase in current. However, increasing the applied voltage above 1.2 V shifts this peak under the Fermi level and charges the interface states, causing these states not to participate in carrying the tunneling current. On the other hand, at high energies the transmission probability of the ideal system and Vac1 become almost equal leading to equal tunneling current at (Vg>1.2 V).

As mentioned above, Fig. 3 shows that vacancies Vac2-5 cause the same defect states near the valence band of SiO_2. However, these states could not participate in the tunneling process due to their large distances from the Fermi energy. They cause changes in the potential landscape of the barrier and consequently in the transmission probability of the scattering region. These changes around the Fermi energy are depicted in Fig. 5. The transmission probability of Vac2 around the Fermi energy is considerably higher than those of Vac3-5, which is the reason for the higher tunneling current of Vac2 compared to the other samples. The same discussion based on transmission probability is valid for the higher current of Vac3 around 2 V.

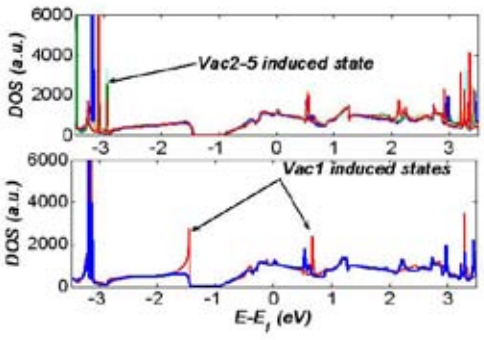

Fig.3: Density of states of the ideal system (thick line-blue) and those containing Vac2-5 (upper-panel) as well as the system containing Vac1 (lower panel)

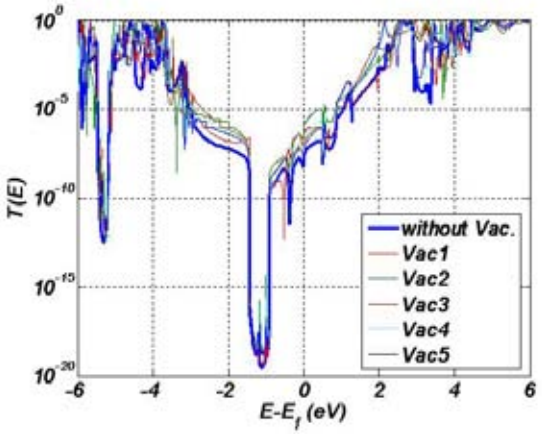

Fig.4: Transmission probability of the ideal system and those containing Vac1-5

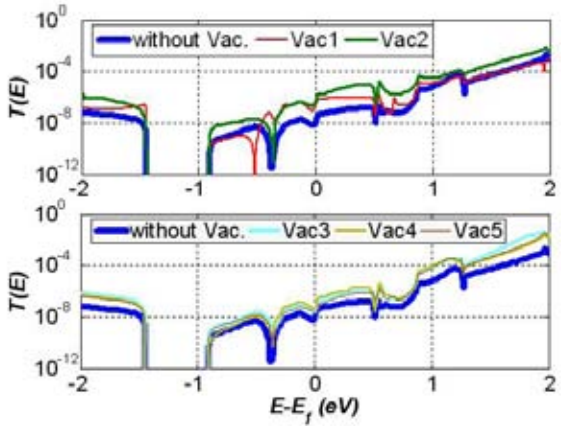

Fig.5: Transmission probability of the ideal system and those containing vacancies

In general all different vacancies are shown to cause an increase in the tunneling current either due to a higher DOS at the conduction band (Vac1) or higher transmission probability around the Fermi energy (Vac2-5). However the bridge vacancy seems to affect the tunneling process only at low applied biases, and acts like an interfacial state, while the arm vacancy has the most destructive effect on the tunneling current at biases under 1 V. Bulk vacancies (Vac3-5) show almost the same behavior with small discrepancies at low and high biases.

4 Conclusions

A combination of DFT and NEGF theory is applied to the construction and calculation of tunneling current through a Si/SiO_2/Si interface model. Several oxygen vacancies are created at different positions in the model structure and their influence on the tunneling current has been studied. The interface vacancy (Vac1) leads to higher tunneling current only at low biases, while bulk oxide vacancies cause an overall increase in tunneling current. The arm vacancy produces the highest tunneling current at low biases.

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Surface energy and wetting behaviour of plasma etched porous SiCOH surfaces and plasma etch residue cleaning solutions

Nicole Ahner[1], Matthias Schaller[2], Christin Bartsch[2], Eugene Baryschpolec[3], Stefan E. Schulz[1,4]

[1]Center for Microtechnologies, Chemnitz University of Technology, Chemnitz, Germany,

[2]AMD Saxony LLC & Co. KG, Dresden, Germany,

[3]Air Products, Lasne, Belgium.

[4]Fraunhofer IZM Chemnitz Branch, Chemnitz, Germany

1 Introduction

With decreasing feature sizes and usage of porous low-k materials within the interconnect system the removal of plasma etch residues becomes a great challenge [1]. Plasma ashing processes using oxidizing chemistries damage the low-k materials and are not able to remove inorganic parts of the residues [2]. Wet cleaning seems to be an alternative, but high aspect ratio features and low energy residue surfaces quite often are not or poor wetted by the cleaning solution [3]. In this work the energetic characteristics of etch residue surfaces, differently plasma etched and stripped low-k dielectric surfaces and several cleaning solutions have been studied to evaluate their wetting behaviour. Additionally contact angle measurements using the cleaning liquids on the studied surfaces have been performed to compare the data.

2 Experimental

Two sets of solid surfaces, provided by AMD, have been studied. Set 1 consists of three blanket etch polymer surfaces generated by a polymerizing plasma etch process using a CF-containing chemistry for 10, 15 and 30 sec. For set 2 porous SiCOH surfaces have been treated by different plasma etching/stripping processes: a 20 sec. etch process, plasma strip 1 and 2 (PS1 and PS2, both reducing) and plasma strip 3 (PS3, oxidizing). Additionally an untreated p-SiCOH surface has been investigated. The cleaning liquids have been provided by Air Products: four commercially available solutions (A: EZSTRIP 511, B: EZSTRIP 520, C: EZSTRIP 530, D: NAC-1) and two experimental liquids (E, F). The surface energy of the solids has been determined using the method of Owens, Wendt, Rabel and Kaelble [4]. The total surface energy of the liquids has been determined by the pendant drop method. The nonpolar part of the surface energy has been calculated using contact angle measurement of the liquid on a PTFE-surface to eliminate the polar part from calculation [5]. Finally the wetting behaviour of the cleaning solutions has been tested on the surfaces of the samples of set 1 and 2. All contact angle measurements have been performed using the KRUSS DSA-100 system.

3 Calculation and Results

Surface Energy. The surface energy of the solid surfaces was calculated from the measured contact angles using the software of the DSA-100. Figure 1 shows the total surface energies and the polar and nonpolar parts. The examined surfaces are quite low-energetic, the untreated ULK surface is nearly completely nonpolar, while the other etched surfaces have a polar part. The nonpolar/polar ratio is changing with different etching processes, leading to a nearly 80% polar surface for PS3. This also leads to an increase of the total energy.

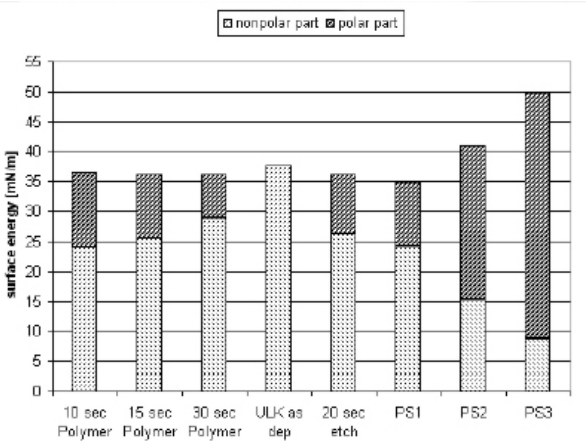

Fig.1: Polar and nonpolar parts and the total surface energy of the evaluated solid surfaces of set 1 and 2 *

The etch polymer surfaces do not change their total energy but move towards nonpolar character with increasing process time. The cleaning solutions show very different energetic characters, Fig. 2. Liquids A and B have low surface energies, liquids C and D show medium surface energy values, while liquids E and F have quite high energies, near to the value of water (72.5 mN/m). The polar and nonpolar part of the liquid's surface energy was determined using a PTFE plate, which is nearly complete nonpolar. So the polar part can be set to zero in the calculation and by measuring the contact angle of the liquid on the PFTE the nonpolar part is the only unknown value as visible in Eq. 1 (γ_l^d: nonpolar part of the liquid's surface energy, γ_l: total surface energy of the liquid, γ_S^d: nonpolar part solid's surface energy, θ: contact angle)

$$\gamma_l^{\,d} = \frac{(\gamma_l \cdot (\cos\theta + 1))^2}{4 \cdot \gamma_S^{\,d}} \qquad (1)$$

By subtracting the nonpolar part from the total surface energy one gets the polar part. The high surface energies of cleaning liquids are a problem if the surface which should be wetted has a low energy. For example water, a very polar liquid with high surface energy, does not wet a PTFE-surface at all. Additionally the energetic characteristic of liquids and surfaces should be comparable to achieve good wetting. Thus by calculating the surface energies of solids and liquids one can make a prediction, which cleaning liquid will provide a good wetting and therefore an effective cleaning. On the other hand, determining the energy of a treated surface can tell a lot about the impact of this process on the surface.

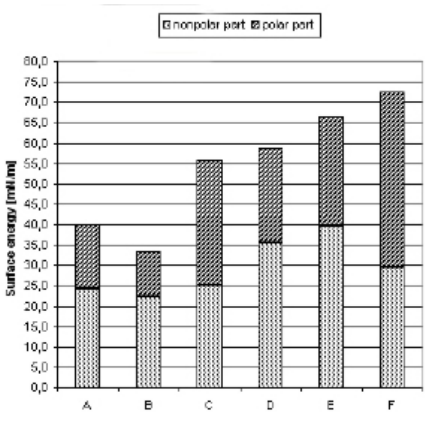

Fig.2: Calculated polar and nonpolar parts and the total surface energy of the cleaning solutions A-F *

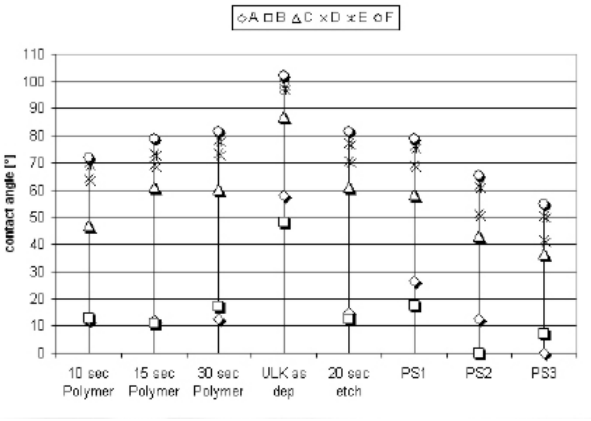

Fig.3: Measured contact angles of the cleaning liquids on the solid surfaces of set 1 and set 2 *

Wetting behaviour. The measured contact angles on the plasma etched/stripped surfaces are shown in Figure 3. Liquid A and B show the best wetting behaviour, both having the lowest contact angles. In some cases they even show complete wetting. The contact angles are much higher for all the other liquids, becoming larger with increasing surface energy of the liquid. The untreated porous ULK surface is an exceptional example because this surface has no polar energy-part. All liquids show high contact angles on this surface, some do not wet it at all. On the other hand higher surface energies of the solid lower the contact angle, as clearly to be seen for the PS3-surface. The polar and nonpolar parts of the surface energies also contribute to the wetting behaviour. For the low-energy-liquids A and B no clear trend is visible, but for all other liquids a decreasing polar part of the solid surface increases the contact angle. This effect is very strong in exceptional situations like for the nonpolar ULK dielectric surface. An increasing polar energy part seems to increase the total energy of a surface as to been seen for the surfaces after PS2 and PS3. Creating a new interface between liquid and solid (wetting) will only happen if the whole system can lower its total energy by doing so [6]. From this point it is clear that a high energy liquid will not wet a low-energy surface and this is also the reason why the increase of the surface energy of the "PS3-sample" lowers the contact angle of the cleaning liquid. Additionally the polar energy part of a liquid can only interact with the polar part of a solid surface, which is also true for the nonpolar parts [5]. Because all of the tested liquids have a polar part the change of the contact angles on solid surfaces with different polar energy parts can be due to this effect.

4 Conclusions

The energetic character of plasma etch polymer surfaces and differently plasma etched/stripped p-SiCOH surfaces has been evaluated by contact angle measurement. The solid surfaces have a quite low energy and change their energetic character after different treatments. The evaluated cleaning solutions show very different energetic characters, from low surface energy for liquid A and B to water-like surface energies for liquid F. The calculation of the surface energies of the solid surfaces and the liquids provides the possibility to make a prediction regarding the wetting behaviour of a special combination of surface to be cleaned and cleaning solution to be used. The wetting experiments show, that at first the total energy of the liquid is the major contributor to wetting behaviour: the lower the energy of the liquid the better the wetting. But also the ratio polar/nonpolar energy contributes to wetting. Due to their low surface energy liquid A and liquid B are best suited to clean surfaces after etching and/or ashing.

5 Acknowledgement

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Efficient Generation of MEMS Reduced-Order Macromodels Using Higher Order Sensitivity Finite Element Technique

Vladimir Kolchuzhin; Wolfram Dötzel; Jan Mehner
Department of Microsystems and Precision Engineering,
Faculty of Electrical Engineering and Information Technologies,
Chemnitz University of Technology, Chemnitz, Germany

1 Introduction

State of the art modeling and simulation tools allow for behavioral analyses of microstructures with fixed dimensions and material properties. Sensitivity analysis and layout optimization require a series of finite element (FE) simulations and subsequent function fit procedures in order to find the relationship between design parameters and component behavior. Especially for a large number of design variables, data sampling and function fit becomes time consuming and prone to errors [1].

The ultimate goal of MEMS component level design is to obtain a macromodel from these accurate results that exhibits just input/output interface terminals of a device by means of internal state variables and can be directly linked into the circuit and system-level schematic. The deformation state and dynamics of flexible electro-mechanical systems can be described efficiently by modal superposition methods. In this technique, the deformation state of the structural domain is described by a weighted combination of linear mode shapes. Capacitance functions with regard to modal amplitudes provide nonlinear coupling between the modes and the electrical quantities, such us electrostatic forces and current. Currently, ROM macromodels are generated by numerical data sampling and subsequent fit algorithms. Each data point must be obtained by a set of separate FE runs in the structural, electrostatic and fluid domains [2].

Advanced parametric modeling technologies based on differentiation of the FE equations have been investigated for mechanical and coupled domain systems in order to improve the computational efficiency of the MEMS reduced-order macromodel generation process. In particular, the time consuming data sampling process in the static and frequency response domains has been replaced by a single finite element run on the basis of the structural, electrostatic and squeeze film analyses with regard to modal amplitudes.

2 Description of the Method

The key idea of the new approach, which account for parameter variations in a single FE run, is to compute not only the governing system matrices of the FE problem but also their partial derivatives with regard to design variables [3].

Difficulties arose mainly from the fact that extraction of high order derivatives (HOD) becomes numerical unstable and time consuming. Automatic differentiation (AD) is known as efficient mathematical algorithm to compute and handle high order derivatives of complicated systems. In contrast to symbolic differentiation which propagates mathematical functions, AD evaluates just numerical numbers extracted at the initial position needed for Taylor series expansion. Differentiation rules describe how to combine partial derivatives in order to form elementary mathematical operations and where to store results in a 3-dimensional array.

As result, Taylor vectors or Pade approximation of the model response can be expanded in the vicinity of the initial position with regard to dimensional and physical design variables. The following diagram, Fig.1, explains the generation process. A test load is applied to the model to simulate the primary motion of the device. Then a modal analysis is performed to compute the mode shapes $\phi_i(x,y,z)$. The test load deflection $\{u(x,y,z)\}$ is compared with the mode shapes $\phi_i(x,y,z)$ in order to select modes which become the state variables of the macromodel. The derivatives of the parameters, characterizing flexible electro-mechanical systems, are extracted from the FE matrices by means of the AD. By using the HOD method, the simulation results become directly polynomial functions in terms of modal amplitudes. Numerical results demonstrate that the generated models are highly accurate in a wide range of modal amplitudes. Taylor series coefficients of the strain energy, mutual capacitances and damping ratios are store in ROM database for further use [4].

3 Conclusion

The advanced simulation technique using differentiation of the discretized FE equations to automatic generating of macromodels has been developed. In linear case, the reduction in expected generation time was at least two times.

It is necessary to point out the necessity for additional memory, parametric mesh-morphing procedures and an access to the source FE code.

The HOD parametric FE technique is a promising alternative to existing data sampling and function fit procedures utilized for MEMS parametric model extraction from ordinary FE analyses. The algorithms support static, modal and harmonic analyses of structural, electrostatic, thermal and fluidic domains. Further work will be focused on extension of the method to nonlinear case and automated generation of the parametric ROM macromodels.

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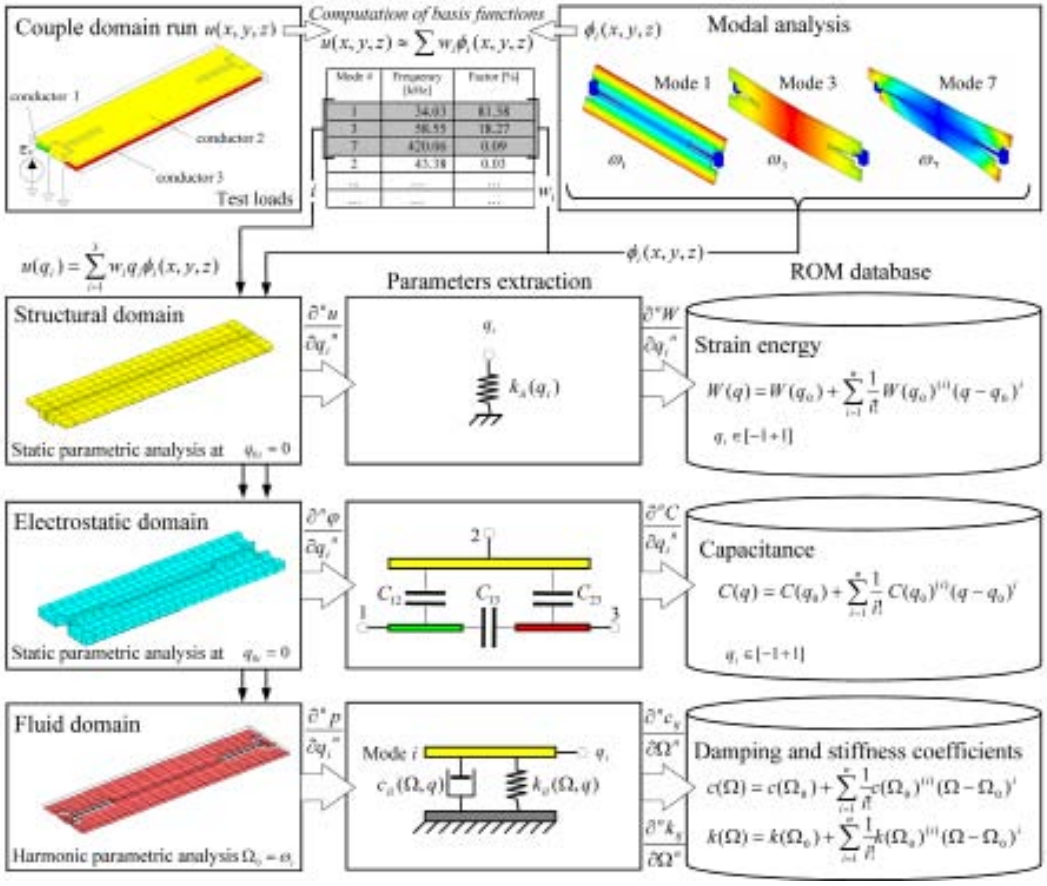

Fig.1: Overview of the data generation for MEMS reduced order macromodel by HOD FE technique

High-Voltage Amplifier Design for MEMS based Electrostatic Actuator Arrays

Steffen Heinz[1]; Andé Lange[1]; Klaus Erler[1]; Gunther Ebest[1]; Wolfgang Miesch[2]; Jürgen Dietrich[2]; Jürgen Knopke[2];Wolfgang Pfau[2]

[1]Chair Electronic Devices of Micro and Nano Technique; Faculty for Electrical Engineering and Information Technologies, Chemnitz University of Technology, Chemnitz, Germany

[2]alpha microelectronics gmbh, Frankfurt/Oder, Germany

1 Introduction

This article describes the design requirements at integrated high-voltage amplifiers for large MEMS based arrays consisting of electrostatic driven actuators. Such actuators will be applied in optical switching arrays for cross connects in wavelength-division multiplexing (WDM) networks.
Important properties of these integrated high-voltage amplifiers are power consumption and waste heat. In particular the chip area must be small enough to facilitate the system integration with MEMS based switching arrays.

Besides a new calculation approach for efficiency of amplifier operation modes a new concept of level-shifter circuitry for switching output stages of high-voltage amplifiers is presented and compared with conventionally level-shifter circuits.

2 Dielectric isolation structures

In the collaborative research center 379 "Arrays of micromechanical sensors and actuators" at the Chemnitz University of Technology one focus of interest are electrostatically driven actuators [2]. Fig. 1 shows a 1-degree of freedom (1D) micro mirror with electrostatic drive.

The flexible plate consists of silicon and forms the upper electrode. The surface is coated with a thin layer of aluminum and forms the mirror with the dimensions: a = 2.8 mm, b = 1.7 mm. The two back-plate electrodes are located on a glass substrate face to the mirror and consist of aluminum. Electrostatic forces tilt of the mirror plate around one axis.

The mirror operation requires high-voltage driver signals to adjusting several tilt angles. Therefore the high-voltage driver signal must be analog or apparently analog.

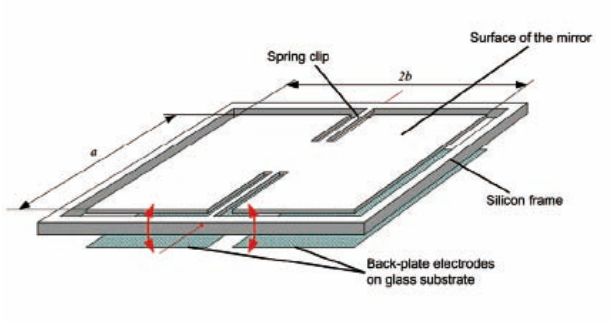

Fig.1: Schematic of 1D-micro mirror

The electrical behavior is dominated by the capacitive component. This component consists of a variable part and a fixed part. The fixed part is eight times higher than the variable part for the actuators described in [3]. The over-all capacity C is less then 2 pF. Due to the small capacity only little energy W_E is necessary to drive electrostatic actuators. Equation 1 indicates the relation (Q .. electric charge, V .. electric voltage).

$$W_E = \int_0^V V \cdot C dV = \frac{Q^2}{2C} \quad (1)$$

Concepts of energy recovery, like in applications with piezoelectric driven actuator, are impracticable. That implies that small power consumption of the amplifier circuitry, in particular in the high-voltage output stage, represents an important demand. This is guaranteed by an efficient amplifier operation and small parasitic capacities in the physical amplifier layout.

3 Efficient amplifier operation

Conventionally (power-) amplifiers are classified in several operation classes in dependence of their dc operation point (OP). Common known operation class designations are class A, AB, B and class D. Thereby class A, AB and B amplifiers have a linear operation mode whereas class D amplifiers switch the output from rail to rail, controlled by pulse width modula-

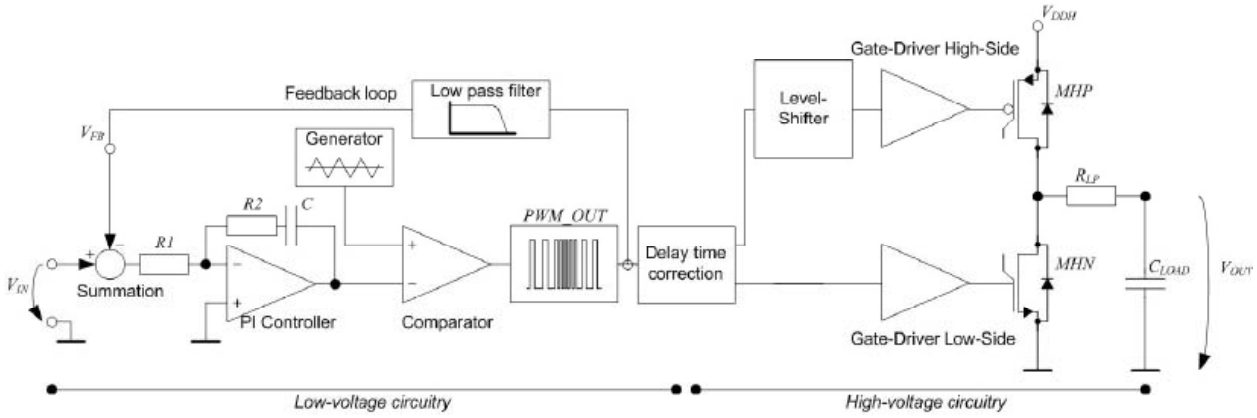

Fig.2: Block diagram of a class D PWM high-voltage amplifier

tion (PWM). For ohmic loads the power efficiency always is least at class A operation and highest at class D operation.

With capacitive loads the behaviour has to be reinvestigated. Amplifiers driving capacitive loads force only reactive power on its output clamps. The power efficiency is defined as the ratio of signal power delivered to the load and the total power consumed by the system. It is calculated by averaging over the cycle duration of sinusoidal signals. The power efficiency is consequently zero in the case of capacitive loads. A new approach has to be established for efficiency calculations of amplifiers with electrostatic driven actuators. The balance of electric charge transfer per unit time should be considered. The procedure of calculation is described in [4].The comparison of operation efficiency reveals the expected dependence of class A operation from modulation range and time constant of the load. Surprisingly, the class D PWM operation shows an equivalent behaviour. The efficiency depends also on the modulation range. Within every switching cycle the charge transferred to the capacitive load also will be transferred to the ground. Therefore the efficiency depends furthermore on the frequency ratio between switching signal and control signal NPP, similarly to a kind of time constant. The efficiency of class B operation is equal one at maximum. A class B operation with constant control signal and with capacitive load is impossible.

A combination of the class A and B operation modes for high-voltage amplifiers with capacitive loads occurs as a logical consequence compared to class D PWM operation in evaluation of these efficiency calculations. A combined class A, class B (not class AB) high-voltage amplifier is demonstrated in [5].

However, the calculation doesn't respect parasitic influences. The concept of the combined class A, class B amplifier needs a feedback coupling inclusive of the high-voltage output stage, likewise an class A amplifier. This feedback loop causes an additional charge transfer and reduces the amplifiers efficiency. The concept of the class D PWM amplifier doesn't needs the feedback coupling inclusive the high-voltage stage. Fig. 2 shows a block diagram for the principle operations.

The amplifier modulates the analog input signal to a square wave carrier frequency by variation of pulse width. The output signal swings from one low-voltage rail to the other. The complete PWM controller only consists of low-voltage devices. The low voltage PWM signal is backcoupled to the summation element. The feedback loop is located in the low-voltage circuitry. The high-voltage circuitry converts the modulated square wave to a high-voltage PWM output signal to drive the capacitive load respectively the micro mirror.

The obtainable signal transfer accuracy depends on rise and fall time of the high-voltage pulse width modulated output signal. The absolute delay time has a secondary importance. But a correct balance of the delay time between high side and low side in the high-voltage output stage is very essential. Due to these interrelations the temperature dependence is small – a weighty factor for array applications.

The demodulation takes place by the actuator. The mechanical resonance frequency is much smaller as the carrier frequency of the amplifier. Therefore the movement of the actuator doesn't follows up the carriers swing. The low pass behavior of the actuator leads to an averaging of the high-voltage output signal and in the issue to analog signal return.

These properties of class D PWM amplifiers rebut its disadvantage ascertained in the efficiency calculation. The class D PWM operation mode is favourable for electrostatic driven actuator arrays.

4 High-voltage level-shifter

The level-shifter determinates the properties of the circuitry first of all as an essential circuit element in the high-voltage switching output stage. Power and chip area consumption will be depending on circuit isolation technology and circuit implementation. A dielectric isolated circuit technology is indispensable for array application. Low leakage currents, small chip area as well as small and voltage independent isolation capacities are the significant properties of this isolation technique [4].

Conventionally level-shifters implementation consumes either a lot of power or much chip area with the effect of low switching speed and high delay time. Dynamic level-shifters must be applied for power saving operation. Diazzi presents a circuit design with two reciprocal switching high-voltage transistors [6].

The transistors on-period is short by pulse operation. Therefore also the current flows in short time only. This circuit concept with the significant signal forms is showed in Fig. 3. However a number of disadvantages make the array application impossible. The non differential operation mode increases the susceptibility to noise. The necessary clamp diodes for over-voltage protection at the nodes V_{X1} and V_{X2} reduce the performance of the circuit by parasitic capacities and therefore increased propagation delay. Moreover the required chip area is grown.

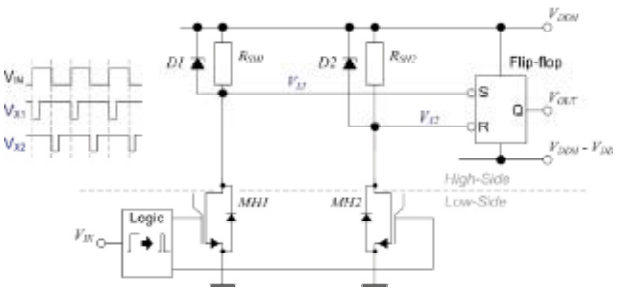

Fig.3: Dynamic level-shifter circuitry [6]

Therefore a new circuitry concept has to be searched. The result, a high-voltage level-shifter with the functional principle of charge pump, is shown in Fig. 4 [7]. This circuitry concept works without high-voltage transistors. The only high-voltage devices are the two pumping capacities. The current consumption is very small. It is determined of the load current in the enabling cycle and the periodic charge transfer between high-side and low side. The cross-coupled inverters in the high-side perform two tasks. The first one is the latch function to solve the switching state. The second one is the over-voltage protection achieved by the substrate diodes of the transistors. Through this the required chip area is small.

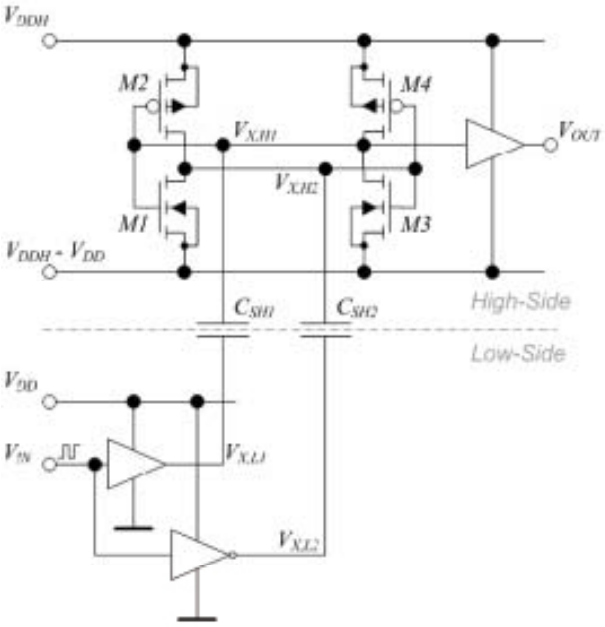

Fig.4: Dynamic level-shifter with charge pump function

The switching-frequency and thereby the propagation delay is determinate of the capacities value. This value can not be any reduced. The capacities must deliver the current to overcome the change-over point of the cross-coupled inverters in the high-side. The maximum current is dependent on edge steepness caused by driver strength of the low-side drivers. The switched-over point of the inverters should be designed to $V_{DD}/2$. The necessary capacities value is then given by (2).

$$C_{SH} = \frac{\beta\left(V_{DD} - V_{TH}\right)^2 t_{R,F}}{3V_{DD}} \qquad (2)$$

The average current consumption in the level-shifter is determined by the voltage variation of the capacities and the switching frequency f_{SW}. Equation (3) describes this bearing.

$$I = 2C_{SH}\Delta V_{CSH} f_{SW} \qquad (3)$$

In the realized version of a high-voltage switching output stage with dynamic charge pump level-shifter principle the capacities value have been determined to 1 pF. That gives an averaging current consumption of approximately 700 nA at a switching frequency of 70 kHz. The only disadvantage of the dynamic level-shifter is the not included generation of high-voltage power supply for the high-voltage PMOS driver. This disadvantage loses attached importance for array applications. For that application the second high-voltage rail will be provide externally. As the result the dynamic charge pump level-shifter is consequently the appropriate circuitry for applications like MEMS based switching arrays.

5 Conclusion

The presented dynamic charge pump level-shifter works in a integrated high-voltage class D PWM amplifier offered by alpha microelectronics gmbh situated in Frankfurt (Oder) Germany. The high-voltage amplifier is separated in two circuits. The high-voltage switching output stage (notation alpha 9112) is fabricated in a dielectric isolated high-voltage technology. The PWM controller (notation alpha 9111) is fabricated in a digital technology with small structure dimensions and works with the bipolar pulse-width-operation mode described in [1]. The alpha 9112 includes 96 high-voltage output stages and has a chip area of 6.0 mm x 6.5 mm. Every of the 96 output stages generate an inverted and a non inverted high-voltage pulse width modulated output signal, delivered to 192 outputs.

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A top-down methodology for MEMS design

Dipl.-Ing. Erik Markert, Dipl.-Ing. Uwe Proß, Prof. Dr. Göran Herrmann, Prof. Dr. Ulrich Heinkel
Chair Circuit and System Design,
Faculty of Electrical Engineering and Information Technologies,
Chemnitz University of Technology, Chemnitz, Germany

1 Introduction

The system complexity is increasing rapidly. In digital domain this steep rise follows Moore's law predicting that the complexity doubles every 18 months [1]. The rise of analog systems is slower but also significant (ADC complexity doubles every five years [2]). MEMS usually consist of analog and digital parts. It is necessary to develop new design methodologies to handle the raising system complexity. Several mixed-signal modeling languages like VHDL-AMS, Verilog-AMS or Modelica support the system developer. But these languages lack of supporting software parts. A new C++ extension library allows modeling of all three domains (analog, digital and software) on a high abstraction level. This SystemC-AMS library [3] is currently under development by an OSCI working group and focusses on communication systems [4].

SystemC-AMS has been tested by the author for the ability of MEMS modeling on several systems (micro mirror array, vibration analysis system and inertial navigation system [6]). It speeds up system simulation significantly (up to 60 times compared to VHDL- AMS) with a small lack of accuracy (about 2 - 4 %). But on lower abstraction level (electrical level, mechanical surface stress analysis) this language currently offers only limited appropriate modeling and solving constructs for MEMS. So it is necessary to switch the modeling language for component refinement.

2 MEMS design methodology

This paper proposes a top down methodology for MEMS design which is currently under development. In the final version it shall accompany the developer team from the specification formulation down to the final assembly of the system gives an overview of the methodology and the used languages and interfaces.

The designer starts system development by stating the key parameters in textual and tabular form. An ADeVA based tool [5] will check the specification for consistency. It is planned to integrate a knowledge database for estimation of component properties like chip area, power consumption or mechanical parameters. The specification tool will provide a code framework for SystemC-AMS. In this language algorithms can be embedded in modules. Linear electrical and mechanical behavior is also allowed in terms of lumped linear elements like resistors and capacitors. A nonlinear solver is under test. This system model can be simulated to check the interaction of components. For critical system parts (usually the analog electrical and mechanical components) an additional refinement is necessary. Exact simulations on DAE level (differential algebraic equations) are difficult to realize in SystemC-AMS. So a conversion to VHDL-AMS is provided by the framework. In VHDL-AMS the component behavior can be modeled using any time-dependent differential equation. The gained parameters may be used in the high level SystemC-AMS model. Synthesis of the digital components described in SystemC-AMS can be achieved using the export functionality to VHDL. For VHDL various tools allow the realization in ASICs (e.g. FPGAs). Additionally the C++ source code of the SystemC-Model can be used programming a microcontroller or a DSP.

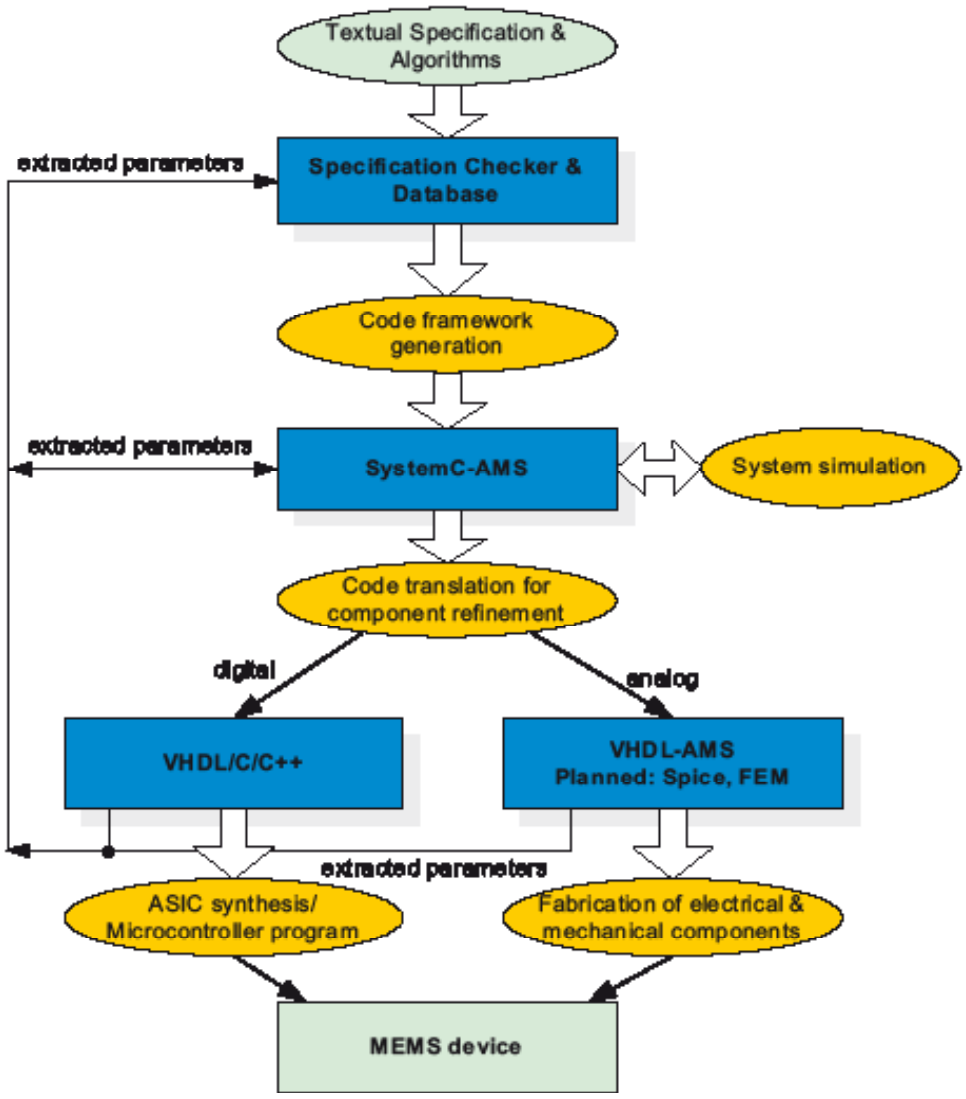
3 Advantages of the methodology

The development process for a new microsystem usually starts with a textual specification of basic functional requirements. Consistency check of the specification is done manually. After finding the algorithms for system realization a mathematical model is implemented for a first simulation check. Then these algorithms are mapped to microelectrical and micromechanical elements.

The new methodology offers an automatic consistency check of the specification. The SystemC-AMS code generator assists the user in code development of the first simulation model. SystemC-AMS is able to simulate all three domains (analog, digital and software) on different levels of abstraction in a fast way. Simulation of complex systems like an inertial navigation system may be done within minutes. The link between SystemC-AMS and dig-

ital synthesizable VHDL is automated as well as the export to VHDL-AMS for component refinement. VHDL-AMS is a well tested language for MEMS simulation and also suitable for Reduced-Order-Modeling [7].

A database of commonly used elements with its parameters will help the designer to speed up the system development.



4 Outlook

The presented methodology is still under development. It is planned to broaden the framework by an interface to FEM simulators and to Spice. The parameter readback from lower abstraction levels to system level should be automated. This allows a continuous check of the system's behavior compared to the specification.

5 Acknowledgments

Parts of the work presented here have been done within the project A2 "System Design" of the SFB 379 (collaborative research center), which is funded by the German Science Foundation (DFG). The proposed methodology is part of the MxMobile project funded by the German Federal Ministry for Education and Research (BMBF).

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New generation of capacitive inertial sensors with high temperature stability

Markus Nowack[1], Danny Reuter[1], Andreas Bertz[1]
[1]Center for Microtechnologies, Chemnitz University of Technology, Chemnitz, Germany

1 Introduction

Inertial sensors are ubiquitous devices of our life. We find them inside mobile phones, notebooks, cars and others. They are used for "freefall" detection, vibration control, tilt sensing for antitheft, shock monitoring, airbag release and dead reckoning. An ever-increasing range of new applications calls for sensor systems offering best performance at low prices. Essential issues for these devices are: fabrication effort including yield, signal to area ratio, calibration effort, signal to noise ratio and temperature drift. The ZfM of the Chemnitz University of Technology and the Chemnitz branch of FHG-IZM have developed a new generation of inertial sensors fabricated by the patented AIM-Technology (Air-gap Insulation of Microstructures). The sensor function in this case is based on detecting the displacement of a proof mass by capacitance change.

2 Technology Aspects

Most of the requirements mentioned above can be met by using silicon technologies with high aspect ratio of structures (HARM = High Aspect Ratio Micromachining). Thus using the third dimension strictly, a large signal to area ratio can be obtained. Additionally, these structures offer overdamping as desired for applications with reduced bandwidth. Among other HARM technologies, like certain SOI procedures, the use of thick epitaxial films or SCREAM (Single Crystal Reactive Etching and Metallization), the AIM technology has additional benefits: its relative simple process flow and the minimisation of mechanical stress caused by thin films or bonded wafers. Additionally, any particle induced residues after deep silicon etching (spikes with diameter not larger than 1.2 µm) are removed by a special lateral etching step which is integrated in the AIM process flow. This means that a yield better than 90% can be achieved even in a cleanroom of class 3 or 4 (according to VDI 2083).

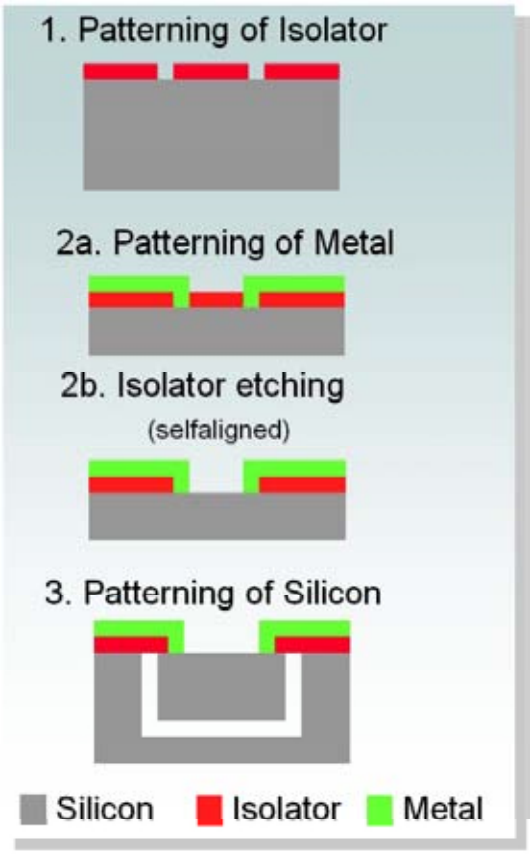

Fig.1: Process flow of AIM technology, showing the anchor area

The basic process flow is shown in Fig. 1. After the last patterning process (step 3), the anchor is electrically isolated and holds the flexure as well as the seismic mass including its electrode plates. The real sensor structure itself (fixed electrodes removed) of the tilt sensor AIM7E is shown in Fig. 2. The four anchor structures (at the edges) as well as the flexures and the perforated mass area can be seen. The whole structure consists of silicon completely. About 95% of the processes can be carried out within a standard CMOS process. The only exception is the silicon etching module at the end of the processing. Nevertheless it has been demonstrated that the DRIE etching system can be used for the polymer spacer based release etch process as well as the lateral etching.

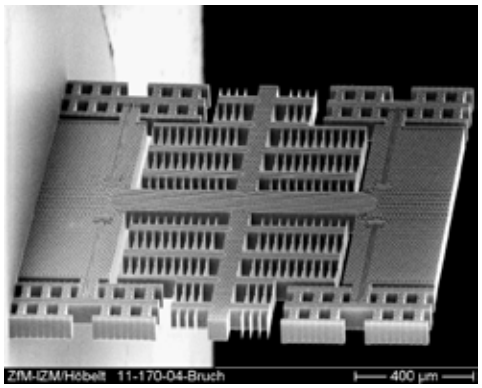

Fig.2: SEM picture of the AIM7E low g sensor having a structure height of 50 µm (fixed electrodes are removed)

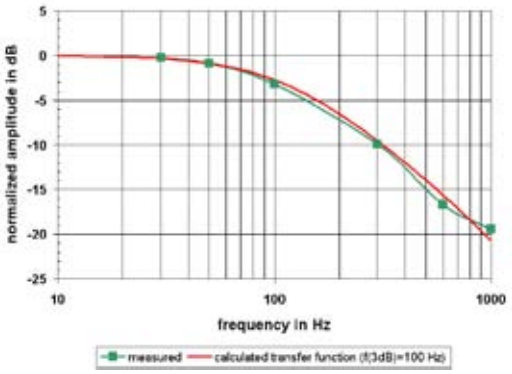

Fig.4: Frequency response of the inclination sensor AIM5i

Thus any wet etching step or even HF vapour etching is not required and technology caused sticking can be excluded. Depending on the application and the device specification, the height of the released structures can be even more than 50 µm. As shown in Fig. 3 the released silicon beams as fabricated for test purposes are almost 100 µm high.

In the following, selected properties of the AIM low g sensors will be presented. Fig. 4 shows the frequency response of the inclination sensor AIM5i. There is a good correlation obtained between the calculation (red line) and measurements for a given damping constant D (green fitted line).

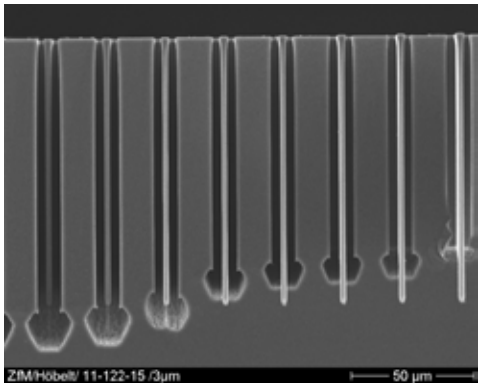

Fig.3: SEM picture of the cross section of released beams with nearly 100 µm height

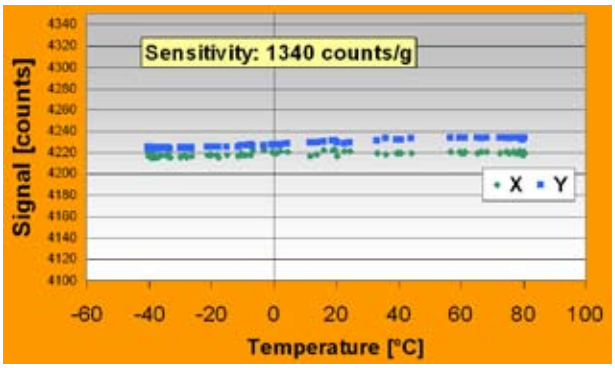

Fig.5: Output signal of a sensor-ASIC systems (AIM7E+ELMOS M777.04) versus temperature (-40°C … 85°C) at 39% relative humidity

3 Functional Test and Characterisation

After complete fabrication including capping by wafer bonding the sensors are tested at wafer level. Beside an isolation test, every sensor is excited by a certain ac voltage at electrode 1. In case the seismic mass is vibrating the oscillation can be detected at the electrode 2 using the second harmonic of the excitation voltage. This procedure has been proven to be sufficient for ensuring the functionality of every single sensor.

As discussed at the beginning, the thermal behaviour of the AIM sensors was expected to be excellent due to the use of crystalline silicon only. Several sensor types have been characterised with respect to their sensitivity change and offset drift vs. temperature. Exemplarily the zero g offset drift of a dual axis sensor AIM7E is shown in Fig. 5. As indicated a coefficient as low as 30 µg/K has been achieved. This is a value which can be reached by other technologies usually only after sensor calibration. Similarly the sensitivity change with respect to the temperature has been measured for several AIM

sensor types. Typically, the coefficients vary from 0 to 0.025 %/K indicating a decrease of the spring stiffness with increased temperature as expected.

Another critical parameter is the noise density. Calculating the mechanical noise only, a density of about 5 µg/Hz1/2 is obtained for the dual axis sensor AIM5i. Using the system combining the same sensor and an analogue ASIC (GEMAC CVC1.0) a total noise density below 20 µg/Hz1/2 could be measured. It is expected that this gap can be further reduced by better matching the device impedances.

4 Contact

Center for Microtechnologies, Faculty for Electrical Engineering and Information Technologies, Chemnitz of Technology, Chemnitz, Germany
Phone +49 (0)371 531 24060
Fax +49 (0)371 531 24069
eMail info@zfm.tu-chemnitz.de
Web http://www.zfm.tu-chemnitz.de/

Fraunhofer IZM, Chemnitz Branch, Chemnitz, Germany

Synthesis and the study of physical properties of a-C:H films deposited from radio-frequency plasma

Klaus Schirmer[1], Josef Lutz[1], Vitali Tarala[2], Tatjana Prohoda[2]

[1]Chair Power Electronics and Electromagnetic Campatibility, Faculty for Electrical Engineering and Information Technologies, Chemnitz University of Technology, Chemnitz, Germany

[2]North Caucasus State Technical University, Stavropol

1 Introduction

The latest decades witness an intense interest in amorphous hydrogenated carbon (a-C:H) as there are extensive potentialities of its application in microelectronics, optoelectronics, microsystem technologies, medicine etc. The carbon capability to form different types of bonds gives an opportunity to precipitate films with different physical and chemical properties. Depending on the deposition method and the chosen synthesis conditions, films with different properties are formed [1-4]. A great number of aspects connected with the understanding of the influence of deposition conditions on the properties of the material have not been completely determined. The combination of different technological factors plays a great role in the formation of a-C:H. In the majority of works devoted to the study of the influence of deposition conditions, as a rule, the role of only one of the technological process parameters is analyzed. The analysis of interference of two or more parameters still represents a difficult task. The object of our work was the study of the influence of two factors (substrate potential and pressure in the reactor) on the speed of deposition, internal stress and electrical properties of a-C:H films.

2 Experimental setup

For the deposition the Roth&Rau production unit «MicroSys 400» was used. It consists in a RF PECVD reactor system of planar type with grounded upper electrode. As substrates n-type Si-wafers have been used. Each substrate was subjected to etching in argon plasma for the purpose of eliminating natural oxide. The deposition was carried out under different potentials of bias supplied to the lower electrode (substrate holder) and under different pressures in the reactor. The gas flow and also the distance between the electrodes were constant in all the experiments. The internal stress in the obtained samples was measured with the automatic plant Tencor FLX-2900. The thickness of the precipitated films was determined in five points of the plate with the «Alpha-Step 500» profilometer. The measuring of voltage-current characteristics of the obtained samples at room temperature, in the range of voltage -10 to 10 V, was carried out with the help of plant «SSM 495 System» with mercury contact.

3 The results and discussion

3.1 The deposition speed

The dependency of deposition speed on the pressure in the reactor (P_r) at different bias voltages (V_{bias}) is shown in Fig. 1. At V_{bias} from -200 V to -800 V, with the rise of P_r, the deposition speed was steadily increasing. This regularity can be accounted for the change of ion and radical quantity in plasma.

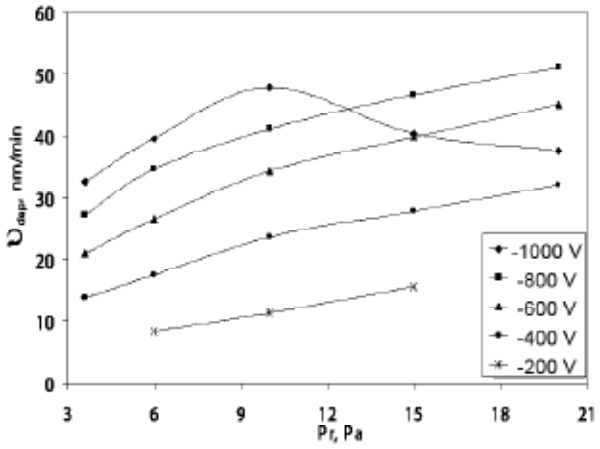

Fig.1: Dependencies of deposition speed on the pressure at different bias potentials.

In spite of the fact that the concentration of active particles is inversely proportional to P_r, their total amount increases, and as the result of this, increases the quantity of ions and radicals capable of forming stable chemical bonds in contact with the surface of the growing film.

At the rise of bias voltage, regardless of pressure in the reactor, the increase in consumable HF capacity was observed. In this case it explains the growth of υ_{dep} with the rise of V_{bias} as the result of changing of the concentration of active particles in plasma. But the influence of pressure and bias potential in the range of their big values is ambiguous. In our opinion, the decrease in υ_{dep} at the rise of P_r to more than 10 Pa is connected with the change of deposition kinetics and with the increased influence of hydrogen etching of the growing a-C:H film. Hydrogen ions posses the capacity for the etching of a-C:H films. With the increase of pressure the efficiency of interaction between the molecules, radicals, ions and electrons has risen and led to substantial changes of the chemical composition of plasma. In particular, it leads to the increase of hydrogen ion concentration in plasma by reason of the rise of the concentration of C_nH_k molecules.

3.2 Internal stress

In Fig. 2 one can see the dependencies of internal stress (σ) on bias potential. At different pressures in the reactor the character of the dependency remains the same. All obtained samples demonstrated high values of σ comparable with the results of the studies [6,7].

The peak values of σ corresponds with the deposition conditions at V_{bias} equal to -400 V. Should V_{bias} increase or decrease, or pressure increases in the reactor, the internal stress in the samples decreased.

According to Davis model [7], the change of internal stress in thin films depends on competing effects connected to the ion bombardment of the surface and the processes of material matrix relaxation. It is well-known that mixing potential supplied to the substrate is the accelerating potential, influencing the energy of plasma particles. At its growth increases the kinetic energy of surface bombarding ions, which is spent on changing of the growing film structure. According to the authors of work [6], for a-C:H films, σ depends on deposition conditions and carries the information about carbon bond types.

3.3 Electrical properties

Typical voltage-current characteristics (I-V) of some samples synthesized within this work are presented in Fig.3. As it is shown in the picture, all of them have symmetric dependencies of current on voltage. The exceptions were the two samples synthesized at V_{bias} equal to -1000 V and at P_r 15 Pa and 20 Pa. In this paragraph these samples are not analysed. It is necessary to note that they had asymmetric dependency of current on voltage which is typical of diode structures. The symmetric character of I-V points at the mechanism of electroconductivity which is limited by bulk properties of a-C:H film.

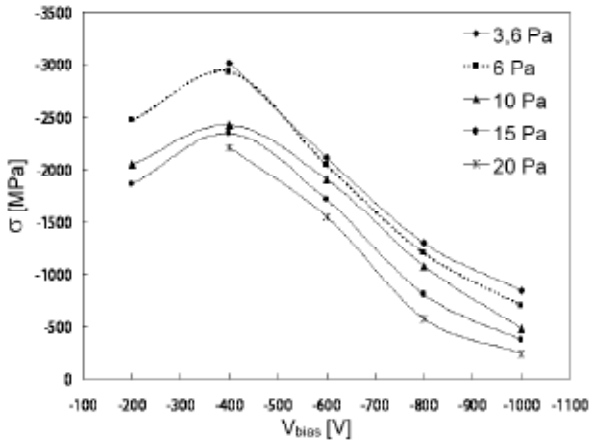

Fig.2: The diagrams of the dependency of internal stress in a-C:H film on V_{bias}.

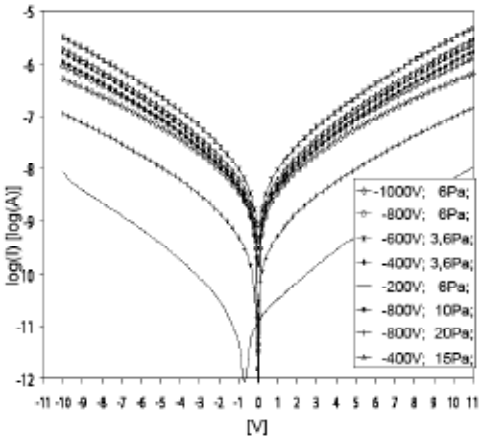

Fig.3: Typical voltage-current characteristics of the obtained samples

In Fig. 4 the dependencies of resistance on V_{bias} at different pressures are shown. The resistance of samples was calculated as electric field strength (E) - current density (J) ratio at voltages equal from 0,1 to 0,5 V. The choice of voltage range of values for the calculation of resistance was determined by the fact that within the range of -0,5 to 0,5 V, linear dependences of J on E were observed.

As it is shown in Fig. 4, under the deposition conditions of a-C:H films in the range of V_{bias} from -400V to -1000V and in the range of pressure from 3,6 Pa to 15 Pa, the resistance of samples practically does not change. It points at slight influence of the chosen

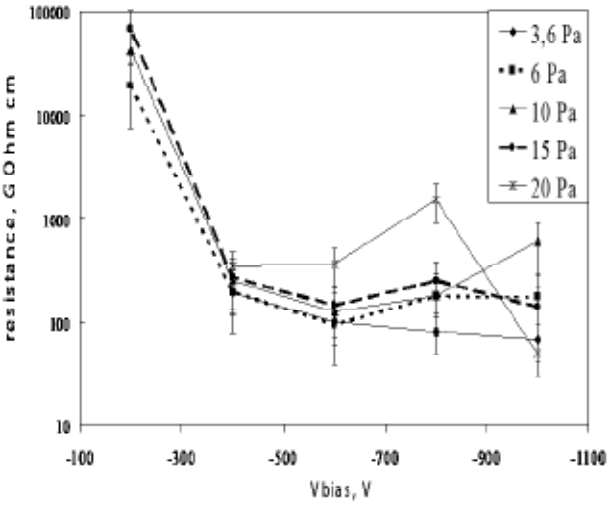

Fig.4: Dependency of resistance of deposition conditions

regimes of deposition on the electrical properties of the samples.

At the decrease in V_{bias} less than -400 V a dramatic change in the value of resistance was observed. At the decrease of V_{bias} to -200 V, occurs the decrease in internal stress in the film due to the increase in concentration of hydrogen and polymer-like clusters. The hydrogen, present in the film, forms bonds with carbon, thereby it decreases the concentration of dangling bonds. Consequently, the increase in resistance is natural for the reason of decrease in defect density in amorphous matrix.

4 Conclusion

On the basis of the undertaken experiments one can point out the following aspects.

- It has been found out that in the low value area of V_{bias} up to -800 V and pressures in the reactor less than 15 Pa the deposition speed has rectilinear dependency on the product of V_{bias} and $P_r^{1/2}$.
- If the pressure increase in the reactor the internal stress at fixed values of bias voltage decreases.
- Within the range of pressures from 3,6 Pa to 15 Pa and within the range of bias voltages from -400 V to -1000 V the resistance in a-C:H films weakly depends on the conditions of deposition. But these conditions influence the microstructure of amorphous matrix, for benefit of it is the evidence of change of internal voltage and the mechanism of electroconductivity in the material. Significant changes in resistance and microstructure of the samples occur during the decrease in V_{bias} less than -400V.

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Some aspects on power cycling induced failure mechanisms

Prof. Dr.-Ing. Josef Lutz, Dipl.-Ing. Marco Feller
Chair Power Electronics and Electromagnetic Compatibility, Faculty of Electrical Engineering and Information Technology, Chemnitz University of Technology, Chemnitz, Germany

1 Introduction

The mayor challenge for higher operating temperatures of power semiconductors is the power cycling capability. With the existent technologies, a significant decrease in power cycling capability was expected for operation temperatures up to 200°C [1]. The maximum operation temperature is mainly limited by the reliability of the assembly and interconnection technology for the required power/temperature cycles.

Known weak points are bond wires and solder interconnection technologies. It is necessary to improve the technology or to replace it by better technologies, to meet the requirements of harsh temperature environment.

2 Some remarks on experiments

Some variables to characterize power cycling tests are explained in Fig. 1. It shows the slope of dissipated power, the die temperature T_j, and the heatsink temperature T_h during one cycle of a power cycling test. The test is adjusted with the parameters T_{high} and T_{low}.

In evaluation of power cycling results, it is not so easy to distinguish the main failure mechanisms. An example of a power cycling test of a standard module at $\Delta T = 123K$ ($T_{low} = 40°C$, $T_{high} = 163°C$) is given in Fig. 2. During the power cycling, the IGBT forward voltage drop V_{CE} at T_{low} is monitored online. Also measured are V_{CE} at T_{high}, forward current I_C, virtual junction temperature T_j and heat sink temperature T_h at the end of the single power pulse, and the thermal resistance R_{thjh} is calculated from these values. For a DC pulse the calculation follows according to

$$R_{thjh} = \frac{T_j - T_h}{V_{CE} \cdot I_C} \tag{1}$$

This method is useful if the duration of the cycle is longer than ca 10s. For short pulses R_{thjc} should be replaced by the transient thermal resistance Z_{thjc}, nevertheless it also provides information about a relative change in R_{thjh}.

Since T_j at T_{high} can increase due to V_{CE} increase, which leads to higher losses, as well as by R_{thjh} increase, one must distinguish both factors. As failure limits an increase of V_{CE} by 5% or an increase of R_{thjh} by 20% are defined. As it can be seen in Fig. 2, the failure limit in this test, V_{CE} +5%, is reached firstly after approx. 10000 cycles. The leaps in the V_{CE} shape indicate lift-off of single bond wires. After 6000 cycles a slow increase of R_{thjh} is observed, which a sign of solder fatigue is. The failure limit of R_{thjh} would be reached at after approx. 11000 cycles. But increase of R_{thjh} is increasing the temperature T_{high}, and this will increase the thermal stress for the bond wires. Therefore solder fatigue is a significant

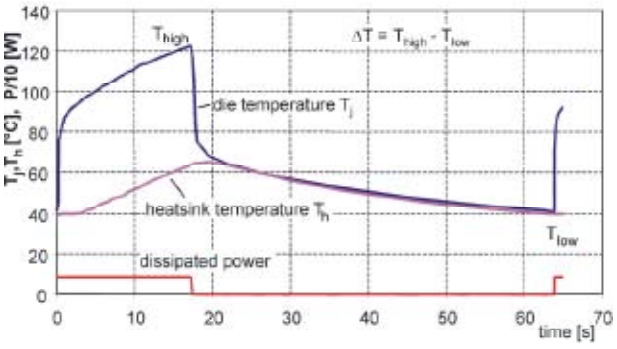

Fig.1: Characteristic variables of a Power cycling test

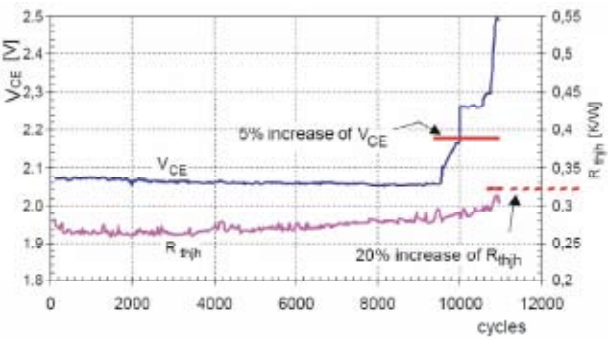

Fig.2: Behaviour of V_{CE} and R_{thjh} in a power cycling test with $\Delta T = 123K$.

failure mechanism in this test; it could even be the main failure mechanism. Power cycling tests need therefore a careful failure analysis. This paper gives some discussion of the failure mechanisms in viewpoint of high junction temperature applications.

3 Bond wires

Bond wires are discussed to be a main weak component. But the bond wire process can be improved significantly. Fig. 3 shows the lift-off picture of an improper bond technology. There is no adherence in the centre of bond area. With improved technology, the power cycling capability of bond wires was significantly improved.

In [2] it was shown, that with improved bond wires in combination with Low Temperature Joining Technique (LTJT) a very high power cycling capability in power cycles up to ΔT = 160K was achieved. In the viewpoint of high temperature applications, bond wires seem not to be the main weak point, if a proper technology is used.

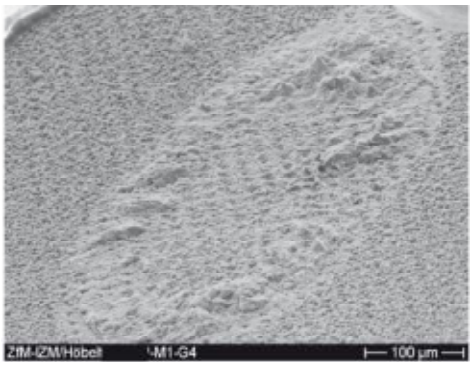

Fig.3: Lift-off pattern as result of power cycling of the device.

4 Solder layers

With improved bond wire technology, limits of solder layers become more and more visible [3]. Using large area silicon dies (>0,5cm²) the hottest spot is under the centre of the device. The degradation of the solder layer starts in the centre of the device for lead free solders, and is not, as often assumed, starting at the edges [4]. This is confirmed by own tests, see Fig. 4.

The start of degradation is also found in the solder underneath the device centre, if lead-rich solders are used. This is not visible in ultrasonic images, but only in a high resolution X-ray image.

It must be noted that these results are in contradiction to models, which assume crack propagation starting at the edges of the devices. Such models are valid for temperature cycling tests, in which the module is heated and cooled passively, and in which a homogeneous temperature is given. During power cycling occur significant temperature gradients between different layers. Especially using semiconductor dies with area >1cm², temperature differences up to 20K are possible between the hot centre and the edge of the silicon die. Correct modelling of power cycling stress will therefore be much more complex.

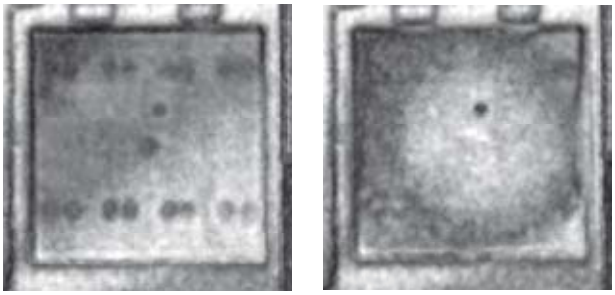

Fig.4: Comparison of unstressed (left) and stressed (right) lead-free chip solder layer. T_{high} = 125°C, ΔT = 80K, 600.000 cycles, ultrasonic image [3]

5 Reconstruction of metallisation

Beside bond wire lift-off and solder degradation, reconstruction of the metallisation occurs, see Fig. 5.

For comparison, Fig. 5a shows an IGBT metallisation after 3.2 millions of power cycles between 85°C and 125°, this figure is taken from [5]. Fig. 5b shows an IGBT metallisation after 7250 power cycles with ΔT = 131K and T_{high} = 171°C. Fig. 5c finally shows the metallisation of a diode after 16800 cycles at ΔT = 160K with T_{high} = 200°C. Significant grains of approx. 5µm diameter and voids between them occur. The increase of reconstruction is visible.

Reconstruction shall not be confused with electromigration. Electromigration is an effect due to high current densities, and its current levels are not reached in power modules. Reconstruction is an effect caused by thermo-mechanical stress.

The reconstruction is comparatively low under the bond wires. Fig. 6 shows a detail of the metallisation adjacent to footprint of a lifted-off bond wire. This diode survived 44500 cycles with ΔT=130K, T_{high} =170°C. The high number of cycles was achieved because of single side LTJT technology [2]. From this observation, we do not suppose reconstruction to be a mechanism which leads directly to bond-wire lift-off.

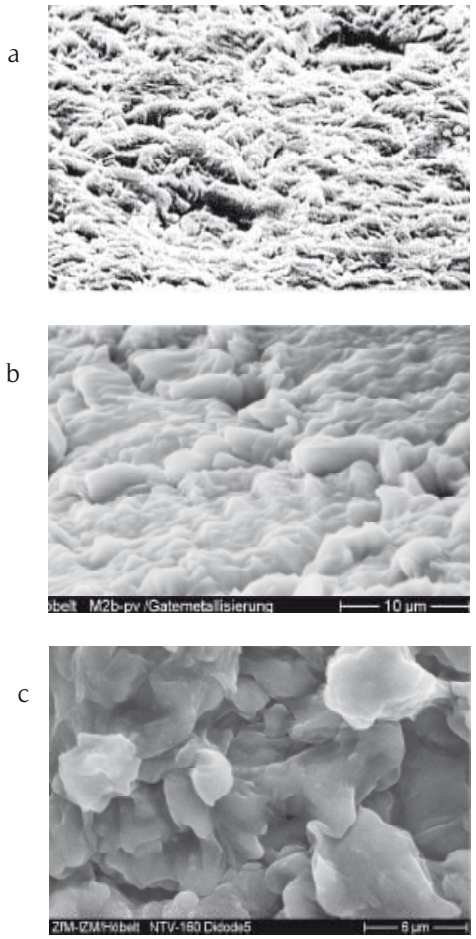

Fig.5: Increase of contact reconstruction with increasing ΔT at power cycling. Fig. 5a taken from [5]

But reconstruction increases the specific resistivity of the metallisation. It can be measured according to the method of van der Pauw [6], see Fig. 7. For symmetrical shape of sample and symmetrical arrangement of contacts holds

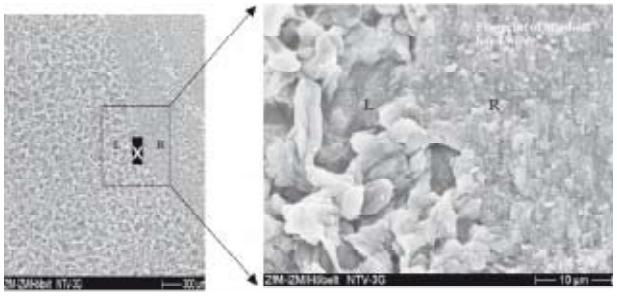

Fig.6: Region adjacent to footprint of a lifted-off bond wire. Diode, failed after ca. 44500 cycles

$$\rho = \frac{\pi}{\ln 2} \cdot \frac{V}{I} \cdot d \qquad (2)$$

In this equation d is the metallisation thickness. This method can be used if the resistivity of the layer is much smaller than the resistivity of the layers below.

For the example of Fig. 5c, which is a diode, a specific resistance of 0.0456 mΩ.m was measured. At an unstressed diode of the same type, 0.0321 mΩ.m was found. This is close to the literature value for pure Al of 0.0266 mΩ.m. The slightly higher value is to expect because the chip metallisation contains some small admixture of Si.

As result, a resistivity increase of 41% for a metallisation with strong reconstruction was found. This will be only of a very low effect to the forward voltage drop. During the power cycling tests of the devices in Fig. 5c and Fig. 6, only a very small increase of the diode

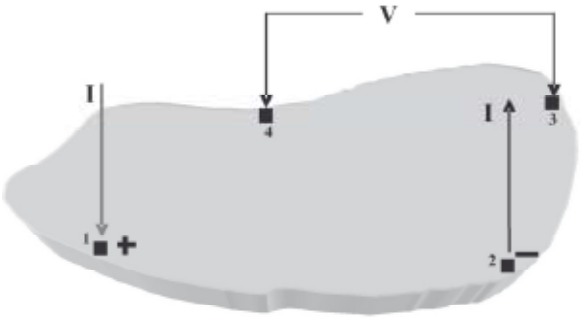

Fig.7: Measurement of specific resistivity ρ according to the method of van der Pauw

forward voltage drop V_F in the range of 20-30mV was observed [2]. Nevertheless, the effect of reconstruction must be regarded and further investigated, because it might affect the current distribution under high stress conditions. This might be of negative influence e.g. on the surge current capability of freewheeling diodes, but this must be further investigated.

6 Conclusion

With improved bond wire technology, limits of solder layers become more and more visible. Beside cracks propagating from the centre to the edge, also fatigue of the solder layers starting from the centre of the devices is found.

Under condition of improved bond wire technology, solder layers become the main weak point in the viewpoint of high temperature environment. Additional, with increasing junction temperature a strong reconstruction of the die metallisation layers occurs. The metallisation below the bond wire is less affected, but the resistivity of the metallisation is increasing significantly.

7 Acknowledgement

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ALD of Copper and Copper Oxide Thin Films for Applications in ULSI Metallization Systems

Thomas Waechtler[1], Nina Roth[2], Steffen Oswald[3], Stefan E. Schulz[1,4], Heinrich Lang[2], Thomas Gessner[1,4]

[1]Center for Microtechnologies, Faculty for Electrical Engineering and Information Technologies, Chemnitz University of Technology, Chemnitz, Germany

[2] Institute of Chemistry, Chemnitz University of Technology, Chemnitz, Germany

[3]Leibniz Institute for Solid-State and Materials Research (IFW), Germany

[4]Fraunhofer IZM Chemnitz Branch, Chemnitz, Germany

1 Introduction

With physical vapor deposition (PVD) being the method of choice to deposit Cu seed layers required for electrochemical Cu filling (ECD) of damascene interconnect structures in ultra-large scale integrated circuits (ULSI), obstacles

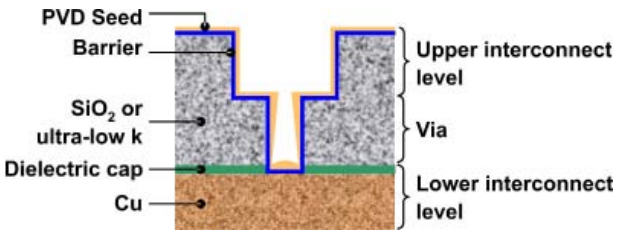

Fig.1: Non-conformal seed layer deposition by PVD in narrow dual-damascene structures.

are being experienced with respect to step coverage and film conformality in nanoscale trenches of high aspect ratio, Fig. 1. Taking into account that for dual-damascene structures of future ULSI devices aspect ratios of 4 to 5 along with a trench width of 15 to 20 nm are expected [1], alternative metallization techniques are highly desirable.

As a possible option for growing Cu seed layers atomic layer deposition (ALD) is therefore under consideration [1, 2]. Nonetheless, the growth of ultra-thin Cu films by ALD is not straight-forward, because suitable ways of reducing the metal precursor while avoiding too high temperatures that would lead to agglomeration of the films have to be found. While several plasma-enhanced (PEALD) methods to deposit metallic Cu have been reported [3-5], pure thermal ALD is of note as it avoids drawbacks related to PEALD such as non-conformality in demanding geometries. To overcome the issues associated with direct, low-temperature thermal ALD, two-step processes have been proposed where copper oxide films are grown by ALD and subsequently reduced [6-8].

The current work therefore is considered with thermal ALD from $[(^nBu_3P)_2Cu(acac)]$ and wet O_2 for growing oxidic Cu films on tantalum-based diffusion barriers as well as on ruthenium and silica. The Cu(I) precursor used in this study is of particular interest as it is a liquid at room temperature and thus easier to handle than frequently utilized solids such as $[Cu(acac)_2]$, $[Cu(hfac)_2]$ or $[Cu(thd)_2]$. Furthermore the substance is non-fluorinated which helps avoiding a major source of adhesion issues repeatedly observed in Cu CVD.

2 Experimental

The precursor $[(^nBu_3P)_2Cu(acac)]$ was synthesized by standard Schlenk techniques according to published methods [9, 10]. Vapor pressure measurements, Fig. 2 display that the volatility of the substance is comparable to $[Cu(acac)_2]$, but

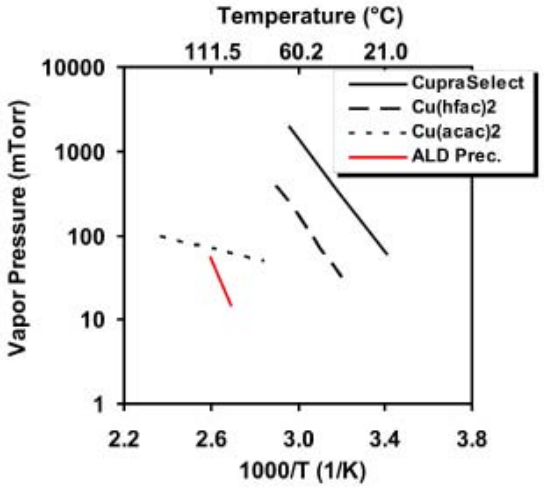

Fig.2: Vapor pressure data of $[(^nBu_3P)_2Cu(acac)]$ compared to other Cu precursors.

much lower to the values of fluorinated substances [(TMVS) Cu(hfac)] (i. e. CupraSelect®) or [$Cu(hfac)_2$].

The ALD experiments were carried out in a single-wafer cold-wall reactor between 110 and 155°C. The precursor was supplied by a liquid delivery system and evaporated at 85 to 100°C, using Ar as carrier gas. Water vapor was introduced by a bubbler.

3 Results and Discussion

As reported previously [11, 12] on Ta and TaN we obtained composites of metallic and oxidized Cu, which was determined by angle-resolved XPS analyses. While smooth, adherent films were grown on TaN in an ALD window up to ~130°C, Fig. 3, cluster-formation due to self-decomposition of the precursor was observed on

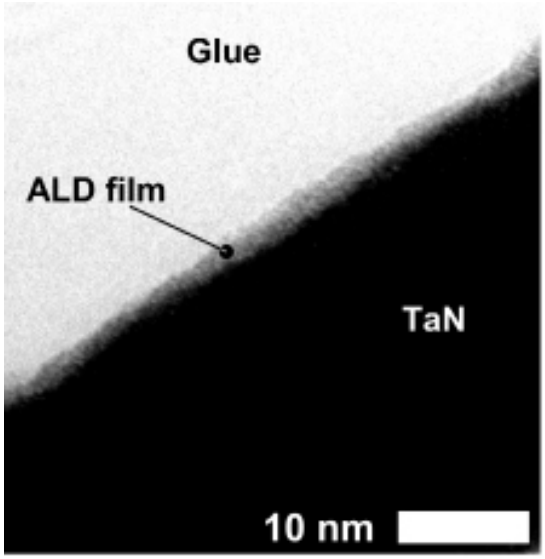

Fig.3: Cross-sectional transmission electron image of an ultra-thin, smooth ALD film grown on TaN at 125°C.

Ta. We also recognized a considerable dependency of the growth on the degree of nitridation of the TaN. In contrast, smooth films could be grown up to 130°C on SiO_2 and Ru, although in the latter case the ALD window only extends to about 120°C, Fig. 4.

To apply the ALD films as seed layers in subsequent electroplating processes, several reduction processes are under investigation. Thermal and plasma-assisted hydrogen treatments are studied, as well as thermal treatments in vapors of isopropanol, formic acid, and aldehydes. So far these attempts were most promising using formic acid at temperatures between 100 and 120°C, also offering the benefit of avoiding agglomeration of the very thin ALD films

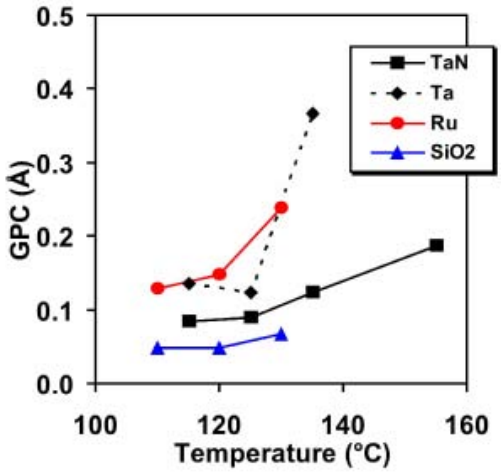

Fig.4: Growth per cycle (GPC) as a function of temperature for ALD on different substrates.

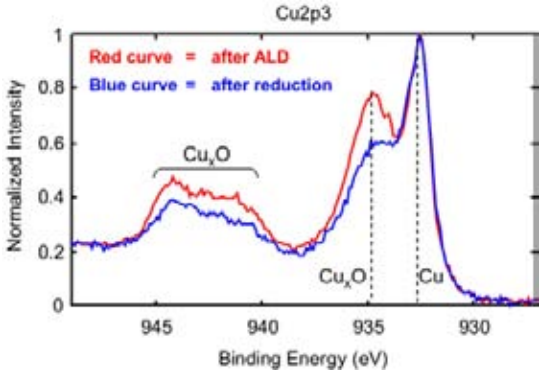

Fig.5: XPS spectra for an ALD film on Ta before and after reduction in formic acid vapor at 115°C.

on Ta and TaN. Fig. 5 displays X-ray photoelectron spectra (XPS) for an ALD film on Ta before and after the reduction with formic acid. Considerable enhancement of the metallic copper fraction is visible. However, some oxidized Cu was also detected which might be due to several weeks of air exposure between the reduction process and the XPS analysis. This result is in agreement with a decrease of the sheet resistance upon reduction in formic acid vapor, also pointing to the formation of conductive material.

4 Summary and Outlook

Thermal ALD of copper/copper oxide composite films on Ta, TaN, Ru and SiO_2 is investigated using the liquid, non-fluorinated Cu(I) β-diketonate [($^nBu_3P$)$_2$Cu(acac)] and wet oxygen as precursors. For all substrates, ALD windows were observed at least up to 120°C and smooth

films could be obtained. On Ta, however, and at elevated temperature also on TaN, cluster formation was observed along with an increase of the GPC due to apparent self-decomposition of the precursor in a CVD-like manner.

For possible applications of the ALD films as seed layers in electrochemical Cu damascene metallization schemes, the films are subjected to reduction processes. So far treatments in formic acid vapor appear most promising. Reduction of films on Ta was already observed at 115°C, hence in the same temperature range as the ALD processes, which helps avoid agglomeration of the films otherwise observed at higher temperature.

Further work will concentrate on optimizing both the ALD and the reduction processes, as well as on applying the ALD films as seed layers for Cu ECD.

5 Acknowledgements

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Evaluation of Airgap structures produced by wet etch of sacrificial dielectrics: Impact of wet etch media on diffusion barriers and copper

Knut Schulze, Stefan E. Schulz, Thomas Gessner
Center for Microtechnologies, Faculty for Electrical Engineering and Information Technologies, Chemnitz University of Technology, Chemnitz, Germany

1 Introduction

The formation of airgap structures is a promising alternative to achieve low-k or even ULK performance for future technology nodes. It has been shown that k_{eff} - values of 2.5 or even significantly lower are well achievable for different integration schemes and MPU generations [1],[2],[3]. Beyond this, several Airgap approaches largely share conventional processing of Cu and SiO_2.

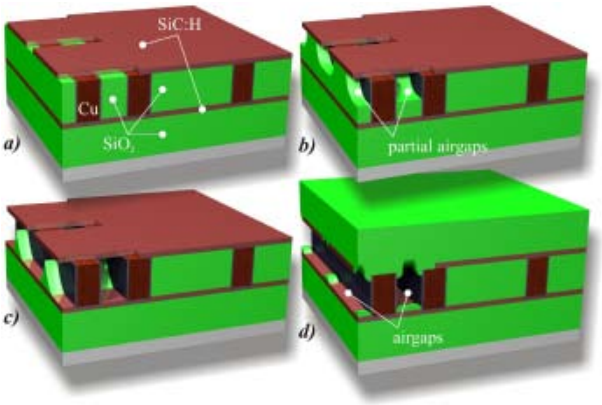

Fig.1: "mask" approach: a) after CMP and "wet-etch-mask" patterning; b) and c) partially wet etched by buffered HF; d) fully removed USG dielectrics, encapsulated airgap structures (using non-conformal CVD)

Two similar sacrificial layer airgap approaches ("mask" and "spacer") were developed at TU Chemnitz. The feasibility of both variants was shown [4] and characterized in terms of their electrical properties (reduction of inter-metal capacitances and k_{eff}) [1]. The general process flows of both approaches is shown in Fig. 1 ("mask") and Fig. 2("spacer"). The removal of the sacrificial PECVD SiO_2 is performed by buffered HF solution (airgap formation). The application of a wet etch treatment is one of the major routes of sacrificial airgap formation known from the literature. The metal lines (Cu) and the dielectric barriers align the wet etch treatment. The functional films for etch stop and masking of both airgap approaches consist of PECVD SiC:H. Critical processes in terms of the reliability of airgap formation were discussed in [5]. The formation of cavities for the "spacer" approach occurs semi-self aligned at the sidewall of the interconnect lines (due to the spacer material, see Fig. 2 b). Because of this mechanism a more relaxed patterning of the wet etch mask can be used and SiO_2 remains in the case of large interconnect spacing and provide mechanical support, compare Fig. 1 and Fig. 2.

This contribution is related to the impact of wet etch media (HF acid) on dielectric and conductive diffusion barrier materials and on Cu interconnect lines, respectively. The exami-nations included blanked film tests and tests on patterned structures.

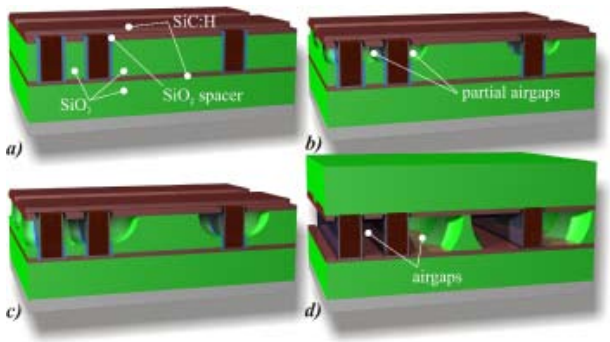

Fig.2: "spacer" approach: a) after CMP and "wet-etch-mask" patterning; b) and c) partially wet etched by buffered HF; d) fully removed USG dielectrics, encapsulated airgap structures (using non-conformal CVD)

2 Experiment

Blanket film tests: Electrical measurements of sheet resistance (Rs) during exposure to HF wet etch media (up to approximately 5 min) were performed for 30 nm films of PVD TaN_X, PVD TiN_X, CVD WN_X and 500 nm films of MOCVD Cu und PVD Cu. The measurements were arranged by the tool Ominmap Rs 50/e (LOT Oriel). Different concentrations of the acid (buffered HF, $HF_{40\%}$/H_2O (2/1), $HF_{40\%}$) and temperatures (20 °C, 40 °C) of wet

etch solution were used for the examinations. Moreover the behaviour of the surface of these materials under HF impact was examined by SEM images and AFM profiles (AFM tool: D3000, Digital Instruments).

Patterned structure tests: The conductive barrier films protect the sidewalls of the copper lines against the impact of HF dilution - if they are totally tight, see Fig. 1 b, c and Fig. 2 b, c. A special technique was developed to examine the closeness of conductive barrier films under HF exposure. This test includes an HF attack from the deposition side which matches the conditions of the real airgap preparations, according to Fig. 1 and Fig. 2. This technology is schematically shown in

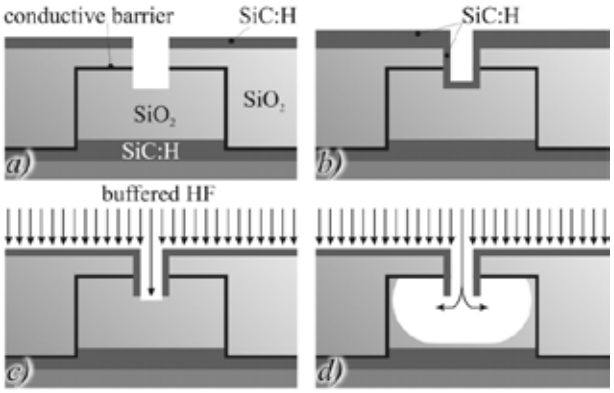

Fig.3: Schematical preparation of the "closeness-test" of conductive diffusion barrier films under exposure of HF acid

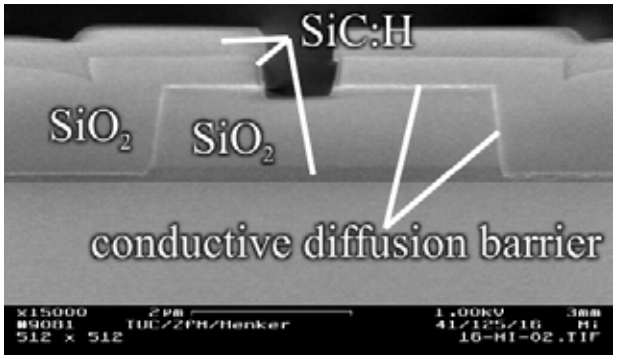

Fig.4: SEM cross-section image of real preparation according to Fig.3 c)

Fig. 3. The conductive barrier materials surround areas of SiO_2 which are undamaged if the diffusion barriers are totally tight against HF media, see Fig. 3 d. In contrast to this HF dilution etches SiO_2 in the encapsulated regions if any defect allows penetration through the conductive barrier films. The "closeness-test" was investigated for different barrier films, varied thicknesses and HF treatment times as well as on vertically and horizontally oriented films. A SEM image of preparations is shown in Fig. 4. The investigations focused on MOCVD TiN_X, PVD TiN_X, CVD WN_X and PVD TaN_X of 10 nm as well as 20 nm thicknesses. The exposure times of each film were 2 min up to 15 min.

3 Discussion

Blanket film tests: All conductive diffusion barrier films show increasing ΔRs with exposure time to HF wet etch media, see Fig. 5. The highest slope occurs for the first 10 s of the treatment at all samples. The subsequent HF treatment affects a leads to a linear slope

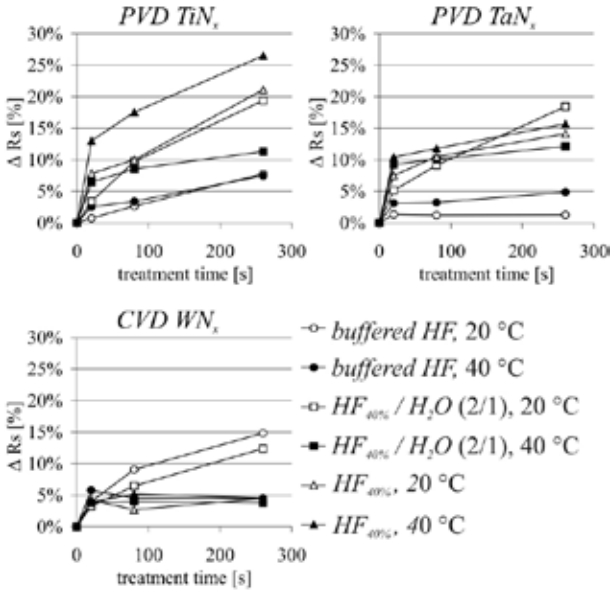

Fig.5: Dependency of ΔRs on exposure time to HF wet etch media to the refractive metal nitrides PVD TiN_X, PVD TaN_X and CVD WN_X

for all samples. The varied HF concentrations as well as both temperatures (20 °C, 40 °C) have different impacts depending on the films. The PVD TiN_X is more sensitive to higher HF concentration (up to 26 % change in ΔRs). Moreover it shows the highest sensitivity compared to PVD TaN_X and CVD WN_X. The influence of a temperature variation is not clear and differs. The PVD TaN_X layer is almost unaffected by buffered HF at room temperature. This is possibly due to the formation of a selfpassivating film. PVD TiN_X and PVD TaN_X show the lowest damage by buffered HF in comparison to higher concentrations. In contrast to this CVD WN_X showed the strongest modification for buffered HF, but it was only slightly damaged by highly concentrated $HF_{40\%}$ and all

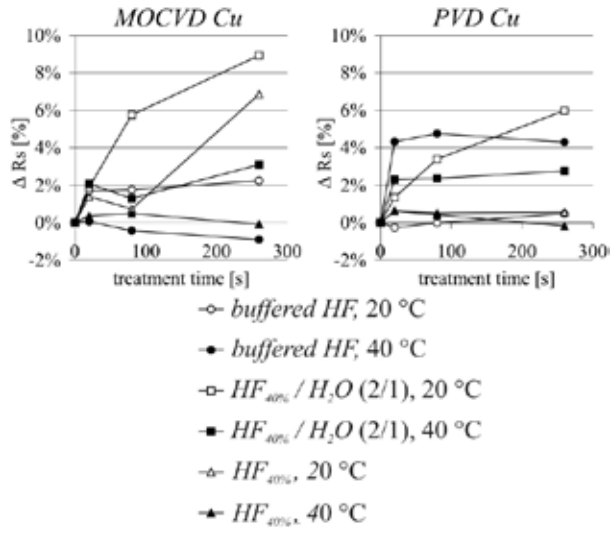

Fig.6: Dependency of ΔRs on exposure time of HF wet etch media to MOCVD and PVD copper films

dilutions at 40 °C. The mechanisms for the Rs increase were not further proven. It is assumed that the wet etch attack occurs primarily at the grain boundaries, followed by a homogeneous thickness reduction. This would also justify the reduced impact for the amorphous CVD WN_X film. Furthermore it is expected that dissolved oxygen (O_2) causes a significant oxidation rate of the barrier film. This mechanism is superposed by the wet etch of oxidized metal films by HF. Higher temperatures of the etch solutions reduce the ability of oxygen dissolving. This would definitely reduce the impact of the wet treatment and appears logical since a temperature variation showed different on the behaviour of Rs. The impact of buffered HF @ 20 °C on Rs values correlates very well to the RMS values of Fig. 7. There is a negligibly low increase of RMS for the PVD TaN_X, but a significant change in the case of PVD TiN_X as well as CVD WN_X films. The copper films show a behaviour similar to the conductive barrier films, see Fig. 6. Diluted HF media induces corrosion [6] (oxidation) of Cu films (in contrast to this, ammonium peroxide mixture (APM, K1) causes passivation of copper films (formation of $Cu(OH)_2$). HF media etches metal oxides simultaneously and reduces the film thickness. First of all an attack at the grain boundaries occurs. The average grain sizes of both films are comparable (both about 220 nm). The PVD Cu is (111) oriented, MOCVD Cu mainly (111) and (100). These morphological distinctions and impurities of both copper films are probably responsible for the different impact of HF media. The RRMS measurements of both copper films, see Fig. 8, show only a slight change under buffered HF exposure. This is also confirmed by comparable AFM profiles before and after wet treatment, see Fig. 8 for MOCVD Cu images.

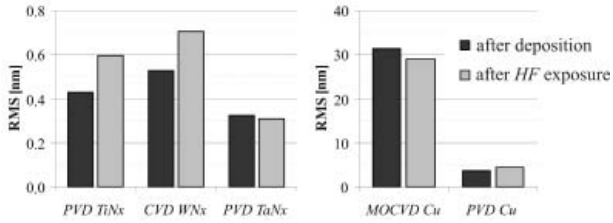

Fig.7: Comparison of RRMS-values of PVD TiNx, CVD WNx, PVD TaNx, MOCVD Cu and PVD Cu immediately after deposition and after exposure to buffered HF for 5 minutes

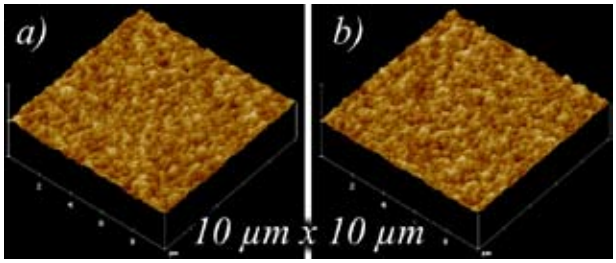

Fig.8: AFM images of MOCVD Cu: a) after deposition; b) after exposure to buffered HF for 5 minutes

Patterned structures tests: Fig. 9 shows the statistical analysis of the "closeness-tests" for different conductive barriers and varied thickness. It was observed that exposure times up to 4 min cause generally no chemical breakthrough of buffered HF even for very low film thicknesses of 10 nm, see Fig. 10 a. The most promising

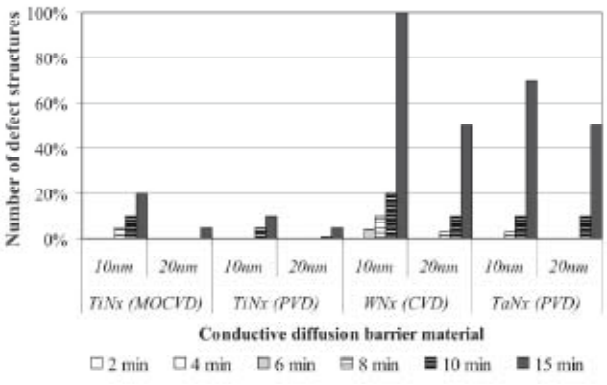

Fig.9: Statistical results of the "closeness-test" for the conductive diffusion barrier films MOCVD TiN_X, PVD TiN_X, CVD WN_X and PVD TaN_X with thicknesses of 10 nm and 20 nm

behaviour shows MOCVD TiN_X. Even after 15 min time of buffered HF impact only 5 % of the structures failed. The highest values of defect rate were observed for the structures which use CVD WN_X. An image of a defect structure of this film is shown in Fig. 10 b. The very low defect rate of MOCVD TiN_X is most likely caused by the thermal,

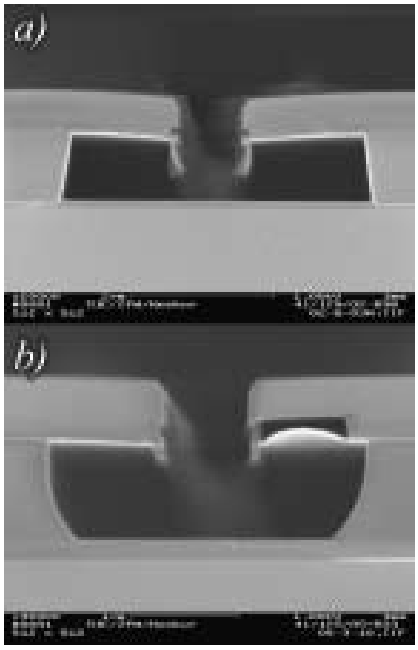

Fig.10: SEM images of preparation accordning to the "closeness-test": a) 15 min MOCVD TiN_X, 20 nm films thickness; b) 6 min CVD WN_X, 20 nm film thickness

plasma-free, deposition process itself. An indication of this is given by the main defect location of the other barrier films PVD TiN_X, PVD TaN_X and CVD WN_X. This was detected especially at the edges and the vertically oriented surfaces of the conductive diffusion barrier films, respectively. Nevertheless a destruction of the barrier films could not be proven by SEM observation directly. The verification of defects of the diffusion barriers was indirectly done by the identification of an attack of the SiO_2 regions.

4 Conclusions

Several conductive diffusion barrier as well as copper films were studies concerning their sensitivity to HF media. The magnitude of impact occurred in a large variety depending on HF concentration, temperature of the media and exposure time, respectively. The ability of oxidation and the morphology of the films are supposed to be the main reasons for the chemical attack. Beyond this, all conductive diffusion barrier films showed high reliability during the "closeness-tests" headed by MOCVD TiN_X.

5 Acknowledgement

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Through Silicon Forming and Metallization for 3D Integration

Ramona Ecke[1]; Lutz Hofmann[1]; Matthias Kuechler[2]; Stefan E. Schulz[2]

[1] Center for Microtechnologies, Faculty for Electrical Engineering and Information Technologies,Chemnitz University of Technology, Chemnitz, Germany

[2]Fraunhofer IZM Chemnitz Branch, Chemnitz, Germany

1 Introduction

Three-dimensional (3D) interconnects by through hole vias (TSV) are one solution for overcoming the increase of delay and power limitations of on-chip 2D interconnects. The directly stacked die interconnections reduce line length, chip size and especially cost. In addition, the 3D integration has the opportunity for hetero-integration, to provide diverse functionally solutions to consumer requirements. Hetero-integration can combine the advantages of different device technologies, such us logic, analog, memory and MEMS, based on incompatible process flows, to fabricate new compact systems. [1]

According to the application of the multi-layered 3D system and therefore combinations of different devices, there exist diverse 3D integration schemes. One of the key roles in 3D chip stacking plays the fabrication and metallization of Through Silicon Vias (TSV) used to electrically connect the dies.

2 Experimental and results

2.1 TSV-Etch

The TSV forming is carried out in 3 steps, etching, passivation and metallization. We are focused on the void free filling of TSVs by chemical vapor deposition (CVD) for metallization. The first crucial condition for TSV filling is the TSV profil after etching.

TSV's are made by deep reactive ion etching (DRIE). This is one of the most critical steps regarding cost and throughput constraints because of high depth (50-150 µm) and partially high density of TSV's. The etch process itself should offer high etch rates, smooth sidewalls, controllable sidewall angle and small mask undercut. Conventional deep Si etching leads to vias with a straight entrance or even with an overhang at the top. For filling of TSV's by deposition of isolation layer, barrier layer and copper this means a pinch-off of the copper film at the via top and a void formation at the lower part of the vias. Better suited are completely V-shaped vias, which is difficult to realize for very deep vias, or at least V-shaped via entrances.

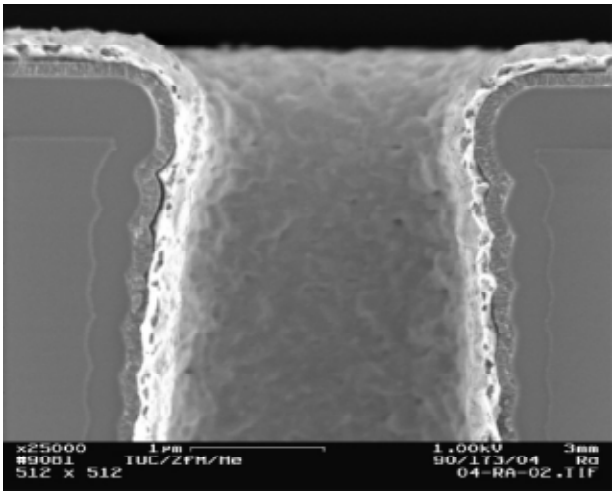

Fig.1: SEM cross section view of the smaller via entrance because of the etch profile and higher step coverage of deposition processes in the upper part in TSVs; leads to via entrance closing without complete fill in via (isolation, CVD-TiN/Cu-CVD)

We fabricated TSV's by DRIE with a modified Bosch process in a STS etching tool. To obtain a tapered opening at the via-top a 4- to 8-step etching process recipe was chosen with a mixture of isotropic and anisotropic etching, Fig. 2. The first step is of isotropic nature with a low bias power and a relative high cycle time, that is reduced cycle by cycle to taper the via-opening. This means lowering of the ratio of etch time to passivation time by each etch cycle. Step 2 is of anisotropic character with a much higher bias power and much lower cycle time. In step 3 the bias power as well as the number of cycles is increased continuously until a certain value is reached which is then held constant in etch step 4. Such a sequence, for which the bias pow-

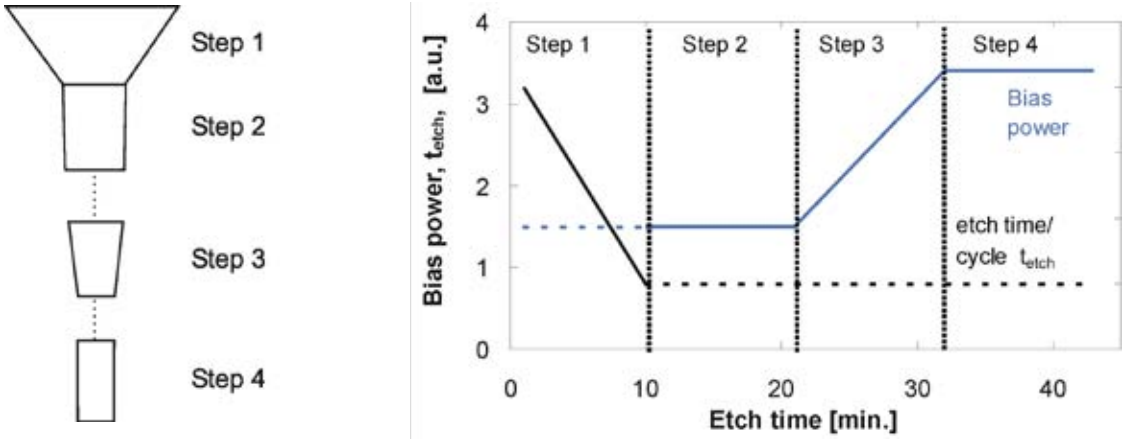

Fig.2: Sketch of the etch sequence (a) and etch power as well as number of cycles versus etch time (b)

er and cycle times are principally shown in Fig. 2b, is used for etch depths up to 50 µm. For higher depths the sequence is extended up to 8 steps repeating step 3 and step 4.

With the etch process described above we obtained a well tapered via entrance. Fig. 3 depicts the profiles of via openings with the multistep process. The figure on the left shows the result of a process which uses one single isotropic etch cycle in etch step one. One can see that there is an undercut of the etch mask and so a wider opening compared to via etched in a conventional process. If the number of etch cycles in step 1 is increased to 4-6 and at the same time cycle time is reduced cycle by cycle the resulting etch profile is as shown in Fig. 3b. The reduction of cycle time leads to a more anisotropic etch and thus the via-opening gets tapered by every cycle. The angle between via wall and the top surface is 80 degree in this case. The surface of the via is slightly waved due to the etch cycles. That effect can be minimized by choosing a highly conformal deposition method (e.g. using TEOS/Ozon chemistry) for the subsequent insulating film.

2.2 Barrier deposition

The required metallization of TSV's needs to be deposited after the electrical isolation in such a way, that reliable electrical interconnects are formed. Mostly the TSV metallization consists of a bi- or multilayer stack of a thin diffusion barrier, adhesion layer and/or seed layer and the conductor material copper. We use CVD processes for barrier and copper deposition especially with regard to the high step coverage of these processes also in high aspect ratio structures (AR > 5).

Currently TiN by CVD is the most promising barrier material for application in 3D integration concerning precursor availability, deposition temperature (< 400°C), good conformality and barrier properties. The TiN barrier layers are produced by a multistep process consisting of alternating pyrolysis steps from TDMAT as pre-

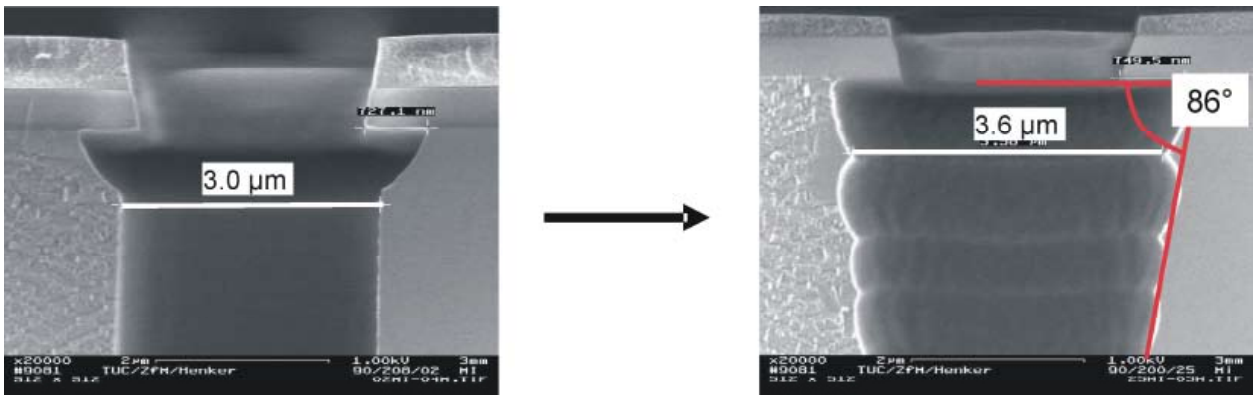

Fig.3: Development steps of the tapered via opening a) one isostropic cycle and b) 4.5 isotropic cycle with decreasing cycle time in step one of the etching process

cursor and plasma treatment steps for densifying. The step coverage in high aspect ratio TSV depends strongly on their geometry and diameter size as well as their depth. With larger diameter the step coverage is improved. In Fig. 4 the step coverage of TiN, deposited with standard conditions, is shown in dependence of TSV diameter.

We counteracted the reduced step coverage in smaller TSV diameter and higher aspect ratios with decreasing of deposition temperature and extension of the pyrolysis step time.

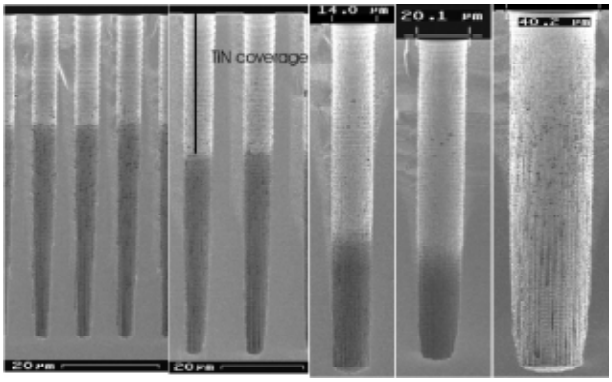

Fig.4: TiN coverage in TSV in dependence of their diameters, with larger diameter better coverage

The step coverage of the TiN barrier depends strongly of via geometry and depth. With the standard process (420°C and pyrolysis step time 5s) the sidewalls of the TSV are covered by the barrier only up to a depth of 4 (ratio opening to depth). If the TSVs are deeper the lower part of the TSV is not covered by TiN. The standard conditions of the process are closed to the transport-controlled regime. With lowering the deposition temperature and increasing the step time of pyrolysis steps the precursor molecules get the chance to reach the via bottom and deposit there. The pyrolysis step time should be optimized for each TSV diameter and depth. In this way a step coverage around 50% at the bottom can be certainly obtained also in aspect ratios > 10.

As well as for the TiN deposition the standard copper CVD process is close to the transport controlled regime. Reducing the deposition temperature leads also to a better step coverage however the deposition rate is drastically reduced. For very high aspect ratios (e.g. ~20) the pressure should be also reduced for a void free filling. The reaction byproducts of copper CVD have low volatility, so it is impeded to remove the reaction byproducts from the lower part of TSV's. This reduces the step coverage and leads to void formation due to the faster closure of the upper part of TSV. The step coverage of copper should be more than 90% to avoid the void formation in a complete copper CVD fill.

2.3 Copper deposition by CVD

In general different deposition techniques are available to realize metal deposition: physical vapor deposition (PVD), electrochemical deposition (ECD, electroplating) or electroless plating and chemical vapor deposition (CVD). Apart from PVD all processes are able to fill high aspect ratio patterns. Figure 5 shows the applicability of different deposition processes and filling concepts depending on the TSV diameter. The pure metal CVD approach is suited for complete TSV fill with lateral width of up to ~3 µm at high aspect ratios. It is currently not clear to which extend the electroplating technology is able to substitute MOCVD (metal-organic chemical vapor deposition) processes for high aspect ratio (HAR) TSV metallization [2, 3]. However, if aspect ratios of larger than 7:1 are to be filled with a conducting material, CVD is the process with the highest currently available conformality. In the region above 3 µm lateral size, several factors impede the application of copper CVD, like process limitations for Cu CVD. In this case, filling can be performed by electroplating. CVD can be used to deposit a so-called seed layer only, which then acts

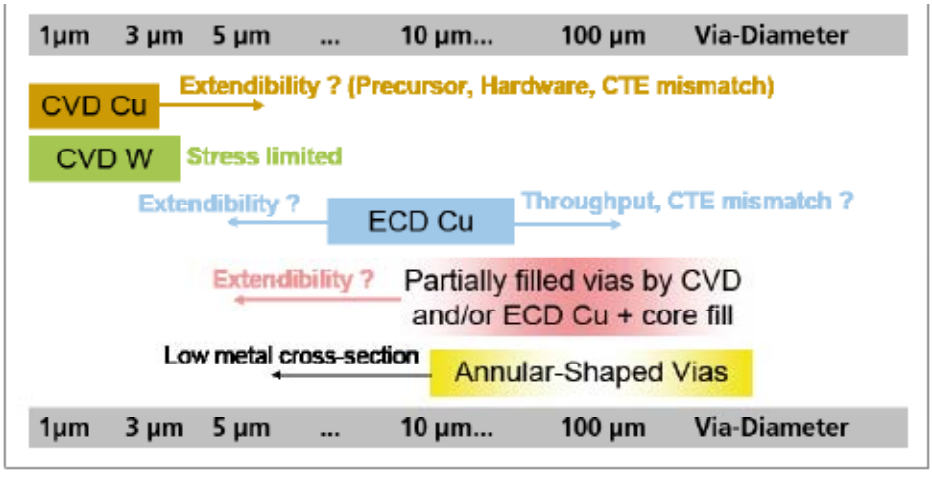

Fig.5: Overview of deposition processes and concepts for metallization of TSVs

as a base layer to grow metals by following electroplating techniques. This is especially of great interest since even most advanced PVD tools are hardly able to cover vias with aspect ratios larger than 7:1 [4, 5].

Depending on the chosen metallization scheme, a thin conducting CVD layer such as Barrier/Cu can be used as a seed layer for the subsequent electroplating process.

The deposition equipment used was a P5000 with a lamp-heated Blanket Tungsten Chamber. The results

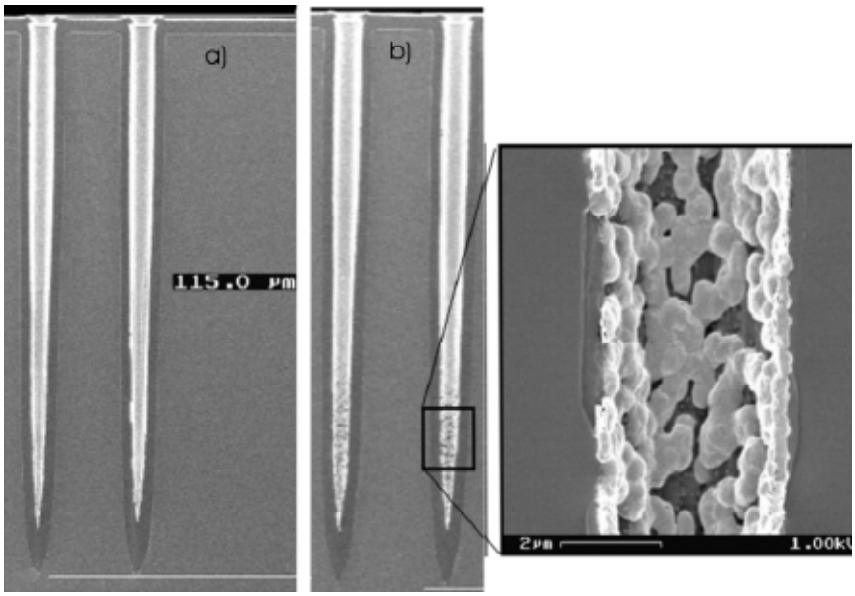

Fig.6: Influence of deposition pressure on coverage in TSV with very high aspect ratio > 20

described in this chapter were obtained with the precursor (hfac)Cu(TMVS) which is evaporated using a liquid delivery system (LDS). This system is composed of a liquid flow meter for the precursor, a mass-flow controller for the carrier gas and a controlled evaporator unit from Bronkhorst. Within the system the precursor is dosed as a liquid with high accuracy and is vaporised just before the deposition. The copper CVD is used for complete fill of smaller TSVs < 3µm diameter and for deposition of seed layer for fill by electroplating.

With copper CVD we obtain very high step coverage of nearly 100% what is account of the deposition rate. This limits the application of copper CVD, on one side for complete fill in small TSV structures < 3 µm or on the other side for the deposit a highly conformal seed layer for further electroplating fill.

3 Summary

The formation of the Through Silicon Vias (TSV) as electrical contact is a very important step in the 3D integration and includes the TSV deep etch and metallization. The formed via profile during the etch process influences the further deposition processes for metallization. The TSV's need a tapered profile for void free filling. However this is difficult to realize in such deep structures with high aspect ratios. So we use a modified etch process for adapted via geometry at the entrance of TSV. This tapered via entrance profile avoids an early closure of TSV before void free filling.

The step coverage of the CVD processes for TiN barrier and Cu were optimized. Lower deposition temperatures lead to film with higher conformality. For the Cu CVD beside the decrease of temperature also the reduction of chamber pressure strongly influences the conformality. Nevertheless the processes have to be adjusted for each TSV geometry and layout with respect to the size, depth and density of TSV's.

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Preparation and investigation of multi wall carbon nanotubes for interconnect applications

Sascha Hermann[1], Stefan Schulz[1,2], Thomas Gessner[1,2]
[1] Center for Microtechnologies, Faculty for Electrical Engineering and Information Technologies, Chemnitz University of Technology, Chemnitz, Germany
[2]Fraunhofer IZM Chemnitz Branch, Department Micro Devices and Equipment, Chemnitz, Germany

1 Introduction

Carbon Nanotubes have outstanding structural, electronic and mechanical properties which open new possibilities for applications in NEMS or in integrated circuit devices.[1] Looking on the requirements for future integrated circuits as listed in the ITRS CNTs are probably the most promising material achieving the challenging aims of smaller feature sizes and higher stress demands where common material systems start to fail.[2] Metallic CNTs have been proposed for nanoelectronic interconnects as the can carry extreme current densities, are more or less insensitive to electromigration and show very good thermal conductivity.[3]

Despite the fact that in fundamental experiments CNTs showed remarkable results there are huge barriers for integration of CNTs in nanoelectronics which have to be overcome. For these and other applications reproducible and scalable production of CNT-based devices has to be accomplished. Furthermore these production processes have to take place at conditions compatible with standard microelectronic process lines as for example at temperatures as low as 450°C. As we are interested in electronic interconnects we focus in this work on the direct growth of MWNTs with catalyst-mediated thermal chemical vapour deposition. This technique allows scalable CNT growth at rather low temperatures. The catalyst (Fe, Co, Ni or alloys [4,5,6, 7,8,9]) defines growth sites and the growth condition of the CNTs. It was found that there is a strong correlation between catalyst particle size and the diameter of the CNTs. This shows the importance of controlling nanoparticle formation as this can control the properties and density of CNT films.

In this work we show basic experiments on the preparation of nickel catalyst particles at different temperatures, from different Ni-thicknesses and on different substrates. The NP-topography was investigated with scanning electron microscopy. Orienting on later on application in electronic devices also silicon samples covered with Al or TiN supporting layers were prepared. We prepared test structures for selective growth of CNTs out of contact holes as a first step towards integration.

The growth of MWNTs under variation of temperature, gas composition and pressure was performed and characterized with SEM, TEM and Raman spectroscopy.

2 Experiment

The most experiments were performed on silicon substrates covered with a 200 nm thick SiO_2 layer prepared by thermal oxidation. On top a very thin Ni film in the range of 1 to 5 nm was deposited with PVD. Aluminium layers with a thickness of 100 nm were sputtered on Si/SiO_2-substrates. For selective growth of CNTs a silicon substrate with a stack of SiO_2/TiN/Cu/TiN/Ni (Fig. 6) was prepared and structured with optical lithography and wet etching steps. The Cu layer was embedded by TiN layers acting as a barrier against copper diffusion and was sputtered by reactive PVD with a thickness of 50 nm. For the selective deposition of the catalyst a lift-off technique was applied.

The preparation of nano-particles and the growth of CNTs was performed in a thermal CVD system. This is a cold wall HV-chamber with a graphite reactor inside especially designed for CNT-growth. The sample holder can capture wafers up to 4". The gas mixture (N_2, C_2H_4, H_2) is spread through a showerhead over the sample. To optimize gasflow for homogeneous CNT-growth on the wafer finite element simulations for different reactor geometries were performed [CoNTemp -project].

Catalyst nanoparticles were prepared by annealing different substrates at temperature ranging from 500°C to 790°C under N_2/H_2 atmosphere. After pre-treatment the sample was rapidly cooled down to conserve the NP state at these conditions. The sample topography was characterized with SEM.

The MWNT samples were prepared by continuing the pre-treatment phase with introduction of ethylene (C_2H_4). We varied temperature, gas composition and pressure and characterization was conducted with SEM, HRTEM and Raman spectroscopy.

3 Results

Our investigations were first focused on the effect of different annealing temperatures, catalyst thicknesses and substrates on Ni nanoparticle (NP) formation, Fig.1-3. The metal films deposited on the interlayer SiO_2 transform into nanoparticles as shown in Fig.1 for 2 nm Ni film at 500°C and 790°C. With increasing temperature the particle size distribution is changed as shown in the histograms. This process is driven by clusters diffusion which increases with annealing temperature resulting in the coalescence of neighbouring particles. As a consequence one gets a bigger spread in particle size distribution with many very small NPs but also with very big particles which are both not favourable for CNT-growth at selected growth temperatures whereas at 500°C a more or less symmetrical distribution with a mean diameter of 30.4 nm was observed.

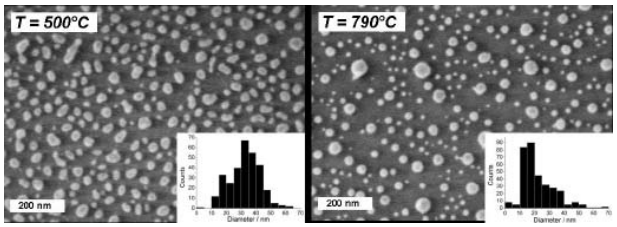

Fig.1: SEM plan views and size distributions of Ni nanoparticles on 200 nm SiO_2 substrates prepared at 500°C and 790°C

Fig. 2 summarizes the SEM results of particle sizes and densities from different Ni-thicknesses. Mean particle diameter shows a linear dependence to the thickness of the starting layer. Meanwhile the density increases with decreasing thickness reaching a value of $3*10^{10}cm^{-1}$ for

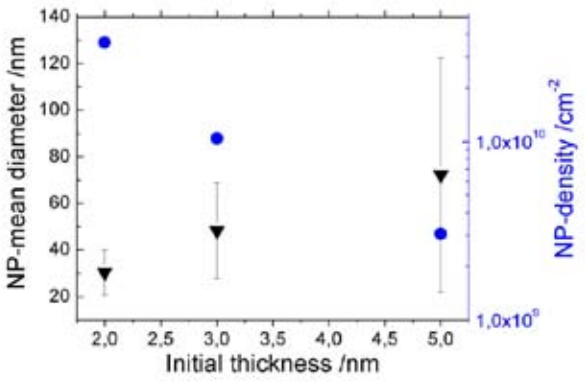

Fig.2: NP-mean diameter and -density as function of initial layer thickness of Ni catalyst at 700°C determined from HRSEM

the case of 2 nm Ni film. It was observed that particle size distribution spreads strongly with thicker Ni-layers and the particles become more uneven. For CNT growth just the thinner catalyst layers are of interest as here the size distributions are much narrower and densities are the highest one. Fig.3 demonstrates NPs prepared on Al support. Obviously Al, which is covered with a thin native oxide layer, effects NP formation as the size distribution shifts to bigger sizes when initial film thickness was 2 nm. This is attributed to lower adhesion forces between Al_2O_3 and Ni. Furthermore NPs on Al show uniform shapes predominantly aligned at the grain boundaries of the underling Al-film.

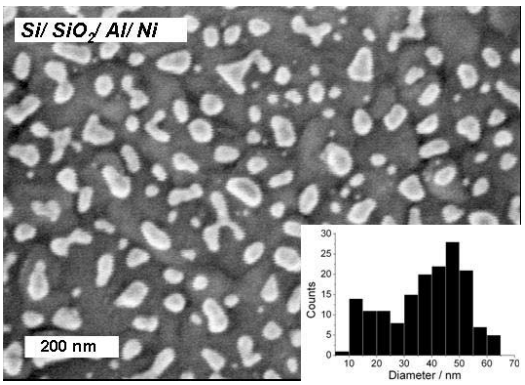

Fig.3: SEM plan views of Ni nanoparticles formed on 200 nm SiO_2 and 100nm Al at 500°C

Fig.4 shows SEM and HRTEM observations of as-grown CNTs on SiO_2 at 500°C and 790°C. For lower temperatures like shown for 500°C a massive growth of twisted MWNTs was achieved whereas higher temperatures conducted to a lower growth rate due to growth kinetics and also a lower growth density but with a better crystallization.

Growth density is also determined by the size and the condition of catalyst particles before CNT growth initiation and can explain the low density achieved at 790°C. As shown above NP size distribution changes with temperature leading to a lower densities of suitable catalysts for CNT growth. This exposes a gap between the conditions for ideal NP formation and the conditions for CNT growth which has to be further optimized. HRTEM observations as shown in Fig.4 (c, d, e) show that predominantly multi walled nanotubes (MWNT) with a diameter of around 20 nm in the tip-growth mode were grown. Increasing temperature affects positively on the crystallinity of MWNTs as seen at Fig.4e where the shell structure of the MWNT could clearly been observed. Further-

more TEM investigations reveal Ni particles inside the CNTs. Some CNTs are even partially filled with Ni material especially observed at samples prepared at high temperatures. It is for this reason that probably Ni is not the right choice for interconnect applications because this metal filling can compromise electronic properties of CNTs.

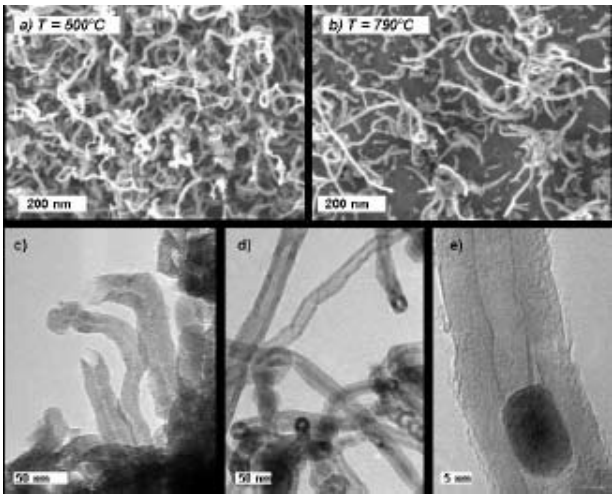

Fig.4: SEM and HRTEM of MWNTs grown at 500°C [a, c] and 790°C [b, d, e] on SiO_2 and a growth time of 10 min

Raman measurements confirm the results from TEM giving an insight into quality of grown MWNTs. Fig 5. shows Raman spectra of CNTs at growth temperatures ranging from 500°C up to 790°C. From the shape and the ratio[10] of these peaks one gets information about morphology of the MWNT samples. To higher temperatures the I_D/I_G ratio reduces to values as low as 0.5 for 790°C which is very good value for MWNTs as they are in general very sensible to defects. The pressure influence was investigated by reducing N_2-pressure to 350 mbar under leaving other parameters constant. Raman spectra reveal that there is a slight decrease in the D-peak suggesting a decrease of defects and amorphous carbon. On the other hand the lower pressure decreases CNT growth rate and catalyst activity leading to a sparse growth of CNTs.

Furthermore the influence of H_2/C_2H_4 ratio during growth process was investigated with Raman and SEM but showed just a slight improvement in quality with increasing H_2 concentration. As a first step towards integration we achieved selective growth of MWNTs on prestructured substrates as shown in Fig.6.

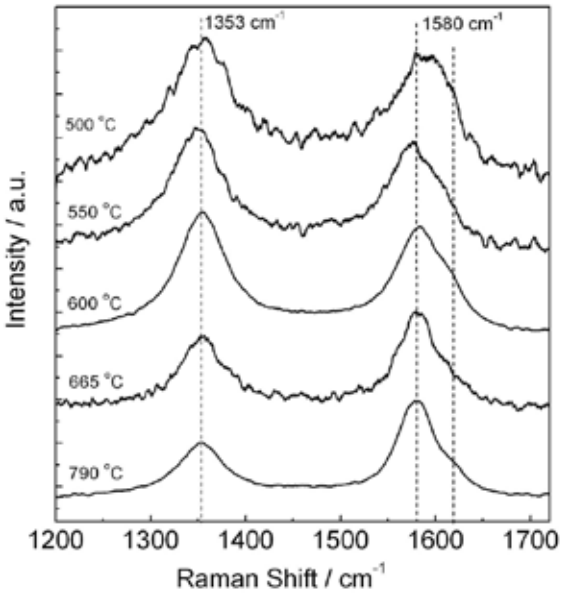

Fig.5: Raman spectra from MWNTs prepared at 500°C...790°C showing the characteristic D-Band (1353cm^{-1}) and G-Band (1580 cm^{-1}).

Massive growth of MWNTs out of 400 nm deep contact holes showed that Aceton treatment could remove very selectively the resist with the Ni on top without harming catalyst activity in the contact holes. This dense CNT-growth also shows that the 50 nm TiN layer prevents sufficiently Cu diffusion also at these high temperatures.

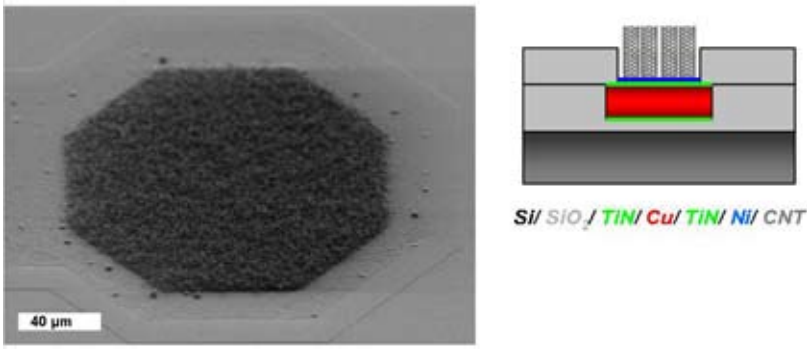

Fig.6: Fig.6: Selective growth of dense MWNTs out of 400 nm deep contact holes on prestructured conductive substrates by CVD at 600°C

4 Conclusions

In summary, a basic study has been conducted on the formation of Ni catalyst nanoparticles on SiO_2 and Al supporting layers for CNT growth. It was found that particle size and density is strongly dependent on initial layer thickness of Ni and shows how to continue to optimize conditions for dense CNT-growth. Looking forward we want to optimize the catalyst/support combination to obtain high density and size homogenous NPs at selected temperatures. The CNT growth was performed on SiO_2, Al and TiN supporting layers and dense films on all supporting layers were achieved. It was found that CNT-growth seems to be affected by temperature, process pressure und H_2/C_2H_4 gas ratio. Furthermore we achieved selective growth of dense MWNTs on pre-structured substrates which will be continued towards preparation of CNT-Via structures. These basic experiments were thought to give an insight into suitable growth conditions for definite CNT growth. As an outlook we intend to continue this investigation but focusing on bimetallic and multilayer catalyst systems to lower CNT-growth temperature and also improving CNT-quality.

5 Acknowledgements

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Non Destructive Characterization of Acceleration Sensor Arrays

Marco Dienel[1]; Jan Mehner[1]

[1]Chair Microsystems and Precision Engineering, Faculty of Electrical Engineering and Information Technology, Chemnitz University of Technology, Chemnitz, Germany

1 Introduction

The characterization of MEMS using traditional destructive methods (SEM of FIB images, polished cut images) leads to high-precision measurement results of the most interesting geometrical parameters – however, dynamical or electrical properties (eigenfrequency, damping and capacitance) cannot be obtained. In contrast the optical characterization in connection with electrical stimuli allows measurement of dynamic properties and geometrical parameters of the surface, only.

A method using eigenfrequencies of MEMS to obtain geometrical parameters of the whole volume and the stress in the structure is developed at the Chemnitz University of Technology [2], the method and the required measurement setup is described in this article. The method is verified at an acceleration sensor array [1].

2 The method at a glance

The method requires three steps. Firstly, a FEM simulation model considering the desired parameters (e.g. spring width, spring height and wedge angle, Fig. 1) has to be created. Afterward the simulated eigenfrequencies are collected in a table.

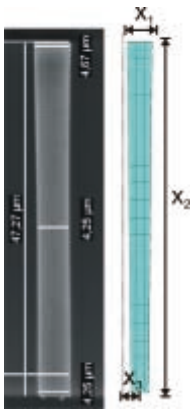

Fig.1: SEM of a spring cross-section and the parameters in the FE-model

In a second step, the eigenfrequencies of the sensor have to be measured and mapped to the corresponding eigenmode, Fig. 2.Finally, using a least squares fit the needed parameters are calculated. Some aspects of realization and of the measurement equipment will be explained in detail.

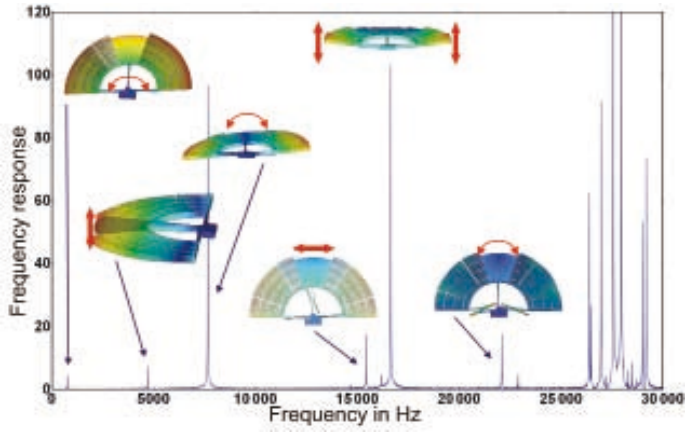

Fig.2: Measured eigenfrequencies and mapping to their simulated eigenmode

2.1 The Simulation

The simulation of a new sensor design with FEM is a standard procedure. The model of a DRIE structured sensor includes parameters like spring height and width. The cross-section is assumed to be rectangular. Fabricated sensors show a variation of the cross-section which at first can be approximated being trapezoidal. Hence, the FE model must be modified to support these parameters. These modifications and the complete patch simulation are done with a self-developed tool [4] which offers an intuitive GUI. This tool allows to set limits for the parameters and an arbitrary function that defines the side wall profile of the MEMS structure. The modal simulations with parameter variation are done automatically. Meanwhile the measurements are performed.

2.2 The Measurement

A Laser Doppler Vibrometer (LDV) is used to measure to motion (velocity) of the electrostatically deflected sensor. The transfer function is calculated and the eigenfrequencies are extracted.

The measurement procedure requires a vibratory sensor, an automatic sampling of the transfer function and eigenfrequency extraction. The latter, is done inside a self-developed PC based signal analyzer [3]. It is generating the stim-

uli, samples data and calculats the eigenfrequencies using a function fit algorithm. The ability of vibration of MEMS depends on damping, in particular on fluidic damping. Often other sources of damping can be neglected. The used sensor arrays are over-damped to prevent overshooting and decreasing settling time. These sensors are not vibratory at atmospheric pressure, hence the pressure has to be lowered (less than 10^{-3} mbar). This is done in a vacuum chamber, which was developed for usage at the microscope with the installed LDV, Fig. 3.

Fig.3: Miniature vacuum chamber for characterization

2.3 The Data Evaluation

The data fusion of the FE-simulation and the measurements completes the method. For details see [2] and [5].

The FE data are fitted to polynomial functions

$$f_n(x_1, x_2, x_3) = \sum_{i=0}^{m}\sum_{k=0}^{m}\sum_{l=0}^{m} a_{n,i,k,l} x_1^i x_2^k x_3^l \qquad (1)$$

The calculated parameter matrix A (consists of an,i,k,l) is stored. Afterward, the measured eigenfrequencies are used in a weighted least squares fit to compute the needed parameters of the sensor:

$$\mathrm{Min}\left(\sum_{i=1}^{n}\left(\frac{f_{meas,i} - X A_i}{f_{meas,i}}\right)^2\right) \quad \forall x_1, x_2, x_3 \qquad (2)$$

3 Results and Comparison

The verification of the method and the test of the developed measurement equipment are done with the mentioned sensor arrays. The results of the method are shown in Table 1. The computed spring width was compared to an atomic force microscopy measurement, compare Fig. 4 and Table 1. The comparison shows a good match of the results.

Wafer position	Height in µm	Std.-dev.	Width in µm	Std.-dev	Wedge in µm	Std.-dev
Border	49,4	0,23	3,53	0,09	0,35	0,09
Middle	50,3	0,53	3,59	0,13	0,47	0,14

Table1: Parameters for 2 sensors consisting each of six spring - mass damping structures

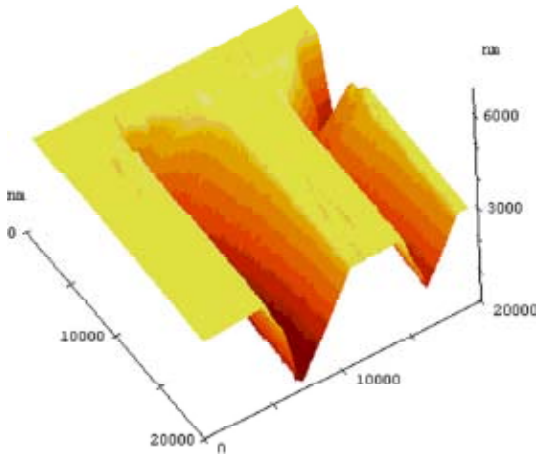

Fig.4: AFM image of a spring suspension (width 3,48 µm)

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Test-structures for characterization of geometrical parameters and stress in the microsystems

Alexey Shaporin[1]; Roman Forke[1]; Ralf Schmiedel[2]; Detlef Billep[3]; Jan Mehner[1]; Thomas Gessner[3]

[1]Chair Microsystems and Precision Engineering, Faculty for Electrical Engineering and Information Technologies, Chemnitz University of Technology, Chemnitz, Germany

[2]Center for Microtechnologies, Faculty for Electrical Engineering and Information Technologies, Chemnitz University of Technology, Chemnitz, Germany

[3]Fraunhofer IZM Chemnitz Branch, Chemnitz, Germany

1 Introduction

The increasing complexity as well as the progressive miniaturization of micro systems call for the development of suitable characterization techniques on wafer level. Micro mechanical sensors and actuators like acceleration sensors, vibration sensors, gyroscopes and micro mirrors form an important group of MEMS that are described as spring-mass-damping (SMD) systems [1]. High throughput manufacturing of these complex microsystems requires the implementation of advanced in-line measurement techniques, to quantify characteristic parameters and related scattering caused by the process conditions. Figure 1 shows a typical etch profile of micro mechanical structures. In contrast to the ideal rectangular form the MEMS structure is wedge-shaped. Also the mask undercut has to be taken into account. The deviation of geometrical parameters affects the system properties and has to be characterized.

Due to the small gaps and the high aspect ratios of microsystem elements (beams, electrodes) optical characterization methods cannot be used. It is also known that built-in mechanical stress influences the behaviour of micro mechanical structures. Raman spectroscopy and X-ray diffraction [2] are suitable for mechanical stress measurements, with a resolution of about 10 MPa.

But even stress less than 10 MPa can lead to strong changes in the behaviour of MEMS. The implementation of these measurement systems in the manufacturing process is hardly possible. Furthermore, it is time consuming because the structure has to be scanned. As mentioned above, most important parameters are not accessible by direct measurement techniques. Hence, indirect methods have to be developed in order to evaluate geometrical parameters and mechanical stress.

2 Test-structures characterization technique

The utilization of test-structures embedded in the wafer layout offers a solution of the mentioned problems [3]. Advantages of these test-structures over a typically complicated microstructure are:

- increased sensitivity of design parameters to process conditions,
- simplicity of the measurement approach and data evaluation,
- development of standardized test methods and conditions.

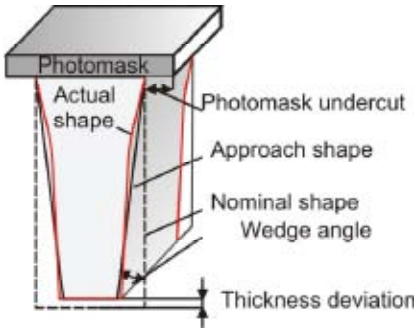

Fig.1: Technologically caused deviations

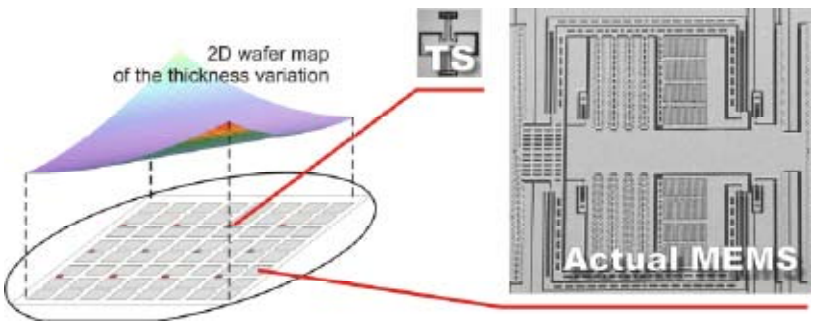

Fig.2: Concept of Test-Structures on wafer level

In order to stay cost efficient it is obvious that the test-structures have to be small compared to the actual micro system, Fig. 2. Non-contact measuring techniques are preferred for both, stimulation and response signal detection on microstructures.

Electrostatic fields usually provide enough energy for mechanical displacement, but a precise quantification of applied forces turns out to be difficult.

The observation of quasi-static force-displacement-functions is inappropriate. Alternatively, dynamic characteristics as Eigenfrequencies and related mode shapes are independent of the excitation magnitude and give valuable information about the mechanical behaviour of the micro component. The excitation scheme is shown in Fig. 3a.

The parameter identification is based on a three step procedure, Fig. 3:

1. Compute the theoretical response of the test-structure:

Several finite element runs have been utilized to simulate the Eigenfrequencies and mode shapes for different values of typical design parameters (numerical modal analysis). Results are represented by a multivariable mathematical fit function referred as "response surface".

2. Measure the actual response of the test-structure:

The structural response of test-structures is measured by a laser Doppler Interferometer (LDI), Fig. 3a and signal analyzer and transformed to Eigenfrequencies and related mode shapes known as "experimental modal analyses", Fig. 3c.

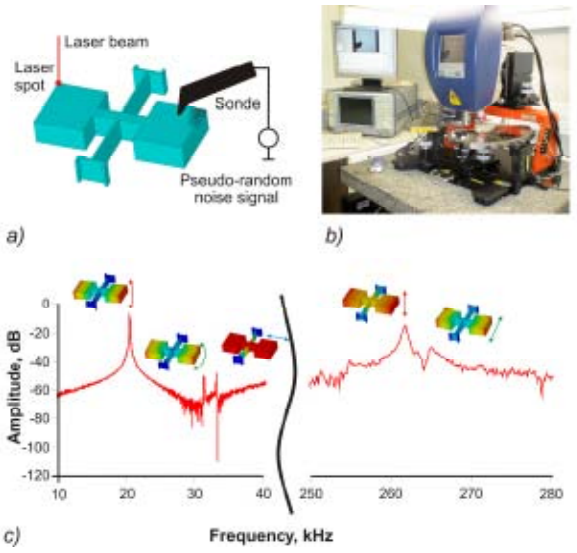

Fig.3: Experimental and theoretical analysis of test-structures

3. Correlate theoretical with actual response data:

Existing material properties and geometrical dimensions are evaluated by a least square fit of the theoretical and the measured structural response. Usually between four to six Eigenmodes provide sufficient information to capture most important design parameters. The last step of the presented characterization method for MEMS devices is the parameter identification. The results of the theoretical analysis and the Eigenfrequencies determination are combined to determine unknown searched parameters. Applying the least square error method one has to minimize the following function: It is important to note, that test-structures have been specially designed in order to increase the sensitivity to the searched parameters [4].

$$ResErr(p) = \sum_{i=1}^{N} \left(\frac{f_{FEM_i}(\bar{p}) - f_{exp_i}(\bar{p})}{f_{exp_i}(\bar{p})} \right)^2$$

$\bar{p}$ – searched parameters

N – number of Eigenfrequencies

$f_{FEM_i}(\bar{p})$ – nominal Eigenfrequencies calculated by FEM

$f_{exp_i}(\bar{p})$ – real Eigenfrequencies, experimentally measured by LDI

3 Geometry and stress characterization on wafer level

The technique has been implemented on wafers where primary MEMS structures and test-structures are processed together with the BDRIE (Bonding and Deep Reactive Ion Etching) silicon technology, Fig. 4a, [5].

The designed test-structures are subdivided into three types focused on the determination of different sets of parameters, Fig. 4b. Structures with mechanical stress compensation allow the determination of thickness, mask undercut and sidewall angles. Structures without mechanical stress compensation are directed on the additional determination of mechanical stress. Clamped-free beams with seismic masses are implemented to define the Young's modulus and the density of the material. Each test-field consists of the three

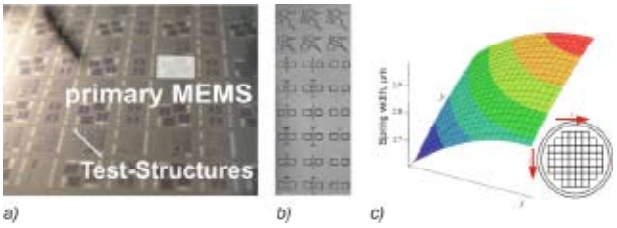

Fig.4: Characterization of geometrical parameters with test-structures

types of test-structures whereby the values for spring width and air gap width are varied in a certain range.

With the technique presented the variation of geometrical parameters for the whole wafer, Fig. 4c, has been obtained.

To determine mechanical stress within the MEMS chip and stress variations due to bonding and packaging steps of the fabrication process another set of test-structures was used. In order to obtain various stress situations test-structures were placed on the edges of unstructured membranes, Fig. 5a, membranes with SMD, Fig. 5b, and membranes with an opening, Fig. 5c. Fig. 5d shows SEM pictures of test-structures with and without stress compensation.

By now the wafer level characterization has been used after back side etching and releasing of the silicon structures. It is confirmed, that the chips show little stress (below 1 MPa) and small deviations of the geometrical parameters (e.g. 4…6 % decreased beam width). Thickness and width of test-structures have been measured by optical methods and profilometry. The next step will be the stress characterization after silicon-glass bonding.

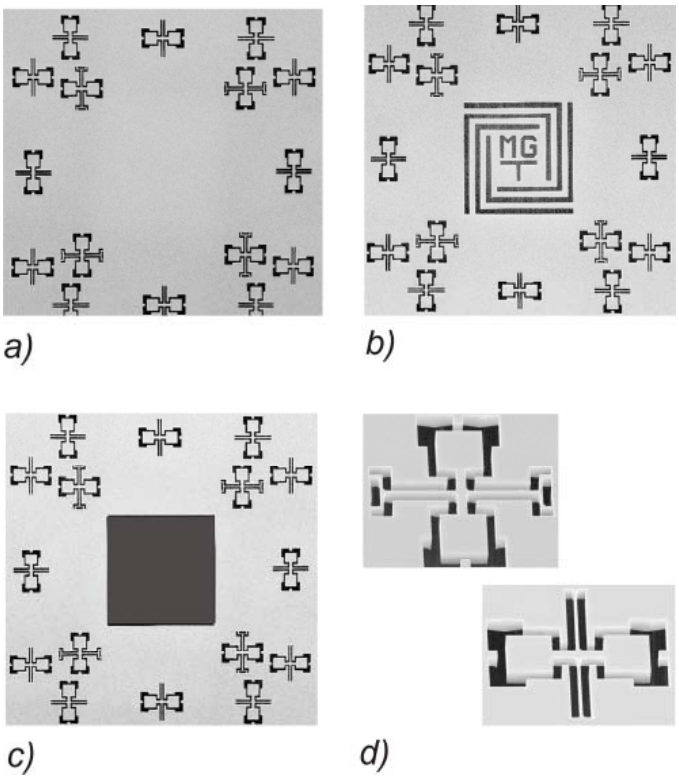

Fig.5: SEM images of chips designed for stress characterization due to bonding and packaging.

4 Summary

The use of test-structures for non-destructive wafer-level characterization of MEMS is a promising solution to monitor the fabrication process. With the presented test-structures geometrical parameters as well as mechanical stress have been determined. An acceptable correspondence between standard and proposed techniques has been found.

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Characterization of mechanical shock by impulse specific peak deflection (ISPD)

Steffen Kurth[1], Thomas Gessner[1,2], Alexey Shaporin[2]
[1]Fraunhofer IZM Chemnitz Branch, Department. Multi Device Integration, Chemnitz, Germany
[2]Chemnitz University of Technology, Chemnitz, Germany

1 Introduction

Since MEMS penetrate the world of consumer and automotive products more and more, a lot of effort is made to protect the devices from mechanical overload of sensitive parts like elastic suspensions or hinges (e.g. Ref.[1]). People involved in fabrication of sensitive MEMS like low g accelerometers, MEMS optical scanners, gyroscopes or other delicate MEMS devices know that handling of unprotected wafers as well as of the dies can lead to unexpected failure due to broken structures. In addition, hinge damages as result of simple handling mistakes are to be observed in spite of the fact that this devices passed shock tests in accordance to standard procedures, e.g. the Mil-Std-883 Method 2002 test condition A or the IEC 60474-14 standard. These standard procedures are widely accepted and devices which are tested in accordance to these procedures should not be damaged in the most common shock and vibration situations.

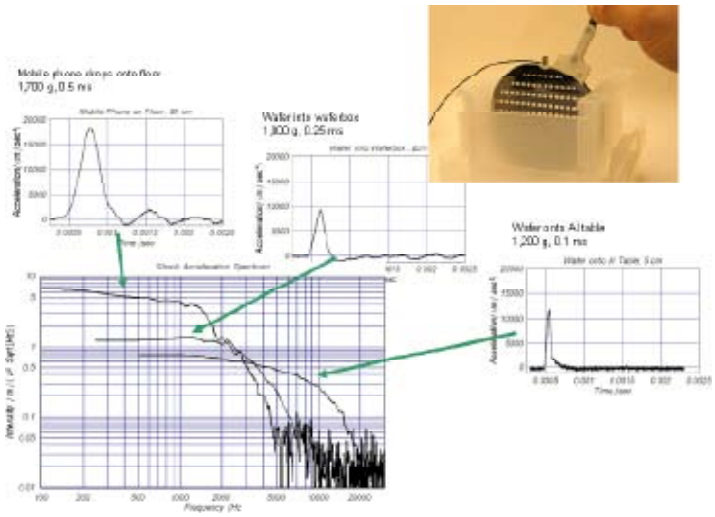

Fig.1: Spectrum densities and acceleration over time measured at impact of a mobile phone onto the floor and at impact of a silicon wafer onto an Al table and into a wafer transport box from 2 cm height respectively.

2 Description of the problem

Several realistic shock acceleration measurements have been performed to obtain information about the actual situation. The acceleration shocks of a mobile phone and of a 4 inch silicon wafer of 400 µm thickness have been recorded during different drop tests. An accelerometer (charge accelerometer type 4374, Bruel & Kjaer, with 0.65 grams weight, a mounted resonant frequency of 85 kHz and ±25,000 g shock full scale measurement range) has been used for monitoring of the acceleration.

The mobile phone was dropped on a floor PVC floor from 80 cm height and the acceleration peak was recorded several times. The accelerometer has been attached by special wax onto the printed circuit board of the Nokia 3110 mobile phone. A representative shock acceleration is depicted within Fig. 1. Since the case of the mobile phone is relatively weak, the peak is approximately 1700 g with a pulse length of 0.5 ms. The spectrum density at 3 kHz is nearly 20 dB lower compared to 500 Hz. It is somewhat comparable to the Mil-Std-883 Method 2002 condition B.

The 4 inch 400 µm thick Silicon wafer was dropped onto an 1 cm thick Al plate fixed on a laboratory table and dropped into a wafer transport box in that way that the wafer moves vertically and impinges with edge opposite to the main flat. The accelerometer has been attached by wax onto the main flat. An acceleration peak of 1000 g and 0.25 ms has been observed as representative shock for bringing the wafer into the wafer box by falling from approximately 2 cm height, Fig. 1.

Falling onto the Al table from 2 cm height was more intensive with 1200 g peak acceleration and 0.1 ms impulse length. The spectrum density shows a decay of 20 dB at 6 kHz and at 15 kHz respectively. In the frequency range from 5 kHz to 20 kHz, the acceleration spectrum density is more than one order higher than the measured values

from the mobile phone. The spectrum densities measured from the Silicon wafer are much stronger compared to the Mil-Std-883 Method 2002 impulse spectrum densities only in the high frequency range but not so severe in the low frequency range. How does it affect MEMS devices?

3 Calculation of impulse specific peak deflection (ISPD)

Assuming linear behavior, the complex deflection of movable MEMS parts is obtained by superposition of the reaction of all resonant modes, and mode decomposition leads to the reaction of the single modes of the multi degree of freedom system. It can be mathematically described by a system of differential equations which is transformed to a system of independent linear differential equations with each equation for a particular resonance mode characterized by eigenfrequency ω_0 and damping ζ. Stress is critical from the materials point of view. Since the mechanical stress and components of the stress tensor are proportional to recoverable strain or the strain tensor for elastic materials and since strain is related to mechanical deflection of structural elements (beams, plates, arbitrarily shaped flexures) it is most critical for material load situation. Hence, the analysis is focused on calculation of deflection.

Every mode follows the rules of this situation: The device is loaded from outside by vibration or by shock and deflects which can be mathematically described by the differential equations

$$m\ddot{x} + c\dot{x} + kx = p \tag{1}$$

with deflection vector **x** and load vector **p**, matrices of inertia **m**, damping **c** and stiffness **k** when it is assumed that the damping force is proportional to the velocity and the additional force by gas compression due to squeeze film effect and nonlinear effects by electrostatic or magnetic fields are negligible.

There are two ways to obtain the deflection of the mode under different mechanical load. First is to calculate the convolution of impulse response of the mechanical system $h(\tau)$ and the overload shock $a(\tau)$ in time domain

$$x(t) = \int_{t_0}^{t_1} h(\tau)a(t-\tau)d\tau \tag{2}.$$

The absolute maximum of the reaction gives information about the load to the material by the respective resonant mode. Second method is to transform the shock acceleration into frequency domain and multiply by frequency response function of the resonant mode. An inverse Fourier transform calculates the response of this mode in time domain. The second way is much more efficient since Fourier transform is done by numerical calculation faster than convolution. This way is followed here.

The general solution of the differential equation (1) yields after simplification and differentiating by time the impulse response:

$$h(t) = \frac{1}{\omega_0} E^{-\varsigma\omega_0 t}\sqrt{1-\varsigma^2}\sin\left(\omega_0\sqrt{1-\varsigma^2}\,t\right) + \frac{\varsigma^2}{\omega_0\sqrt{1-\varsigma^2}} E^{-\varsigma\omega_0 t}\sin\left(\omega_0\sqrt{1-\varsigma^2}\,t\right) \tag{3}$$

Practically, the convolution is replaced by multiplication in frequency domain and following inverse Fourier transform.

$$x(t) = \Im^{-1}(\Im(h(t))\Im(a(t))) \tag{4}$$

The ISPD is the maximum deflection in time domain $x_{max}(t)$ as function of the resonant frequency $\omega_0/2\pi$. In contrast to the pseudo velocity spectrum (Ref. [2]), the ISPD is directly related to mechanical stress in the device material.

4 Analysis of examples

Various shock acceleration functions will affect mechanical structures different. One can observe that a 500 g, 1 ms shock does not affect a MEMS structure whereas a 1000 g, 0.1 ms shock, which seams to be not so severe, damages it. Fig. 1 shows very different shock impulses in peak amplitude and length which force a mechanical system to different reaction, strongly depending on the resonance frequency and damping of the resonant modes. The aim of this analysis is to obtain the maximum peak deflection of the mechanical system for a certain shock to obtain information about mechanical load of the material in worst case, the possibly largest deflection. Fig. 2 shows the ISPD for 1000 g haver sine shock with 1 ms, 0.1 ms and 0.05 ms impulse length for instance. The calculated shock response for the 0.1 ms shock is additionally drawn into the plot for better understanding. Although the shocks have equal peak acceleration, the 1 ms shock is much more severe in the frequency range below 2 kHz compared to the 0.1 ms shock of course. The situation is different in high frequency range, with much higher deflection in case of the weaker 0.1 ms shock compared to the 1 ms shock.

The shock from the introduction section is analyzed and the ISPD can be compared to Mil-Std-883 test condition C in the plot of Fig. 3.

In spite of the higher acceleration spectrum density of short length shock loads in the upper frequency range, the shock with longer impulses are more harmful for MEMS devices. In high frequency range, the ISPD of the impact in the wafer box reflects higher severity of the shock compared to the shock according to the Mil-Std-833 Test Cont. C. This is important for high frequency resonant modes.

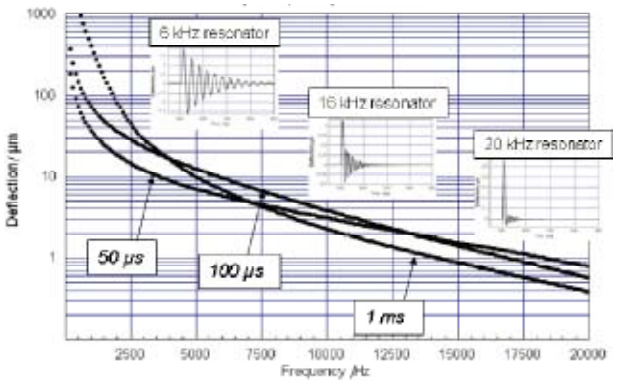

Fig.2: ISPD of 1000 g shock loads with 50µs, 100µs and 1ms shock length and the SDOF reaction of a 6 kHz, a 16 kHz and a 20 kHz system onto the 100 µs shock

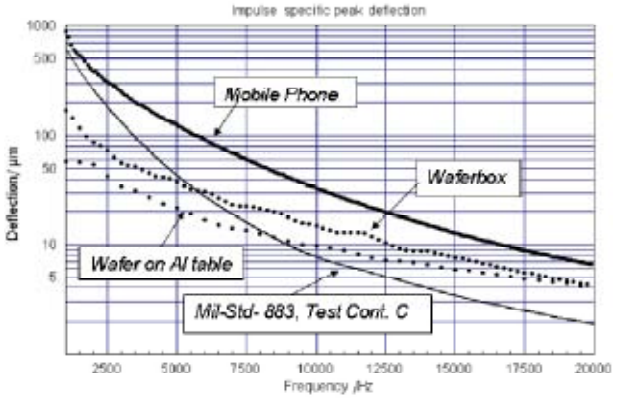

Fig.3: ISPD of the measured shock loads of mobile phone, wafer impinging onto the Al table, wafer impinging into wafer box and the Mil-Std-883 test condition C (3000 g, 0.3 ms) for reference

5 Summary and Conclusions

It has been found that the derived impulse specific peak deflection is useful to estimate how severe a particular shock forces a device to deflect its resonant modes with a certain resonant frequency respectively. The impulse specific peak deflection describes the deflection due to a shock in general for arbitrary resonant frequencies of the tested device. Arbitrary shocks can be analyzed. Shock impulses with short duration, which practically occur in many wafer and chip handling situations, are much more harmful for MEMS devices having high resonant frequencies compared to longer shock impulses with same acceleration level. It was shown that very short shock impulses of less than 0.05 ms can lead to damage of MEMS devices with high resonant frequency much more likely than 1ms impulses of same level.

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Education

Lectures

Diploma thesis and PhDs

International Research Training Group

Lectures

Chair Microtechnology

Process and Equipment simulation
Lecturers: Prof. Dr. T. Gessner, Dr. R. Streiter

Interconnect Processes and Technology – Back-end of Line (BEOL) Processing
Lecturers: Prof. Dr. T. Gessner, Dr. S. E. Schulz

Microtechnologies / Materials and Technologies of Microsystems and Devices
Lecturers: Prof. Dr. J. Frühauf, Prof. Dr. T. Gessner

Semiconductor Device Technology
Lecturer: Prof. Dr. T. Gessner, Dr. S. E. Schulz

Chair Microsystems and Precision Engineering

Design Technology and Production Engineering
Lecturer: Prof. Dr. J. Mehner

Device Technology
Lecturer: Prof. Dr. W. Dötzel

Microsystems
Lecturer: Prof. Dr. J. Mehner

Reliability and Quality Assurance
Lecturer: Prof. Dr. W. Dötzel

Control Engineering (Microsystem Technology)
Lecturers: Dr. J. Markert, Dr. S. Kurth

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Lecturer: Prof. Dr. J. Mehner

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Micro Production Technologies
Lecturer: Prof. Dr. G. Herrmann
(at the Brandenburg University of Technology Cottbus)

Micro Systems
Lecturer: Prof. Dr. G. Herrmann
(at the Brandenburg University of Technology Cottbus)

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Lecturer: Prof. Dr. G. Herrmann
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Advisor: DI Nestler

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Entwicklung einer industrietauglichen Fertigungstechnologie und Aufbau einer Bearbeitungsstation für das Lasertrimmen von Silizium-Mikroaktoren.
Advisors: Dr. Kaufmann, DI Hänel

Böhme, M.:
Elektrostatische Anregungen von MEMS zur Analyse des dynamischen Verhaltens.
Advisors: Prof. Dötzel, Dr. Kurth

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Advisors: Dr. Bertz, Dr. Hermann Schlemm (R&R)

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Gebauer, S.:
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Simulation & Entwurf gedruckter Schaltungen
Advisor: Dr. Kempa

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Upgrade und Optimierung von Prozessanlagen in der Lithografie
Advisors: Prof. Dötzel, Dr. Kiehnscherf

PhD / Habilitation

Heiko Wolfram:
Regelungstechnische Analyse und Synthese von MEMS mit elektrostatischem Wirkprinzip
Promotion zum Dr.-Ing., May 2007

Sven Zimmermann:
Entwicklung einer Technologie zur Herstellung eines neuartigen Substrates mit strukturierten vergrabenen Kobaltdisilizidschichten für eine gemeinsame Integration bipolarer und unipolarer Bauelemente auf einem SOI-Wafer
Promotion zum Dr.-Ing., October 2007

International Research Training Group
„Materials and Concepts for Advanced Metallization“

Internationales Graduiertenkolleg

At a Glance

Since 1st April 2006, the International Research Training Group (Internationales Graduiertenkolleg 1215) “Materials and Concepts for Advanced Interconnects”, jointly sponsored by the German Research Foundation (DFG) and the Chinese Ministry of Education, has been established for 4.5 years between the following institutions:

- Chemnitz University of Technology
  - Institute of Physics
  - Institute of Chemistry
  - Center for Microtechnologies
- Fraunhofer Institute for Reliability and Microintegration
- Technische Universität Berlin
- Fudan University, Shanghai
- Shanghai Jiao Tong University

This International Research Training Group (IRTG) is the first of its kind at Chemnitz University of Technology. It is lead by Prof. Ran Liu of Fudan University as the coordinator on the Chinese side and Prof. Thomas Gessner on the German side. A graduate school like this offers brilliant young PhD students the unique opportunity to complete their PhD work within 2.5 to 3 years in a multidisciplinary environment. Up to 14 PhD students of the German and 20 of the Chinese partner institutions, as well as a post-doctoral researcher at the Center for Microtechnologies are involved in the current program. The different individual backgrounds of the project partners bring together electrical and microelectronics engineers, materials scientists, physicists, and chemists. In particular, the IRTG is working to develop novel materials and processes as well as new concepts for connecting the devices within integrated microelectronic circuits. Smaller contributions are being made in the field of device packaging and silicides for device fabrication. In this sense, the IRTG project is helping to solve problems currently encountered on the way to nanoelectronics.

Fig.1: Prof. Thomas Gessner with Prof. Liu Ran, speaker of IRTG from Chinese side, and Prof. Ruan Gang, both member of Fudan University Shanghai, at the Novellus-Fudan workshop

Therefore, the research program of the IRTG concentrates on both applied and fundamental aspects, and treats the mid- and long-term issues of microelectronics metallization. Atomic layer deposition (ALD) of metals, new precursors for metal-organic chemical vapor deposition (MOCVD), ultra low-k dielectrics and their mechanical and optical characterization together with inspection techniques on the nanoscale are considered. New and innovative concepts for future microelectronics such as carbon nanotube interconnects or molecular electronics along with silicides to form links to front-end of line processes are of interest, as well as the evaluation of manufacturing-worthy advanced materials. Moreover, the research program addresses reliability and packaging issues of micro devices. Highlighting links between fundamental materials properties, their characteristics on the nanoscale, technological aspects of materials and their applications to microelectronic devices is the main objective of the program.

Nevertheless, the principal idea of the IRTG is fourfold: The research program defines the framework of

the activities and the topics of the PhD theses. This is accompanied by a specially tailored study program including lectures, seminars and laboratory courses to provide comprehensive special knowledge in the field of the IRTG. The third part of the program comprises annual schools held either in China or Germany, bringing together all participants of the IRTG and leading to vivid discussions during the presentation of the research results. Moreover, an exchange period of 3 to 6 months for every PhD student at one of the foreign partner institutions is another essential component. Besides special knowledge in the scientific field, these activities will provide intercultural competencies that cannot easily be gained otherwise.

In 2007, the second year of the IRTG, all PhD positions could be allocated. Eight of 15 positions (14 PhD and 1 postdoc position) have been assigned to female researchers. Such high percentage of women can only rarely be obtained in the fields of engineering and natural science.

Fig.2: Chinese and German Members of the IRTG during night boat tour on Huangpu River

Current Activities

Summer School

From 29th May to 4th June 2007 the second Summer School took place in Shanghai. The Summer School was organized by the School of Microelectronics of Fudan University, Shanghai and was held in conjunction with the 4th International Copper Interconnect Technology Symposium. This workshop is based on cooperation between the Chinese university and the American company Novellus Systems and is held every year in Shanghai. Dr. Zou Shi-Chang, member of the Chinese Academy of Science and President of the Shanghai Integrated Circuits Industry Association, opened the 4th International Copper Interconnect Technology Symposium. In his presentation he described the development of the Chinese economy as being in large parts based on the semiconductor industry. According to Dr. Zou, there is an imbalance of supply and demand of electronic products in China. He illustrated that only one third of the demand can be met by Chinese products. While Dr. Zou recognized the high standard of the theoretical higher education in China, he criticized that the students are not familiar enough with industrial processes and lack practical experiences, often due to insufficient laboratory facilities at the universities. Therefore newly established educational programs are intended to strengthen the practical training of the students and also involve the industry in the education. In this respect, Dr. Zou's presentation once again certified the necessity of the International Research Training Group which especially by the Mobility Period contributes to the practical education of the Chinese PhD students.

Most other invited speakers were scientists from the U.S. such as Dr. Jon Reid (Novellus Systems), Dr. Duane Boning (Massachusetts Institute of Technology) and Dr. David Ruzic (University of Illinois, Urbana-Champaign). In further invited talks, Prof. Thomas Gessner, coordinator of the International Research Training Group in Germany, gave an overview of the European activities in micro-and nanotechnology, and Dr. Stefan Schulz (Center for Microtechnologies, Chemnitz) presented recent results concerning the new field of vertical systems integration. Apart from the invited scientists, also four PhD students of the International Research Training Group had the opportunity to present their work during the three days of the Fudan-Novellus workshop. Three PhD students from Chemnitz, Nina Roth, Thomas Wächtler and Sukumar Rudra, as well as one PhD student from Fudan University, Chen Wei, demonstrated the current status of their PhD topics and answered the questions of the interested audience. Following the Fudan-Novellus workshop, the other 16 PhD students reported about the progress in their work during the Summer School. Both the Chinese and the German professors agreed that the PhD students showed an appreciable scientific advancement since the last Autumn School in November 2006 in Chemnitz.

The Summer School and Fudan-Novellus Workshop were flanked by a cultural and culinary program to become acquainted with the Chinese way of living and

culture. An excursion to the traditional village Zhujiajaio near Shanghai gave an impression of how Shanghai could have looked only some decades ago. Furthermore, a night boat tour on Huangpu River and a visit to Shanghai Museum were organized. Especially during these activities the PhD students got to know each other and vivid discussions and exchange of ideas developed. It was an open and sincere reunion, much different from the restraints sometimes observed during the first Autumn School.

Exchanging Program

Four Chinese PhD students and two German PhD students made use from the exchanging program last year. During this time, the fellows worked and studied at one of the foreign partner institutions in China or Germany.

From the German side, two chemists started a three-month stay at Fudan University Shanghai after the summer school. The Chinese PhD students, two from Fudan University and two from Shanghai Jiao Tong University, attended our lectures in the study program as well as social and cultural events.

The 14 PhD students and the Postdoc of th International Research Training Group are:

Name	Origin	Working field
Ramona Ecke (Postdoc)	Germany	Barrier and Copper CVD for 3D Integration
Nicole Ahner	Germany	Methods of cleaning sub 100 nm sustrures
Olga Bakaeva	Russia	Simulation of copper seed layer deposition
Olena Chukhrai	Ukraine	Mechanical characterization of thin films
André Clausner	Germany	Theoretical and practical treatment of lateral load in nanoindentation
Ines Eidner	Germany	Elastic under-bump structures for wafer level packaging
Sascha Hermann	Germany	Carbon nanotube interconnects
Saeideh Mohammadzadeh	Iran	Simulation of electronic transport properties in nanoscale interconnects
Anastasia Moskvinova	Russia	Characterization of electroplated copper and annealing processes by EBSD and TEM
Nina Roth	Germany	Transition metal complexes as precursors for CVD, spin on and ALD processes
Sukumar Rudra	India	Optical spectroscopy of ultrathin films
Uwe Siegert	Germany	Metal formiates and carboxylates as precursors for CVD, spin on and ALD processes
Teodor Toader	Romania	Electron spectroscopy studies of advanced interconnects
Marius Toader	Romania	Scanning tumnneling microscopy investigations
Thomas Wächtler	Germany	ALD of copper thin films

Public relations and Marketing

Memberships

Scientific publications

Trade fairs and events

International guests

Memberships of the directors board

Prof. Dr. Dr. Prof. h.c. mult. Thomas Gessner
Member of the Academy of Science of Saxony, Leipzig, Germany

Member of acatech (Council of Technical Sciences of the Union of German Academies of Sciences and Humanities)

Member of the Scientific Advisory Board of the Federal Republic of Germany

Member of "Senatsausschuss Evaluierung der Wissenschaftsgemeinschaft Gottfried Wilhelm Leibnitz" (WGL)

Member of the Board of „KoWi", Service Partner for European R&D funding, Bruessel

The Institute of Electrical and Electronics Engineers, Inc. (IEEE), USA

The Electrochemical Society, USA

Visiting professor at the Institute of Semiconductors at the Chinese Academy of Sciences in Beijing, June 2007

Principal Investigator in the World Premier International Research Center of the Tohoku University Sendai

„Advisory Professor" of FUDAN University: honorary professor, 1st June 1999

„Advisory Professor" of Chongqing University: honorary professor, 1st July 2003

Referee of the German Science Foundation (DFG-Fachgutachter) „Systemtechnik"

Dean of the Faculty of Electrical Engineering and Information Technology at TU Chemnitz since March 2006

Prof. Dr.-Ing. Ulrich Heinkel
edacentrum e.V., Hannover

Forschungsgesellschaft für Messtechnik, Sensorik und Medizintechnik e.V. Dresden

Sächsisches Netzwerk "Mikro- und biosensorische Messtechnik", Chemnitz

Prof. Dr.-Ing. habil. John Thomas Horstmann
The Institute of Electrical and Electronics Engineers, Inc. (IEEE), USA

Gründungsmitglied Nanotechnologie-Verbund NRW e.V.

Prof. Dr.-Ing. Prof. h.c. Josef Lutz
International Steering Committee of the European Power Electronics and Drives Association (EPE), Brussels

Member of the Advisory Board of the Power Conversion Intelligent Motion Conference (PCIM), Nuremberg

International programme committee of the International Seminar on Power Semiconductors (ISPS), Prague

International Technical and Scientific Committee of the Conference on Integration of Power Electronic Systems (CIPS)

Honourable professor at the North Caucasus State Technical University, Stavropol, Russia

Prof. Dr. rer. nat. Christian Radehaus
Optical Society of America (OSA)

The Institute of Electrical and Electronics Engineers, Inc. (IEEE), USA

The American Physical Society (APS)

Deutsche Physikalische Gesellschaft (DPG)

Prof. Dr.-Ing. Wolfram Dötzel
Member of the Academy of Science of Saxony, Leipzig, Germany

Member of acatech (Council of Technical Sciences of the Union of German Academies of Sciences and Humanities)

Gesellschaft für Mikroelektronik und Mikrotechnik (VDI/VDE-GMM)

ESPRIT III – Network „NEXUS"

Prof. Dr.-Ing. Gunter Ebest
Vertrauensdozent „Studienstiftung des Deutschen Volkes"

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Events and Colloquia in 2007

February 25th to March 18th, 2007
Exhibition "Mikrowelten – Zukunftswelten" at the Chemnitz University of Technology was accompanied by an exhibition of demonstrators developed at the Center for Microtechnologies

March 1st, 2007
final presentation of the Collaborative Research Center No. 379 : „Arrays of micromechanical sensors and actuators"

March 2nd, 2007
Innovation forum microsystem technologies at the fair SIT

March 27th and 28th, 2007
Smart Systems Integration Conference in Paris

July 9th, 2007
colloquium „New Jersey Nano Consortium – Bell Labs Ressources and examples of the development", Juergen Becker, Bell Labs

July 9th, 2007
Kickoff presentation of Smart Systems Campus Chemnitz

July 13th, 2007
colloquium „Adaptronics used in Adaptive Optics", Dr.-Ing. Timo R. Möller, manager of Genesis Adaptive Systeme Deutschland GmbH, Westhausen

August 31st, 2007
Colloquium „Nanotechnology for Electronics Packaging Applications", Prof. J. Morris, Portland State University, Portland, OR, USA

September 21st and 25th, 2007
Presentation of scientific results of the PhD students

October 15th to 17th, 2007
2nd German Microsystem Technology Congress Dresden

November 14th and 15th 2007
regional Microsystem Technology congress Chemnitz

Smart Systems Integration
Chair: Prof. T. Gessner

SMART SYSTEMS INTEGRATION 2007 European Conference & Exhibition (March 27th and 28th, 2007) was the first event of that kind held in Europe. An extensive know-how exchange in an intensive networking atmosphere characterized the opening event in Paris. Consequence of which was a consistently positive mood among enthusiastic conference participants, exhibitors and visitors.

285 participants from 16 European and 6 other countries supplemented by several external visitors took part.

SMART SYSTEMS INTEGRATION is the international communication platform for research, development and science to exchange know-how on Smart Systems Integration and to create a basis for successful research co-operations with focus on Europe. It is organized by Mesago Messe Frankfurt as well as Fraunhofer IZM (chair: Prof. T. Gessner) and part of the activities EPoSS.

Fig.1: SMART SYSTEMS INTEGRATION 2007 European Conference & Exhibition in Paris

Second German Congress on Microsystem Technologies
Chair: Prof. T. Gessner

The second German Congress on microsystem technologies was held from October 15th to October 17th, 2007 in Dresden. The 3 day congress, consisting of plenary sessions, lectures and poster sessions, an exhibition and a young scientist´s forum, was a forum for research and industry, producers and users, trainers and trainees, policy makers and networks. More than 1000 participants took part. The opening address was given by Annette Schavan, the Federal Minister of Research and Education, VDE-President Prof. Josef Nossek, the Prime Minister of Saxony Prof. Georg Milbradt, VW research director Prof. Juergen Leohold and Prof. Peter Gruenberg, the German Nobel Laureate in physics 2007. The importance of the microsystem technology for Saxony had been pointed out by Christian Esser Director Technology Development of Infineon Technologies GmbH & Co KG Dresden and the chairman of the congress Prof. Thomas Gessner, Director of the Center for Microtechnologies of the Chemnitz University of Technology and Head of the Chemnitz Branch of Fraunhofer Institute for Reliability and Microintegration. The feedback from participants was very positive.

Fig.2: Annette Schavan, the Federal Minister of Research and Education (left), VDE-President Prof. Josef Nossek (right), and Prof. Peter Gruenberg, the new German Nobel Laureate in physics (in the middle). The GMR effect of Prof Gruenberg is used in magnetic microsystem.

8th Congress on Microsystems in Chemnitz
Chair: Prof. Dr.-Ing. W. Dötzel,
Prof. Dr. G. Herrmann

On November 14th and 15th, 2007 the 8 regional Conference on Microsystems Technology took place in Chemnitz. The Conference has been organised by the Department of Electrical Engineering and Information Technology of Chemnitz University of Technology in Cooperation with GMM, the AMEC (Angewandte Mikroelektronik Chemnitz e. V.) and the Förderverein für Gerätetechnik und Mikrosystemtechnik Chemnitz e. V. Nearly 100 participants took part. An invited presentation concerning sensor applications in automotive was given by Bosch. The second invited talk was related to the new developments in Chemnitz, the smart systems campus.

In the afternoon of the second day of the conference a special meeting was held concerning the activities in the field of MEMS design and reliability.

Trade Fairs in 2007

nano tech 2007
International Nanotechnology Exhibition & Conference
Tokyo, February 21st to 23rd, 2007

SIT 2007
Sächsische Industrie- und Technologiemesse
Chemnitz, February 28th to March 2nd, 2007

Semicon China
Shanghai, March 21st to 23rd,2007

SSI 2007
Exhibition at Smart System Integration Conference
Paris, March 27th and 28th, 2007

HMI MicroTechnology
HANNOVER MESSE
Hannover, April 16th to 20th, 2007

Sensor & Test
The Measurement Fair
Nürnberg, May 22nd to 24th, 2007

MiNat
International Trade Fair for Precision Mechanics and Ultra-Precision, Micro and Nano Technologies
Stuttgart, June 12th to 14th, 2007

Micromachine
Exhibition Micromachine/MEMS
Japan, July 25th to 27th, 2007

Semicon Europa
Stuttgart, October 9th to 11th, 2007

Microsystem Technology Congress
Exhibition at MST Congress
Dresden, October 15th to 17th, 2007

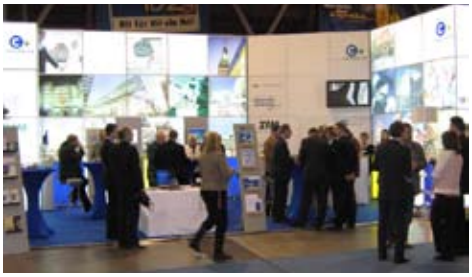


Fig.1: Center for Microtechnologies ZfM of Chemnitz University of Technology and the Chemnitz Business and Development Company (CWE) at SIT 2007 in Chemnitz

Fig.2: Fraunhofer Institute for Reliability and Microintegration IZM and Center for Microtechnologies ZfM of Chemnitz University of Technology at HMI MicroTechnology 2007 in Hannover

Fig.3: Center for Microtechnologies ZfM of Chemnitz University of Technology and the Chemnitz Business and Development Company (CWE) at Sensor and Test 2007 in Nuremberg

International Guests

Visiting scientists:

Prof. Vitaly Tarala,
North Caucasus State Technical University, Stavropol, Russia
January – March 2007

Dr. Fafa Chiker,
Algeria
January – December 2007

Associate Prof. Alexander Gridchin,
Novosibirsk State Technical University, Russia
September – November 2007

Dipl. Ing. Yaqing Chi,
P.R.China
October - December 2007

Dipl. Phys. Afshin Abbasi,
Iran
November – December 2007

Dr. André Möller,
SGS Fresenius Dresden
January 4th, 2007

Dr. Jarek Patyk, Dr. Pawel Szroeder,
Institute of Physics, University Torun,
Poland
February 1st, 2007

Dr. Reiner Taege,
Air Products GmbH, Hattingen
February 15th, 2007

Takashi Usuda,
National Metrology Institute Japan
March 1st, 2007

Eric van Grunsven,
Philips, Netherlands
March 2nd, 2007

Fred Roozeboom,
NXP, Netherlands
March 2nd, 2007

Renzo DalMolin,
Vermont, USA
March 16th, 2007

Dr. Reiner Taege,
Air Products GmbH, Hattingen
April 11th, 2007

Dr. Ian Buchanan,
Air Products European Electronics, Glasgow, Scotland
April 11th, 2007

Dr. John A. T. Norman,
Air Products, Carlsbad CA, USA
April 11th-12th, 2007

Jean-Luc Delcarri & Thierry Remy,
Altatech, Semiconductor, Montbonnot, France
April 16th-17th, 2007

Dr. rer. nat. Verena Vescoli,
Austria Microsystems, Graz, Austria
June 6th, 2007

Masayoshi Shiosaki,
Omron, Japan
June 15th, 2007

Robert Preisser,
Atotech Deutschland
June 21st, 2007

Eugene Baryschpolec,
Air Products, Belgium
July 11th – 12th, 2007

Prof. J. Morris,
Portland State University, Portland, OR, USA
August 31st, 2007

Prof. Viktor A. Gridchin
Novosibirsk State Technical University, Russia
November 13th-23rd, 2007

Prof. Alexander A. Velichko
Novosibirsk State Technical University, Russia
November 13th-23rd, 2007

Prof. Vladimir A. Ilyushin
Novosibirsk State Technical University, Russia
November 13th-23rd, 2007

Eugene Baryschpolec,
Air Products, Belgium
November 26th -27th, 2007

Dr. Kompat Satitkovitchai
Thailand
December 11th-13th, 2007

Les Molnar,
Air Products, Allentown, PA, USA
December 13th, 2007

Eugene Baryschpolec,
Air Products, Belgium
December 13th, 2007

Students:

Eduard Yang
Portland State University, USA
June – September 2007 (ISAP)

Joel Rieger
Portland State University, USA
June – September 2007 (ISAP)

Popazu, Cristina
Universität "Politehnica" Bukarest, Romania
October 2006 – March 2007 (SOCRATES)

Scientific coworkers / PhD:

Tatjana Prohoda
North Caucasus State Technical University, Stavropol, Russia
October 2006 - March 2007

Ping Liu
Shanghai Jiatong University, China
December 2007 – March 2008

International Research Training Group „Materials and Concepts for Advanced Interconnects"

Olena Chukhrai
Ukraine

Teodor Toader
Romania

Sukumar Rudra
India

Anastasia Moskvinova
Russia

Olga Bakajeva
Russia

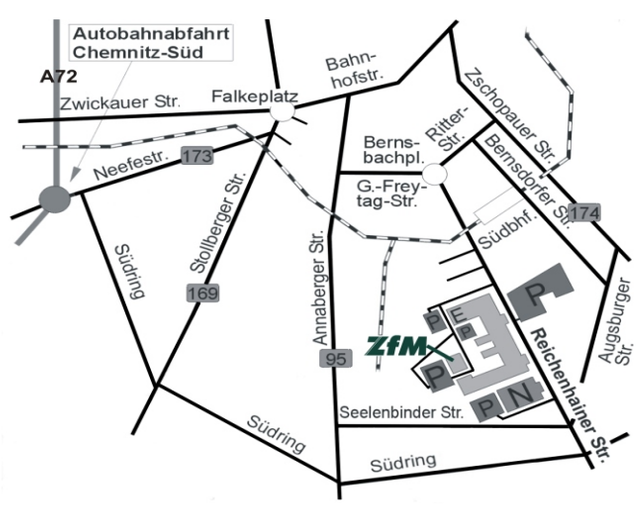
Saeideh Mohammadzadeh
Iran

Mahoud Abdel-Hafiez (associated)
Egypt

Jin-Yi Wang
Fudan University Shanghai
June 2007 – October 2007

Yiming Jiang
Fudan University Shanghai
June 2007 – October 2007

ZfM
Zentrum für Mikrotechnologien



Contact:

Prof. Dr. Dr. Prof. h.c. mult.
Thomas Gessner
Head of Center for
Microtechnologies

Chemnitz University of Technology
Faculty of Electrical Engineering and
Information Technology
Center for Microtechnologies
Reichenhainer Strasse 70
D-09126 Chemnitz

Phone: +49 (0)371 531 24060
Fax: +49 (0)371 531 24069

E-mail: info@zfm.tu-chemnitz.de
http://www.zfm.tu-chemnitz.de

Co-operation partner:

Fraunhofer Institute for Reliability
and Microintegration IZM
Chemnitz Branch of the Institute
Reichenhainer Strasse 88
D-09126 Chemnitz

http://www.izm.fraunhofer.de/standorte

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Fraunhofer Institut Zuverlässigkeit und Mikrointegration